Torque Ripple Control of BLDC Motor Using SVM Technique

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Abstract: Brushless dc (BLDC) motors, due to their inherently sensor less operation, are considered as viable candidates in large scale production industries say, the automotive one. Within this trend, the minimization of torque ripples becomes mandatory for a smooth operation. Compared with the sinusoidal PWM strategy, the SVM strategy shows improved reliability due to the balanced switching frequencies achieved in the inverter upper and lower insulated-gate bipolar transistors on one hand and scaling down in the average value of the motor common mode voltage on the other hand. Furthermore, the torque ripple is significantly reduced during sector-to-sector commutations. An experimentally based comparative study of PWM gating pulses and SVM gating pulses is made in the MATLAB2013/SIMULINK environment which clearly highlights the potentials exhibited by the later one.

Key words: Space vector modulation(SVM) · Pulse width modulation(PWM) · Brushless dc motor (BLDC)

INTRODUCTION

Considering the last three decades AC machine drives are becoming more popular, especially Induction Motor (IM) and Permanent Magnet Brushless DC Motor (PMBLDC), but with some special characteristics [1], the BLDC drives are ready to match the sophisticated needs such as fast dynamic response, high power factor and wide operating speed range, as a result, a gradual gain in the use of BLDC drives will surely be witnessed in the future in low and mid power applications [2, 3]. Dealing with BLDC motor control strategies it is quite commonly believed that they are based on current and torque control approaches. Among the most popular strategies is the generalised harmonic injection to find out optimal current waveforms minimizing the torque ripples [4, 5, 6].

Green car manufacturers and entities like NASA prefer BLDC motors because of their quick motor responses. The high-performance and the small-diameter magnetic rotors reduce the inertia of the armature, allowing high acceleration rates, decrease in rotational losses and smoother servo characteristics. This optimal motor response leads to more constant speeds, instant speed regulation and a quieter drive system [7, 8].

Comprising with above mentioned many special characteristics of BLDC is the present day researcher’s hotspot. It can be operated at improved power factor for which the overall system power factor is improved. BLDC drive could become an emerging competitor to the IM drive in servo like industrial applications. There is a great challenge to improve the performance with accurate speed tracking and smooth torque output minimizing its ripple during transients [9, 10]. It has been reported that in [11] that the two phase conduction mode is penalized by torque ripple in sector to sector commutation [12].

In order to apply voltage to the motor, it is required to convert this reference voltage $U_r$ to the switching signals of the inverter. There are several strategies to produce gating signals. Here both pulse width modulation (PWM) and space vector modulation technique (SVM) are used to generate gate pulses to the inverter [13].

Principle of PWM: The sinusoidal PWM scheme for a two-level inverter is illustrated in Fig. 2, where $V_{na}$, $V_{nb}$ and $V_{nc}$ are the three-phase sinusoidal fundamental waves and $V_{c}$ is the triangular carrier wave. The fundamental-frequency component in the inverter output voltage can be regulated by amplitude modulation index.
Fig. 1: General block diagram

Fig. 2: Sinusoidal pulse width modulation

\[ m_a = \frac{V_m}{V_{cr}} \]  \hspace{1cm} (1)

where \( V_m \) and \( V_{cr} \) are the peak values of the fundamental and carrier waves, respectively. The amplitude of the modulation index \( m_a \) is usually given by varying vector \( V_m \) while keeping vector \( V_{cr} \) fixed. The frequency modulation index is defined by:

\[ m_f = \frac{f_{cr}}{f_m} \]  \hspace{1cm} (2)

where \( f_m \) and \( f_{cr} \) are the frequencies of the fundamental and carrier waves, respectively. The ON and OFF of switches S1 to S6 is determined by comparing the fundamental waves with the carrier wave. When \( V_m \) is greater than or equal to \( V_{cr} \), the upper switch S1 in inverter leg A is turned ON. The lower switch S4 operates in the opposite manner and so it is turned OFF. The resultant inverter terminal voltage \( V_{AN} \), which is the phase A voltage with respect to the negative dc bus, is equal to the dc voltage \( V_d \). When \( V_m \) is less than \( V_{cr} \), S4 is on and S1 is off, leading to...
V_{AN} = 0. As the V_{AN} wave form has only two levels, V_1 and zero, the inverter is known as a two-level inverter. In order to avoid short circuit during sudden switching transients of the upper and lower devices in an inverter leg, a blanking time is implemented, during which both switches are at off state. The inverter line-to-line voltage V\_{AN} is given by V_{AN} = V_{AN} - V_{BN}. The fundamental-frequency component V_{AB1} waveform is also given in the figure. The magnitude and frequency of V_{AB1} can be controlled independently by ma and fin, respectively. The switching frequency of the ON state switches in the two-level inverter can be found from f_{sw} = f_m \times \text{m}. For instance, V_{AN} in Fig. contains nine pulses in one cycle of the fundamental frequency. Each pulse is produced by turning S1 ON and OFF once. With the fundamental frequency of 60 Hz, the obtained switching frequency for S1 is f_{sw} = 60 \times 9 = 540 Hz, which is also the carrier frequency f_c. It is of no worth since the device switching frequency may not always be equal to the carrier frequency in multilevel inverters. When the carrier wave is synchronized with the modulating wave (fm is an integer), it is known as synchronous PWM, which is in contrast to asynchronous PWM whose carrier frequency (4) is usually fixed and independent of f_c. The asynchronous PWM has a fixed switching frequency and easy implementation with analog circuits. However, it may generate non characteristic harmonics. The synchronous PWM scheme is more suitable for implementation with a digital processor.

**Space Vector Modulation for Three Leg Voltage Source Inverters:** The switching state topology of a three-leg voltage source inverter is shown in Fig. 3. Because of the limit that the input lines must not be shorted and the output current must always be continuous a inverter can assume only eight different topologies. Six of these eight topologies gives a nonzero output voltage and are known as non-zero switching states and the other two topologies filled with zero vectors.

**Control Scheme:** Taking into account the operation basis of BLDC motor drives, a SVM strategy dedicated to these drives in the case of a B6-inverter in the armature could be inspired from the one considering the case where the motor is fed by B6-inverter. The implementation scheme of such a SVM strategy is shown in Fig. 4.

**Switching Timing:** In Fig. 5, U_i can be approximated based on timely switching among U_{100}, U_{110} and the two zero vectors. In this case, vector U_{100} should be applied for a longer time than U_{110} since U_1 is nearer to U_{100}; and a time of zero vectors should also be applied to reduce the magnitude.

The calculation of the durations of the base vectors is described based on Figure 6.

If the reference voltage space vector U_1 falls between two adjacent base vectors, U_i and U_j, the reference vector U_1 can be represented with the combination of the two vectors, U_i and U_j.

\[ u_i = r_1 u_1 + r_2 u_2 \]  

\[ \begin{align*}  
  r_1 &= \sqrt{3} \frac{u_{dc}}{u_{dc}} \sin(60^\circ - \theta) 
  
  r_2 &= \sqrt{3} \frac{u_{dc}}{u_{dc}} \sin \theta 
\]  

where U_i and U_j are the length of the two vectors and U_1 is the length of vector U_c. To summarize we get.

\[ \begin{align*}  
  T_0 &= (1 - r_1 - r_2)T 
  
  T_1 &= r_1T 
  
  T_2 &= r_2T 
\]  

where T is the PWM period, T_0 is the duration for zero vector and T_1 and T_2 the durations for vector U_i and U_j, respectively. These equations mean that an arbitrary space vector enclosed by the triangle defined by the two adjacent base vectors, between which the particular vector is present, can be represented by the sum of these
Fig. 3: Eight switching state topologies of a voltage source inverter

Fig. 4: Block diagram of SVM strategy

Fig. 5: Voltage space vectors available using a three phase inverter

Fig. 6: Approximation of arbitrary voltage space vector using base vectors

Fig. 7: Combination of vectors by time division

Fig. 8: Seven segment switching for $V_{ref}$ in sector I

Table 1: Vector sector table during sector to sector commutation during counter clockwise rotation

<table>
<thead>
<tr>
<th>Sector</th>
<th>Sector</th>
<th>Vector</th>
</tr>
</thead>
<tbody>
<tr>
<td>VI</td>
<td>I</td>
<td>$U_1(01110)$</td>
</tr>
<tr>
<td>I</td>
<td>II</td>
<td>$U_2(001110)$</td>
</tr>
<tr>
<td>II</td>
<td>III</td>
<td>$U_3(000111)$</td>
</tr>
<tr>
<td>III</td>
<td>IV</td>
<td>$U_4(100011)$</td>
</tr>
<tr>
<td>IV</td>
<td>V</td>
<td>$U_5(110001)$</td>
</tr>
<tr>
<td>V</td>
<td>VI</td>
<td>$U_6(111000)$</td>
</tr>
</tbody>
</table>

Two vectors $V_1$, $V_2$, and $V_0$. The sampling period $T$ can be split into seven segments for the selected vectors.

The following results can be observed:

Two vectors $V_1$, $V_2$, and $V_0$. The sampling period $T$ is short, the approximation can accurately represent the reference vector.

Seven Segment Switching: Seven-Segment switching sequence and inverter output voltage waveforms for reference voltage in sector I, where reference voltage is synthesized by $V_1$, $V_2$, and $V_0$. The sampling period $T$ can be split into seven segments for the selected vectors.

The following results can be observed:
The dwell times for these seven segments are summed up to the sampling period \( (T_s = T_1 + T_2 + T_3) \). Design requirement (a) is satisfied. For instance, the transition from \([OOO]\) to \([POO]\) is achieved by turning \(S1\) on and \(S4\) off, which involves only two switches.

The redundant switching states for vector \( V_o \) are utilized to reduce the number of switching per sampling period. For the \( T_s/4 \) segment in the centre of the sampling period, the null switching state \([PPP]\) is selected, whereas for the \( T_s/4 \) segments on both sides, the null state \([OOO]\) is used.

Each of the switches in the inverter turns on and off once in a sampling period. The switching frequency \( f_{sw} \) of the switches is thus equal to the sampling frequency \( f_{sp} \), that is, \( f_{sw} = f_{sp} = 1/T_s \).

The vector selection table for the proposed system is shown below:

**Advantages of SVM over PWM:** In SVM, it is possible to generate the switching signals directly using the space vector of the reference voltage, without converting the space vector to the three phase values at first as in PWM.

The obtained results showed that, the proposed SVM inverter have stator current with low harmonic distortion and low active and reactive powers ripples (about 65\%) than PWM inverter.

Compared to PWM the Total harmonic distortion (THD) and lower order harmonics (LOH) contents are less in SVM.

In the space vector PWM technique, there is a increase of 15\% maximum voltage compared to PWM, hence Space Vector enables efficient use of DC voltage.
Fig. 9d: Hall signals

Fig. 9e: Torque waveform

Fig. 10a: SVM gate pulses

Fig. 10b: Stator current waveform
Simulation Results: The simulation results for the steady-state operation of the BLDC motor under the proposed DTC strategy for a speed \( \omega_m = +25 \text{ rad/s} \), respectively are illustrated by the following waveforms.

Fig. 9a-9e are the output waveforms of the BLDC motor when operated under SVM technique.

Fig. 10a-10e shows the output waveforms of the BLDC motor when operated under SVM technique.

SVM technique has the advantage of less harmonic content, which is useful in applications that need a low harmonic level for preventing overheats and malfunction in sensitive systems.

Table 2: THD comparison table

<table>
<thead>
<tr>
<th>Motor Output</th>
<th>THD%</th>
<th>SVM%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stator current A</td>
<td>157.18</td>
<td>46.90</td>
</tr>
<tr>
<td>Stator current B</td>
<td>141.61</td>
<td>55.32</td>
</tr>
<tr>
<td>Stator current C</td>
<td>105.94</td>
<td>50.40</td>
</tr>
<tr>
<td>Electromagnetic torque</td>
<td>157.59</td>
<td>53.29</td>
</tr>
</tbody>
</table>

Space Vector Modulation provides best output performance, optimized efficiency and high reliability compared to similar Inverters with conventional PWM.
CONCLUSION

This project has proposed a novel SVM strategy dedicated to the control of BLDC motor drives. Torque ripples in the BLDC motor drive will lead to speed oscillations and excitation of resonances in mechanical portions, leading to acoustic noise and visible vibrations. Minimization or elimination of these ripples is considerable issue in BLDC drive. It has been found that the motor operated under SVM pulses is said to have about 60% less Torque ripples when compared with the PWM carrier pulses provided under open loop condition.

REFERENCES