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Algorithm of Failure Detection of Digital Transceivers Made by System-On-Chip Technology

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Abstract: Suggested an algorithm of the digital transceiver failure detection if the transceivers are made using System-on-Chip technology. The algorithm is based on utilization of radio signal characteristic estimation using vector signal analyzer. There are given the results of different failures modeling and their influence on the signal characteristics as well as the results of a digital transmitter experimental investigation using the analyzer FSV produced by the firm Rohde & Schwarz.

Key words: Vector signal analyzer • Bit error rate • Vector of error • Diagram 'constellation' • Vector diagram

INTRODUCTION

Modern technology trends towards miniaturization of devices and power consumption decrease. Realization of a full functioning device within a microcircuit System-on-Chip (SoC) allowed to solve two those problems but made the process of failure detection and repair more complicated. Digital receivers and transmitters produced by SoC technology don't allow the access to test points in order to observe the signals. So, getting the big value of the bit error rate (Bit Error Rate - BER; methods of BER measurement are described in [1]), designers have no opportunity to estimate the kind of the error, using standard analyzers. The error could be detected by a vector signal analyzer (VSA) able to demodulate the signal at the transmitter output and to decode it according to the standard chosen. The article suggests the algorithm of digital equipment failure detection based on signal characteristics estimation using VSA. Table 1 describes characteristics provided by VSA.

Besides, the vector analyzer calculates error of amplitude and phase and vector error (Error Vector - EV; information about EV is described in [2]). It also allows to observe time variations of these errors.

Algorithm of Failure Detection: The algorithm of failure detection utilizes comparison of the signal under investigation characteristics and the defects of the digital transceiver inner blocks. The algorithm consists of several steps starting with investigation of the transmitter output dynamic range and the receiver input with amplifiers. Influence of signal compression in amplifiers is defined using vector diagram and EV time dependence. If EV suddenly grows at the moment of the instantaneous power maximum, the signal compression provides unacceptable distortion and worsens decoding (grows of BER) [3]. If vector diagram and EV time dependence don't show any detects in amplifiers the next step is to test the circuits putting the frequency up/down and the IF filters. Errors could show up in discrepancy of the IF filters frequency characteristics and the wrong signal group delay which leads to errors at the stage of decoding. In order to find this defects scattering of the measured symbols around the ideal positions in the constellation diagram and the EV time dependence should be investigated. Constant in time high level of EV in case of wide scattering of points in the constellation diagram mean the defect of filters. To be sure IF filter characteristics should be tested separately using debugging tools of SoC.

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Name	Description		
Eye diagram	Characterizes summery appearance of all symbol periods of the signal part under measurement put on each other;		
	allows to estimate the quality of reference oscillators and circuits of the symbolic velocity restoration.		
Vector diagram	Characterizes the signal instantaneous power within two-dimensional complex plane.		
Constellation diagram	Characterizes the received symbols within two-dimensional complex plane relative to the ideal symbol positions.		
Spectrogram	Characterizes dependence of the signal spectral power density on time.		
Eye diagram Vector diagram Constellation diagram Spectrogram	Characterizes summery appearance of all symbol periods of the signal part under measurement put on each other; allows to estimate the quality of reference oscillators and circuits of the symbolic velocity restoration. Characterizes the signal instantaneous power within two-dimensional complex plane. Characterizes the received symbols within two-dimensional complex plane relative to the ideal symbol positions. Characterizes dependence of the signal spectral power density on time.		

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Fig. 1: Results of the interfering signals influence on the EV time characteristic (*a*), frequency characteristic of the error vector (*b*) and the 'constellation' diagram (*c*)



Fig. 2: The constellation diagram in case of quadrature offset (a), gain imbalance of the quadrature (b)

Mixers could be the sources of high level combination signals (interferential, disturbing) deforming the form of symbols and making decoding more difficult. Scattering in the constellation diagram in parallel with the EV periodic variations testify to the interfering signal presence. The source of these interference signals could be found using the EV frequency characteristic got by the vector signal analyzer in the process of Fourier transformation of EV time dependence.

Results of MatLab modeling of the interfering signals influence on the EV time characteristic, EV frequency characteristic and the 'constellation' diagram are shown in Fig. 1, α , β , c. The wanted signal S(t) is mixed with two interfering signals with frequencies 50 and 100 kHz and amplitudes A, B:

$$S'(t) = S(t) + A\sin(2\pi.\ 50 \times 10^3.t) + B\sin(2\pi.\ 100 \times 10^3.t).$$
 (1)

Fig. 1*a*, shows EV time dependence in the complex plane - the error vector grows and goes round the point (0,0). It is difficult to tell this effect from the usual scattering in the defective IF filter or from the influence of high noise. After investigation of the error vector (Fig. 1*b*,) becomes clear the presence of two interfering signals with frequencies 50 and 100 kHz. They scatter the symbols around the ideal position (Fig. 1*c*).

If there are no errors mentioned above it is necessary to investigate distortions of quadrature modulation and demodulation. There are possible the following distortions: quadrature offset, gain imbalance of the quadrature, quadrature phase offset. The constellation diagram is the most convenient mean of the quadrature investigation. Results of modeling are shown in Fig. 2*a.b.*



Fig. 3: The constellation diagram in case of quadrature phase offset



Fig. 4: The constellation diagram on VSA monitor in case of quadrature offset (*a*), gain imbalance of the quadrature (*b*)

In case of the quadrature offset by some positive value C the signal symbols in the constellation diagram also shift along the axis Q relative the ideal position (Fig. 2a). The signal in this case is described as follows:

$$S(t) = I(t) \cdot \cos \omega t - Q'(t) \cdot \sin \omega t = I(t) \cdot \cos \omega t - [C + Q(t)] \cdot \sin \omega t.$$
(2)

Where I(t), Q(t)- sign changing modulating digital streams of the transmitter in-phase and quadrature chanels.

In case of the gain imbalance the signal symbols in the constellation diagram moves along the axis Q relative the ideal position (Fig. 2b). The signal in this case is described as follows:



Fig. 5: The constellation diagram in case of quadrature phase offset on VSA monitor

$$S(t) = I(t). \cos \omega t \ Q^{2}(t) \ . \sin \omega t = I(t). \cos \omega t + D.Q(t). \sin \omega t,$$
(3)

Where D < 1.

Condition of quadrature components ortogonality is violated at the phase (φ) which leads to change of the symbols value and rotation of the constellation diagram relative the ideal symbol positions (Fig. 3). The signal in this case can be described as follows:

$$S(t) = I(t). \cos \omega t - Q(t). \sin(\omega t + \varphi)$$
(4)

Then it is necessary to investigate whether the filter standard corresponds the envelope of the transceiver. It is especially important for the systems which envelope characteristics have the form of the raisedcosine. If they don't correspond the shape of the raisedcosine interference between the symbols becomes possible [4]. It increase EV at the moments of the symbol transaction, which is easily discovered by the spectrum analyzer.

Experiment: The suggested algorithm was tested using the vector signal generator SMBV100A and the vector signal analyzer FSV produced by Rohde & Schwarz. The generator was used as a transmitter which allowed to add to the signal different distortions. Fig. 4,5 show some results of investigation.

CONCLUSION

The algorithm suggested in the paper allows to detect failures of inner blocks of the transceivers built using technology SoC. Results of experiments proved the results of modeling. The suggested algorithm can be used at the stage of design of new digital cell system equipment, INTERNET access, digital TV and so on. Besides, the suggested algorithm can be also used as an expert system or atomized systems of digital communication equipment testing.

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