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Design of Signed Multiplier Using T-Flip Flop

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Abstract: In VLSI, Digital multipliers play a vital role when compared to the critical arithmetic functional units. The performance of the multipliers depends on the throughput and the variable latency. The negative bias instability effect of the pMOS transistor will increase the threshold voltage and it reduces the speed. Similarly the positive bias temperature instability effect occurs in an nMOS transistor, when the nmos transistor is positive biased. Both of these effects diminish the speed and bring in the aging effect in the transistor. Therefore it is essential to propose reliable high performance signed multipliers. This project deal with the multiplication of signed multiplicand with signed multiplier (Design 1) and signed multiplier with unsigned multiplicand (Design 2). Modified razor flip-flop checks for any path delay timing violations and to mitigate performance degradation due to aging effect. The signed number is converted into two's complement number using T-flip-flop. The proposed design 1 and design 2 architecture are applied to array, column and row bypassing multiplier and it is synthesized using Xilinx ISE Design Suite 13.2. The power is analyzed using Xpower analyzer. The total memory usage and the power of the proposed design 1 and design 2 are compared with the conventional unsigned multipliers.

Key words: Component · Signed multiplier · Razor flip flop

INTRODUCTION

Digital multipliers play a vital role in many applications, such as the Fourier transform, discrete cosine transforms and digital filtering. The throughput of these applications depends on multipliers and if the multipliers are too slow, the performance of complete circuits will be reduced.

In addition, negative bias temperature instability (NBTI) occur when a pMOS transistor is less than negative bias (Vgs = -Vdd) [1], [2]. BIAS temperature instability (BTI) is a degradation event mainly affecting MOS field effect transistors. The highest impact is observed in p-channel MOSFETs which are stressed with negative gate voltages at higher temperatures. A very interesting aspect of device degradation caused by NBTI is its capability to anneal to a certain extend when the stress conditions are diminished [3], [4]. In this situation, the interaction between inversion layer holes and hydrogen - passivated Si atoms splits the Si–H bond generated during the oxidation process, generating H or H2 molecules. When these molecules diffuse away, interface traps are left. The accumulated interface traps between silicon and the gate oxide interface resulting in increased threshold voltage (Vth), reducing the circuit switching speed. When the biased voltage is removed, the reverse reaction occurs, reducing the NBTI effect. However, the reverse reaction does not eliminate all the interface traps generated during the stress phase and Vth is increased in the long term. Hence, it is important to design a reliable high-performance multiplier [11]. The corresponding effect on an nMOS transistor is positive bias temperature instability (PBTI) [5-9], which occurs when an nMOS transistor is under positive bias. Compared with the NBTI effect, the PBTI effect is much smaller on oxide/polygate transistors [10] and therefore is usually ignored. In the proposed work,

- Both Multiplicand and multiplier bit as a signed bit (Design 1)

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- Multiplicand as unsigned bit and multiplier as a signed bit (Design 2) is implemented using array, column bypass and row bypass multiplier design in order to generate the product term and the razor flip-flop is used to detect the error. The proposed multipliers are compared with the conventional unsigned multipliers.

Ease of Use: A literature survey is prepared for various papers which are essential to know the previously available techniques, their significance and limitations. It also includes various supporting papers that can meet the objective of the topic chosen. There are many approaches available for variable latency design and the implementation of reliable multiplier. The following literature survey provides an overall idea about the previously done works in this field and their significance. Mauro Olivieri proposed variable-latency multiplier architecture [11], suitable for implementation as a self-timed multiplier core or as a fully synchronous multicycle multiplier core. Ing-Chao Lin, Yu-Hung Cho and Yi-Ming Yang proposed Reliable Multiplier Design with Adaptive Hold Logic [12]-[14]. Meanwhile, the negative bias temperature instability effect occurs when a pMOS transistor is under negative bias (Vgs = -Vdd), increasing the threshold voltage of the pMOS transistor and reducing multiplier speed. From the above literature work, it is evident that the previous techniques suffers from various problems like increase in multiplication operations, bit shift operations, percentage degradation in circuit performance lower than that of threshold voltage cannot be analyzed, does not captures the performance degradation across week inversion regions and used only for unsigned numbers. In the proposed work signed multiplication are performed and compared with conventional unsigned multipliers.

Conventional Unsigned Multiplier: A multiplier is one of the key in hardware blocks in the majority digital signal processing (DSP) systems. In parallel multipliers number of partial products to be added is the main parameter that decides the performance of the multiplier. Serial-parallel multipliers compromise speed to accomplish better performance for area and power consumption.

Array Multiplier: Array multiplier is well known due to its regular structure and is shown in Fig. 3.1. It is based on addition and shifting algorithm. The partial product is generated by the multiplication .The partial product are shifted according to their bit orders and then added. The addition can be performed with normal carry propagate adder. N-1 adders are required where N is the multiplier length.

Column By-Pass Multiplier:

- The Column by-pass multiplier is used to turn off the column whenever the multiplicand bit input is zero. This in turn reduces the power consumption in the circuit, is shown in Fig. 3.2.

Row By-Pass Multiplier: Similar to Column by-pass multiplier, Row by-pass multiplier is used to turn off the row whenever the multiplier bit input is zero. This in turn reduces the power consumption in the circuit, is shown in Fig. 3.3. The power consumption in the circuit reduces whenever the switching activity is reduced without changing the functionality of the circuit.

Unsigned Multiplier: In the conventional multiplier the multiplication of multiplier and the multiplicand is performed only for the unsigned numbers and the error signal due to timing violations are observed using the razor flip-flop.Unsigned multiplier architecture includes two m-bit inputs (m is a positive number), one 2m-bit output, one column- or row-bypassing multiplier, 2m 1-bit Razor flip-flops and it is shown in Fig. 3.4. The multiplicand and the multiplier bit from the d-flip flop are given to the multiplier block and the multiplier gives the product term. Razor flip flop is used to detect the error and it is corrected by hold logic.

Proposed Signed Multiplier: Signed number representation is necessary to encode negative numbers in binary number systems. On the other hand, in computer hardware, numbers are represented only as bit string , without extra symbols.

Modified Razor Flip Flop: Razor relies on a combination of architectural and circuit level techniques for efficient error detection and correction of delay path failures. The concept of razor is illustrated in Fig. 4.1 for a pipeline stage. Each flip-flop in the design is augmented with a so called shadow latch which is controlled by a delayed clock. . In clock cycle1, the combinational logic $L1$ meets the setup time by the rising edge of the clock and both the main flip-flop and the shadow latch will latch the correct data. In this case, the error signal at the output of the XOR gate remains low and the operation of the pipeline is unaltered. To guarantee that the shadow latch will always latch the input data correctly, the allowable operating

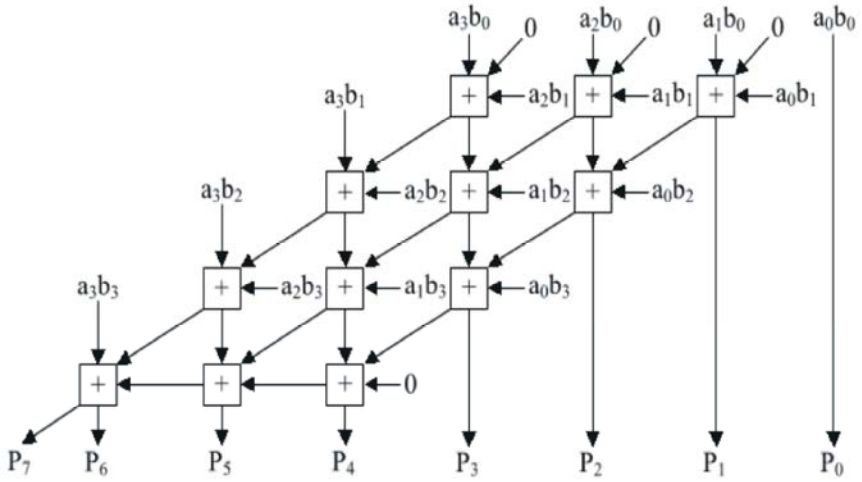

Fig. [3.1]: Array Multiplier

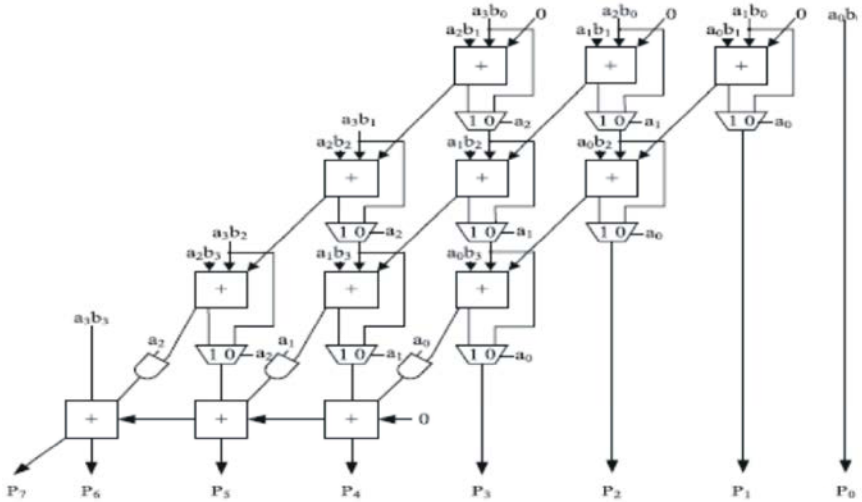

Fig. [3.2]: Column by-pass Multiplier

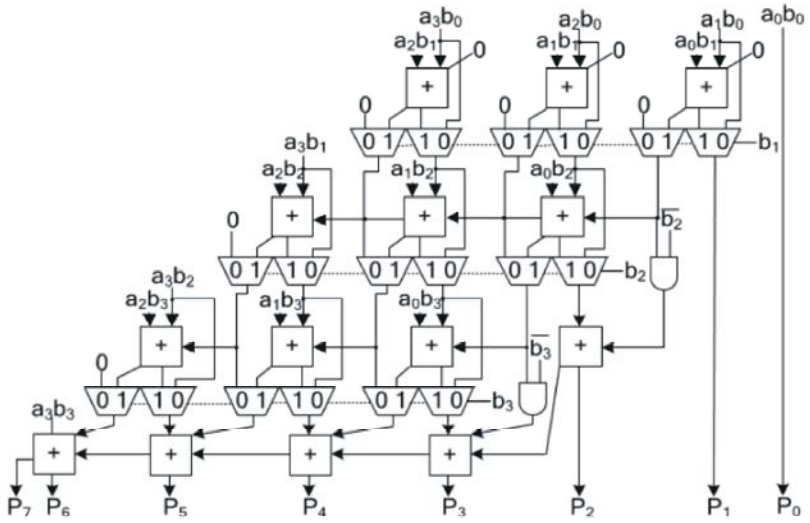

Fig. [3.3]: Row by-pass Multiplier

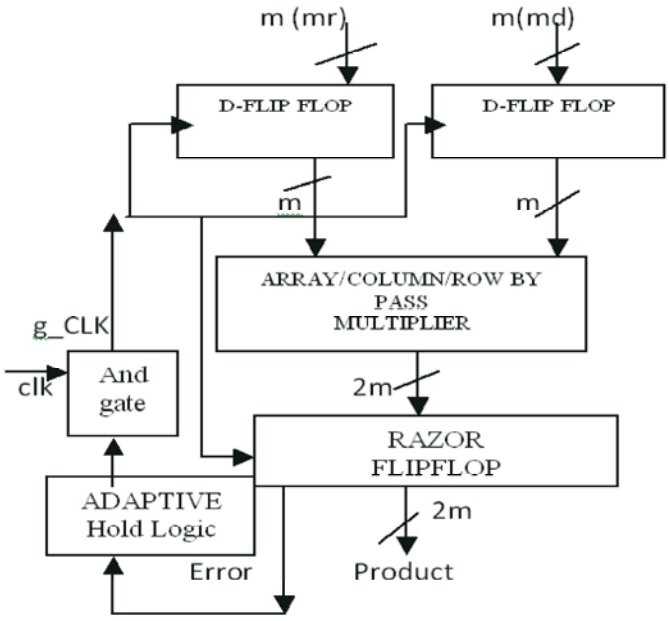

Fig. [3.4]: Unsigned Multiplier

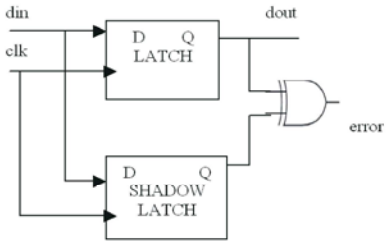

Fig. [4.1]: Modified Razor Flip Flop

voltage is constrained at design time such that under worst-case conditions, the logic delay does not exceed the setup time of the shadow latch. By comparing the valid data of the shadow latch with the data in the main flip-flop, an error signal is then generated in cycle 3 and in the subsequent cycle, cycle 4, the valid data in the shadow latch is restored into the main flip-flop and becomes available to the next pipeline stage *L*2 [15].

Two's Complement: The two's complement of a number behaves like the negative of the original number in most arithmetic and positive and negative numbers can coexist in a natural way. Its wide use in computing makes it the most important example of a radix complement. The two's complement of an *N*-bit number is defined as the complement with respect to 2^N; in other words, it is the result of subtracting the number from 2^N. This is also equivalent to taking the ones' complement and then adding one, since the sum of a number and its ones' complement is all 1 bits. In this method two's complement is performed using the T-flip flop and it is shown in Fig. 4.2. In the first step the given input bit are one's complemented using a T-flip flop and for the one's complemented input binary bit 1 is added in the LSB to convert the one's complement number into two's complement.

Proposed Multiplier Design I: In the proposed architecture both the multiplicand and the multiplier bit are signed bit and the block architecture of a signed multiplier is shown in Fig. 4.3. To perform the multiplication for multiplicand and multiplier the signed bits are converted into the two's complement form and it is given to the array multiplier, column bypass multiplier and row bypass multiplier. The product term from the multiplier are given to the razor flip-flop to detect the error.

Proposed Multiplier Design II: In the proposed architecture the multiplicand bit is unsigned and the multiplier bit is signed bit and the block architecture of a multiplier design 2 is shown in Fig. 4.4. To perform the multiplication for multiplicand and multiplier, the multiplicand is given to D-flip flop and the multiplier bit is given to Two's complement block where the signed bits are converted into the two's complement form and it is given to the array multiplier, column bypass multiplier and row bypass multiplier. The product term from the multiplier are given to the razor flip-flop to detect the error. From the above proposed method it is observed that, the block schematic is implemented for the signed

multiplicand, signed multiplier and the block schematic is implemented for the signed multiplier and unsigned multiplicand, two's complement of the signed number is carried out using T-flip-flop and the multiplication is performed using array, column bypass and row bypass multipliers.

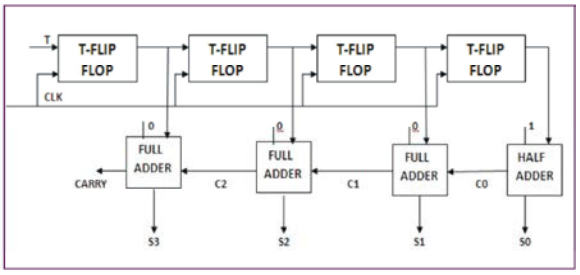

Fig. [4.2]: Two's Complement

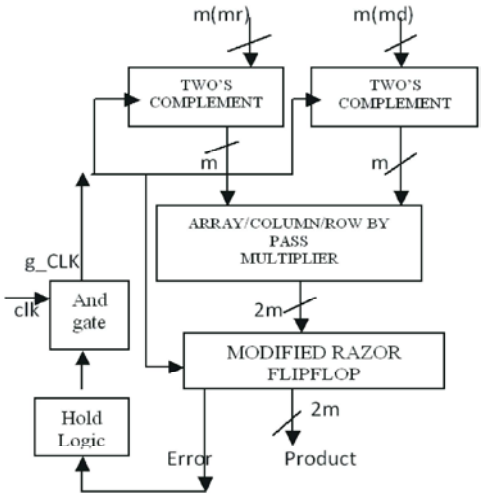

Fig. [4.3]: Proposed multiplier design

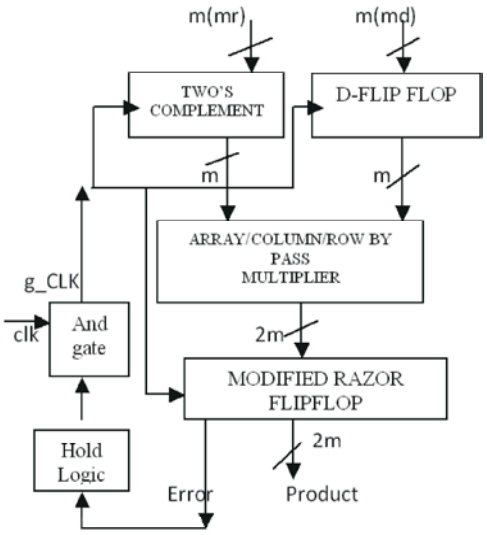

Fig. [4.4]: Proposed multiplier design II

Simulation: In this the simulation results of conventional unsigned multiplier and proposed design 1 and design 2 multipliers are discussed. The comparisons among the unsigned, design 1 and design 2 multipliers have been made. The various designs are coded in Verilog and simulation is carried out using the ISIM simulator, the synthesis is done in XILINX ISE Design Suite 13.2 and the power is analyzed using Xpower analyzer.

Simulation Results for Unsigned Multiplier: The simulation result of unsigned multiplier is shown in Fig. 5.1.

Simulation Results for Signed Multiplier Design I: The simulation result of Signed multiplier is shown in Fig. 5.2.

Simulation Results for Signed Multiplier Design II: The simulation result of design 2 array multiplier is shown in Fig. 5.3.

Figures and Tables: TABLE I shows the analysis of various parameters such as 4 Input LUT, Slice and Delay for the unsigned and signed multipliers.

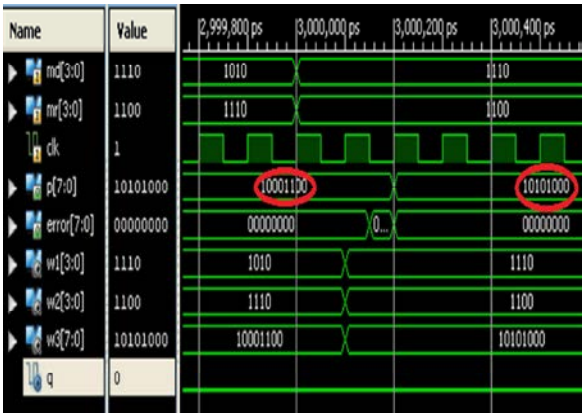

Fig. [5.1]: Simulation of unsigned multiplier

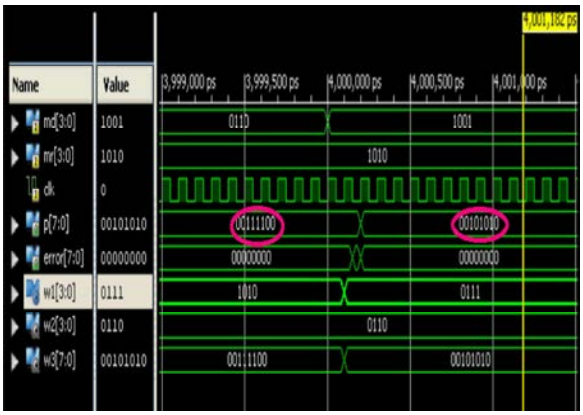

Fig. [5.2]: Simulation of Signed multiplier design I

Fig. [5.3]: Simulation of Signed multiplier design II

Table 1: Comparision of Multipliers

Method	4 Input LUT	No of Occupied Slice	IOB	Power (W)	Total Memory Usage (KB)	DELAY (ns)
	CONVENTIONAL UNSIGNED MULTIPLIER					
ARRAY MULTIPLIER	36	31	36	0.081	138096	7.183
COLUMN BYPASS	36	31	36	0.081	138096	7.183
ROW BYPASS	48	37	25	0.081	138096	8.368
	PROPOSED MULTIPLIER DESIGN 1					
ARRAY MULTIPLIER	42	34	25	0.052	137072	8.602
COLUMN BYPASS	43	34	25	0.052	137072	8.118
ROW BYPASS	62	44	25	0.052	137072	9.996
	PROPOSED MULTIPLIER DESIGN 2					
ARRAY MULTIPLIER	42	34	25	0.081	137700	8.440
COLUMN BYPASS	40	33	25	0.081	137700	8.297
ROW BYPASS	61	44	25	0.081	137700	9.921

From the table various multipliers are compared in terms of IOB, Memory usage, power and delay and it is noticed that the proposed architecture occupies lesser number of IOB and memory usage. The power consumed by the proposed architecture is less. Hence it is concluded that the proposed Design 1 and Design 2 signed multipliers are efficient compared to conventional unsigned multipliers.

CONCLUSION

In this project:

- Both multiplicand, multiplier as a signed bit (Design 1)
- Multiplicand as unsigned bit, multiplier bit as signed bit (Design 2) is implemented using array, column by pass and row bypass multipliers and razor flip-flops is used to detect whether timing violations occur before the next input pattern arrives and checks for any path delay timing violations. The experimental results shows that the proposed architecture with 4x4 Design 1 signed multipliers uses 25 IOB and 137072KB of memory and the proposed architecture with 4x4 Design 2 multipliers uses 25 IOB and 137700KB of memory which is lesser than the conventional unsigned multiplier. In addition, the power consumed by Design 1 signed multiplier is 0.052W and for Design 2 multiplier the power consumed is 0.081W which is less when compared with Conventional unsigned multiplier.

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