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A Systematic Approach to 60GHZ Cmos Low Noise Amplifier Design for Low Power Transmission

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Abstract: Recent interest in the 60GHz band for high-density and short range wireless links has led to significant progress in the development of integrated circuits for low-cost millimetre wave radio systems. The low noise amplifier (LNA) serves as the first component in the radio frequency (RF) transceiver system. The performance of LNA determines the sensitivity and selectivity of the system. In order to maximize performance gain, noise figure(NF) and input matching of LNA need to be optimized. We have designed a LNA for 60GHz in this paper. The main topology used in our design is cascode with a middle inductor. The design is laid out on 130nm standard CMOS technology designed using classical noise matching techniques. Simulated results show that the reflection coefficient for the designed LNA is -10dB with the gain of 31.5dB and noise figure of 1.9dB.

Key words: LNA · CMOS · CASCODE topology · CS configuration · 60GHz.

INTRODUCTION

Recent interest in the 60-GHz band for high-density, short-range wireless links has led to significant progress in the development of integrated circuits for low-cost mm-wave radio systems [1, 2].

57-64GHz is an unlicensed frequency band [3, 4]. It can be used for short range gigabit wireless communication systems [5]. The main function of an LNA is to amplify extremely low signals and is used at both the transmitter and the receiver side without adding noise, thus preserving and maintaining the required signal to noise ratio (SNR) of the system and operates at extremely low power levels. Also for large signal levels the LNA eliminates channel interference by amplifying the received signal without introducing any distortions.

Obtaining high gain with considerable noise figure along with proper input and output matching is a challenging work while designing an LNA.

Class A amplifier has bias point more or less at the centre of maximum voltage and current capability of the device used. So basically the LNA always operates in the same region as that of the class a amplifier mostly at 15-20% of its maximum useful current.

Carefully selecting the transistor and having proper understanding about various parameters and their respective trade-offs can help us meet most conditions met without using feedback arrangements. Proper Transistor selection is the first and most important step in an LNA design.

Millimetre wave radio frequency transistors have traditionally been the domain of III-V compounded semiconductors such as GaAs and InP, an increasing number of 60-GHz blocks and systems have been recently reported in advanced SiGeBi-CMOS and CMOS technologies to meet the cost, size and power consumption needs of the consumer[6,7]. The transistor needs to exhibit proper S parameters and have a low noise figure and good performance with lowest possible current consumption and preserving the matching of the design at the same time along with proper linearity. The cascode topology have been implemented which provides better isolation, improved bandwidth, higher gain even at millimetre wave frequencies.

In this paper, we design a LNA for 60GHz which is based on cascade topology with a middle inductor. The remaining paper is organized as follows: section 2 focuses on the CMOS LNA topology that has been used in this paper. The design methodology for the mm-wave CMOS LNA is presented in section 3. Section 4 shows the schematic of the LNA and Section 5 shows the simulation results. Conclusion is presented in section 6.

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Cmos Lna Topology: CMOS technology have low current drive and power dissipation when compared to any other technologies like BJTs, HEMTs and any other semiconductor group technologies. Using BJT is one of the most famous ways of designing an LNA, HEMTs came into the role for high frequency systems or block design. Here we are using CMOS in our design. Common-Gate and Cascode amplifier is the two common ways of designing an LNA for CMOS technology. The Common-Gate stage provides a wide-band input matching and also has a high noise figure [8,9].

The main topology used in our design is cascode with a middle inductor. This is also called as source degenerative cascoded topology.

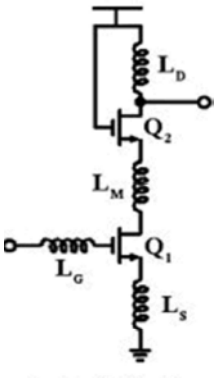

Fig. 1: Cascode with middle inductor

The cascode topology provides better isolation, improved bandwidth and higher gain even at millimetre wave frequencies. For the tuning out of the middle pole of cascode a series inductor is always placed between the common source and common drain. For any LNA design we prefer to have higher value of f_t, so an optimal value of the middle inductor has to be chosen by simulating f_t and noise figure for the whole cascode with inductive broad banding, as a function of L_M.

Although the cascode topology has higher gain, larger output impedance and flat IDS-VDS characteristic, the single-transistor CS configuration is advantageous in terms of the lower supply voltage required, leading to higher efficiency and good linearity. [10]

Here in the given design of the LNA consists of both cascode topology and the single-transistor CS configuration techniques. This leads to the better performance of the system.

Design Procedure: Using the above mentioned topology and techniques, a three stage LNA is designed with CMOS transistors. Firstly a paper pencil design is made using the transistor considerations and then simulating using ADS. The design steps are follows[11]:

Step 1: Consider a bias current for the required application. For the present system design I_{bias} = 13mA.

Step 2: The transconductance of the system should be selected in such a way that it prevents the inversion of the transistor. The transistor inversion plays an important role at high frequencies like 60GHz. The relationship between I_{bias} and transconductance (g_m) can be established as follows $g_m = K*I_{bias}$ where K is an integer. This conditions help in maintaining the weak inversion where 'K' can range from 10 to 25.

Step 3: The saturation voltage of the transistor is determined by the width and length of the transistor along with the transconductance parameter. The saturation voltage of the transistor plays the critical role in maintaining the linearity. This voltage varies according to the frequency of operation. The width and length of transistor can be calculated by

$$\frac{W}{L} = \sqrt{\frac{2 \times I_{bias}}{K' \times V_{sat}^{\ 2}}} \quad (1)$$

$$V_{sat} = \sqrt{\frac{2 \times I_{bias}}{K' \times \left(\frac{W}{L}\right)}} \quad (2)$$

Step 4: A bypass capacitor should be placed between the gate and source which helps in matching of the input.

The capacitor can be selected with the help of oxide density of the transistor. This helps in better performance of the transistor and its matching with external component.

$$C = \frac{2}{3} \times \text{Oxide density} \times W \times L$$

Step 5: To provide matching at the input with 50? input matching. An external inductor value is determined using the matching technique.

$$g_m \times \frac{L_s}{C} = \text{matching impedance} \quad (5)$$

Step 6: To provide the matching at the output and L and C is tuned to the output matching impedance.

Step 7: In order to provide inter stage matching for consecutive stages, we need match the L and C values according to the matched impedance.

Step 8: Using the tuning technique for 60GHz frequency the second, third and further stages is developed with common source configuration.

Circuit Design: The complete design of the 3stage LNA with source degenerative inductive and common source topologies is shown.

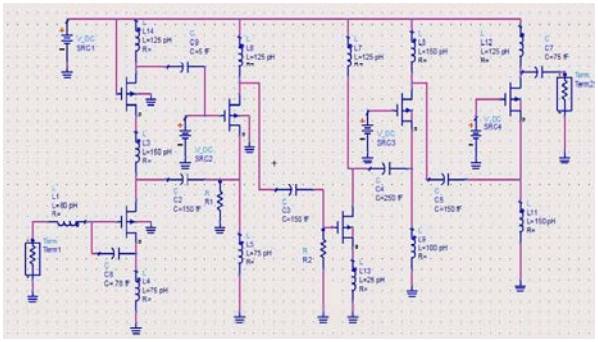

Fig. 2: Schematic of proposed LNA design

Simulation Results: The above circuit is simulated using ADS and the output of the circuit is measured using the parameters reflection coefficient, gain and minimum noise figure.

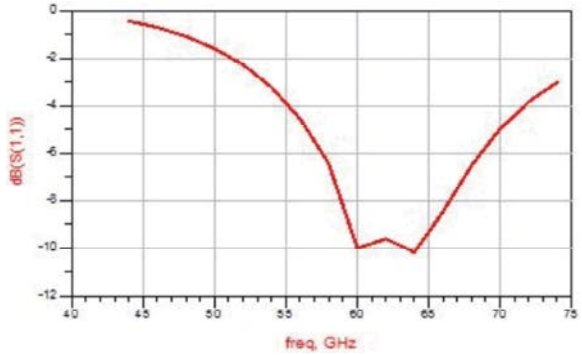

Fig. 3: Illustrates S_{11} at 60GHz.

Figure 3 shows the obtained graph for S_{11} vs frequency where the obtained S_{11} is -10dB. Fig.4 which shows the plot for Noise Figure vs frequency where the Noise Figure obtained is 1.9dB which is followed by Fig.5 shows the graph for gain vs frequency where the obtained gain is 31.5dB.

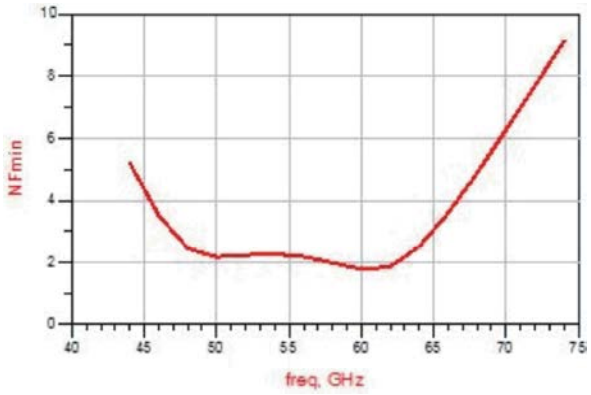

Fig. 4: Illustrates noise figure at 60GHz.

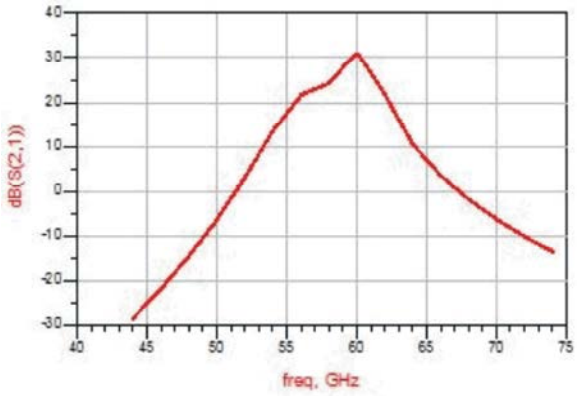

Fig. 5: Illustrates gain at 60GHz.

CONCLUSION

From the designed LNA we observe that a good trade-off is maintained between noise figure and gain with minimum reflected signal at the input. Using CMOS sufficiently low noise figure and good linearity is maintained throughout the system and also sufficient gain is obtained by maintaining the low power. The reflection coefficient for the designed LNA is -10dB with the gain of 31.5dB and noise figure of 1.9dB.

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