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Leakage Power Analysis of Dynamic Footed Circuits in 45nm CMOS Technologies

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Abstract: In this paper, two new circuits are proposed and compared to the existing techniques for the leakage power reduction of footed domino logic circuits. First proposed circuit employed one extra high-V_t pMOS transistor between power supply and footer node. Second proposed circuit employed sleep transistors. Proposed circuits reduce both subthreshold and gate oxide leakage currents. Simulation is done using 45nm HSPICE for OR2, OR4, OR8 and2 and AND4 gates at operating temperatures 25°C and 110°C. The first proposed circuit technique lowers the total leakage power by 54% to 96% as compared to standard low-V_t circuits and 10% to 85% as compared to standard dual-V_t circuits. Similarly, second proposed circuit lowers the total leakage power by 79% to 96% as compared to standard low-V_t circuits and 54% to 90% as compared to dual-V_t circuits.

Key words: Dual-V_t · Footed Domino logic · Gate Oxide Leakage Current · Standby mode and Subthreshold Leakage Current

INTRODUCTION

Domino logic circuit has two sub categories, footed domino circuit and footless domino logic. Footed domino circuit consists of precharge transistor, footer transistor, pull down network (PDN) and keeper transistor [1]. Footer transistor isolated the pull down network during the precharge phase. Omitting the footer transistor, it turns to footless domino circuit [2]. Footless domino circuit reduces evaluation delay and power consumption as compared to the footed domino circuit. Both footed and footless domino circuit are used in high performance microprocessor. In cascading of domino circuits, first stage of the circuit is footed and rest of the stage is footless domino circuit.

Domino logic is used in high performance digital circuits such as logic gates, microprocessor, adder etc. due to the superior speed and low area required as compared to static CMOS circuits. Domino logic is more prone to input noises and it has low noise margin as compared to static CMOS gates. Scaling of CMOS technology reduces the power supply and transistor sizes. Dynamic power consumption is directly proportional to the power supply and its value decreases at the cost of speed. To enhance the speed, threshold voltage of the transistor is reduced [14, 15]. This lowering of threshold voltage leads to an exponential increases in subthreshold leakage current. Several circuit techniques are implemented to reduce the subthreshold leakage current and gate oxide leakage current is neglected [3-5].

In dual-V_t technique, high-V_t transistors are placed in the precharge path and low-V_t transistors are placed in the evaluation path [6-8]. High clock and high inputs (CHIH state) discharged the dynamic node, low dynamic node cuts off all the high-V_t transistors and it reduces the subthreshold leakage current. High clock and low inputs (CHIL state), dynamic node maintains high voltage, all low-V_t transistors are cuts off and subthreshold leakage current increases. CHIH state produces large gate oxide leakage current through pull down network for both footed and footless dominos. To tackle both subthreshold and gate oxide leakage current, sleep switch technique is more efficient [9-12]. This technique discharged the dynamic node through sleep switch and places the circuit into low leakage state.

In this paper, we proposed two circuits to reduce simultaneously both subthreshold and gate oxide leakage current of the footed domino. First proposed circuit employed high-V_t pMOS transistor between the power supply and footer node. Second proposed circuit employed sleep switch transistors to place the circuit into low leakage state. The remainder of this paper is organized as follows. Section 2 presents the leakage current characteristics of single transistor. Leakage current

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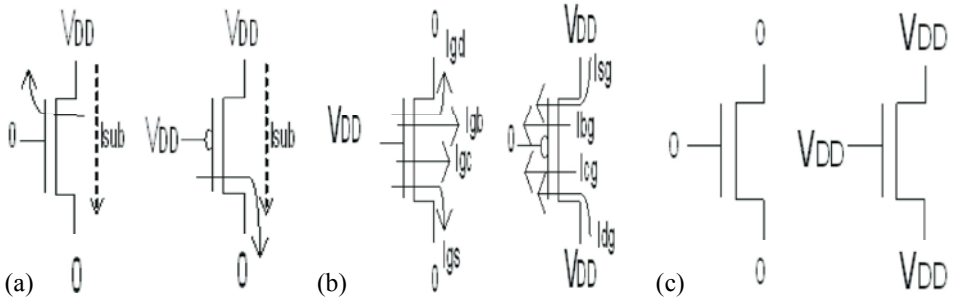

Fig. 1: (a) Maximum subthreshold leakage current state. (b) Maximum gate oxide leakage current state. (c) Condition to avoid both subthreshold and gate oxide leakage current.

characteristics of footed domino circuit are presented in Section 3.Section 4 introduces two new proposed circuits for minimizing the total leakage currents. In section 5, we present simulation results and Section 6 concludes this paper.

Leakage Current Characteristics of Single Transistor: The subthreshold and gate oxide leakage currents are shown in Fig. 1. Subthreshold leakage current is maximum when transistor is in cuts off mode and voltage difference between drain-to-source is maximum and it has reverse edge gate oxide leakage current as shown in Fig 1 (a). Gate oxide leakage current has four components: gate-to-channel (Igc), gate-to-drain (Igd), gate-to-source (Igs) and gate-to- body (Igb). Igb is several orders smaller as compared to all three components and it is neglected, Igc is shared between drain and source as shown in Fig 1. (b). Gate oxide leakage current is maximum, when transistor is in active mode and the voltage difference between the gate to source and gate to drain are maximum. To avoids both subthreshold and gate oxide leakage current, all terminal of transistor must have same potential as shown in Fig.1(c).

The width and length of both nMOS and pMOS transistor are set to be 1ìm and.045um respectively. Gate oxide leakage of nMOS transistor is dominant over pMOS transistor because tunneling probability of electron is greater than tunneling probability of hole as shown in Fig 2. The gate oxide leakage current produced by an nMOS transistor is 9.9x to 40.1x times higher than the gate oxide leakage current of a pMOS transistor depending on the voltage difference across the gate oxide [11,12].

Variation of subthreshold and gate oxide leakage current of an nMOS with supply voltage at two different temperature is shown in Fig 3. At 110°C, the subthreshold leakage current is 6.7 times higher than the gate oxide leakage current at 0.8 V supply voltage [12].

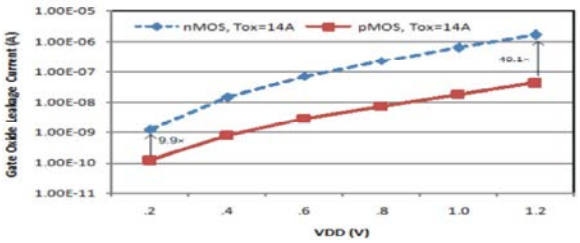

Fig. 2: Comparison of gate oxide leakage current for an nMOS and pMOS [12].

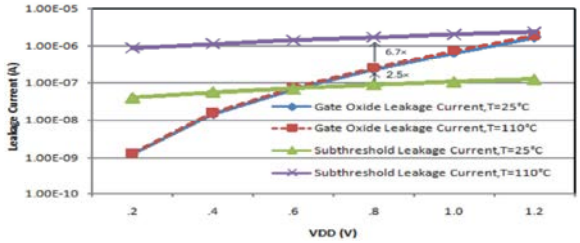

Fig. 3: Comparison of subthreshold and gate oxide leakage currentof an nMOS at two different temperatures [12].

Similarly, at the room temperature, the gate oxide leakage current is 2.5 times higher than subthreshold leakage current at 0.8V.

Comparison of normalized subthreshold leakage current and gate oxide leakage current produced by low-V_t transistor and high V_t transistor in dual V_t CMOS technology is shown in Table I [12]. Here we have taken transistor width=1µm, transistor length=45nm, Low-V_t=0.22V for nMOS pMOS having T_{OX}=14Å, High-V_t=0.466V having T_{OX}=17.5Å for nMOS and High-V_t=-0.4118V having T_{ox}=18.5Å for pMOS, V_{DD}=0.8V. For each temperature, the currents are normalized to the subthreshold leakage current produced by the high-V_t pMOS transistor. The gate oxide leakage current of a low-V_t nMOS transistor is 3.30 times and 9.4 times higher

Table 1: Normalized subthreshold and gate oxide leakage currents of the Low-V_t and High-V_t transistors at two different temperatures [12].

	nMOS		pMOS	
	Low-V_t	High-V_t	Low-V_t	High-V_t
I_{sub} (110°C)	22.3	2.6	16.01	1.0
I_{gate} (110°C	3.3	0.05	0.097	0.0003
I_{sub} (25°C)	3.7	1.9	3.1	1.0
I_{gate} (25°C)	9.4	0.15	0.31	0.001

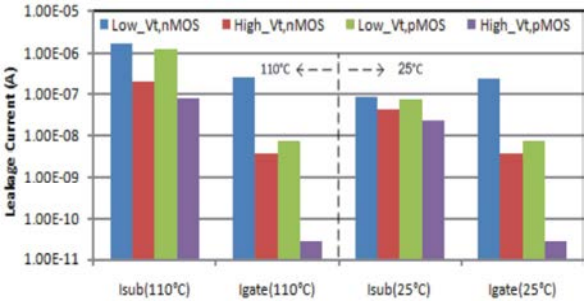

Fig. 4: Comparison of subthreshold and gate oxide leakage current of low-Vt and high-Vt transistors at two different temperatures.

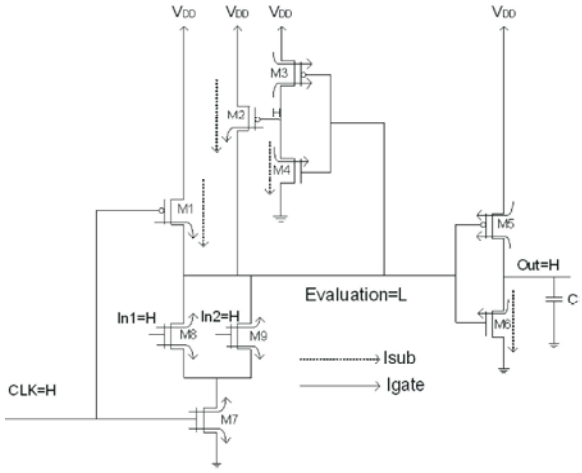

Fig. 5: Variation of subthreshold and gate oxide leakage current conduction path in standard low-Vt footed domino OR2 circuit with CHIH state.

than the subthreshold leakage current of a high-V_t pMOS transistor at the high and low temperatures, respectively. The gate oxide leakage current produced by a low-V_t nMOS transistor is 34 times and 30 times higher than the gate oxide leakage current produced by a low-V_t pMOS transistor at 110°C and 25°C. The gate oxide leakage current for pMOS device is lower as compared to an nMOS device with the same width and length with different T_{ox} and the same voltage difference across the gate insulator.

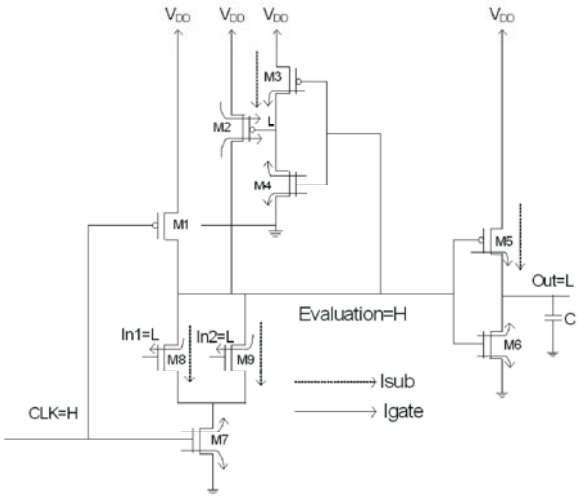

Fig . 6: Variation of subthreshold and gate oxide leakage current conduction path in standard low-Vt footed domino OR2 circuit with CHIL state.

Fig.4 shows that subthreshold leakage current produced by the low-V_t transistors is the highest source of leakage current in sub-45nm technologies at high temperature (110°C). At room temperature (25°C), gate oxide leakage current produced by the low-V_t nMOS is the dominant source of the leakage current. At room temperature, gate oxide leakage current is bigger contributor and it has weak dependence on temperature. Subthreshold leakage current increases exponentially with temperature and it is dominant for high temperature. Relative contribution of gate oxide and subthreshold leakage currents is also dependent on fan-in, structure of the PDN and inputs of the fan-in of domino circuits.

Leakage Current Characteristics of Footed Domino Circuit: In this section, leakage current characteristics of the footed domino circuit is analyzed in standby mode, clock is gated high. Depending on the inputs, there are two states, inputs are high (CHIH) and inputs are low (CHIL).

Standard Low-V_t Domino Circuit: Variation of subthreshold and gate oxide leakage current with low dynamic node voltage and high dynamic node of standard low-V_t OR2 domino footed circuit is shown in Fig.5 and Fig. 6. All transistors of the circuits are low-V_t [13]. Total leakage current of the domino circuit is expressed as

$$I_{leakage} = I_{sub} + I_{gate} \quad (1)$$

In CHIH state, leakage currents are modeled as

$$I_{sub} = (W_{M1} + W_{M2})\, J_{SLP} + (W_{M4} + W_{M6})\, J_{SLN} \quad (2)$$

$$I_{gate} = W_{PDN}.\, J_{GFLN}\, (W_{M4} + W_{M6})\, J_{GRLN} + (W_{M1} + W_{M2})\, J_{GFLP} + (W_{M3} + W_{M5}).\, J_{GRLP} + W_{7}.\, J_{GFLN} \quad (3)$$

In CHIL state, leakage currents are modeled as

$$I_{Sub} = W_{PDN}.\, J_{GFLN}\, (W_{M3} + W_{M5})\, J_{GRLN} + (W_{M3} + W_{M5})\, J_{GFLP}$$
$$I_{gate} = W_{PDN}.\, J_{GFLN}\, (W_{M4} + W_{M6} + W_{M7})\, J_{GRLN} + (W_{M3} + W_{M5})\, J_{GFLP} + W_{M2}.\, J_{GRLP} \quad (4)$$

Where J_{SLN}, J_{SLP}, J_{GFLN}, J_{GRLN}, J_{GFLNP} and J_{GRLP} are subthreshold leakage current per width unit of low-V_t nMOS and pMOS, forward and reverse gate oxide leakage current density per width unit of low-V_t nMOS and pMOS. Comparison of subthreshold leakage current and gate oxide leakage current in CHIH and CHIL states is given as

$$I_{SUB,CHIL} > I_{SUB,CHIH} \quad (5)$$

$$I_{GATE,CHIH} > I_{GATE,CHIl} \quad (6)$$

Gate oxide leakage current is dominant over subthreshold leakage current in CHIH state. Similarly, subthreshold leakage current is dominant gate oxide leakage current in CHIL state.

Standard Dual-V_t Footed Domino Circuit: Variation of subthreshold and gate oxide leakage current with low dynamic node voltage and high dynamic node of standard low-V_t OR2 footed domino circuit as shown in Fig.7 and Fig. 8. The critical signal transition that determines the speed of a domino circuit occurs along the evaluation path. In a dual threshold voltage (dual-V_t), all of the transistors that are activated during precharge phase have high-V_t and rest of transistors are low- V_t. Transistors M1, M2, M4 and M6 are high-V_t devices [2, 3, 6-8].

In CHIH state, dynamic node is discharged to low voltage through pull down network and footer transistor M7 and output node charged to high voltage. Low dynamic node voltage cuts off all the high-V_t transistors, reduces the subthreshold leakage current of the circuit. All low-V_t transistors are turned ON, it increases the gate oxide leakage current of the circuit.

In CHIL state, dynamic node remains high voltage and output node discharges to low voltage. High dynamic node voltage cuts off all the low-V_t transistors except

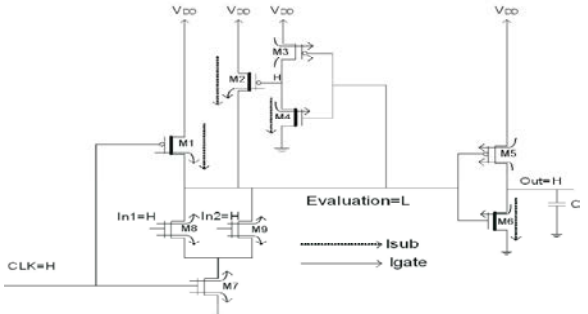

Fig. 7: Variation of subthreshold and gate oxide leakage current conduction path in standard dual-Vt footed domino OR2 circuit with CHIH state

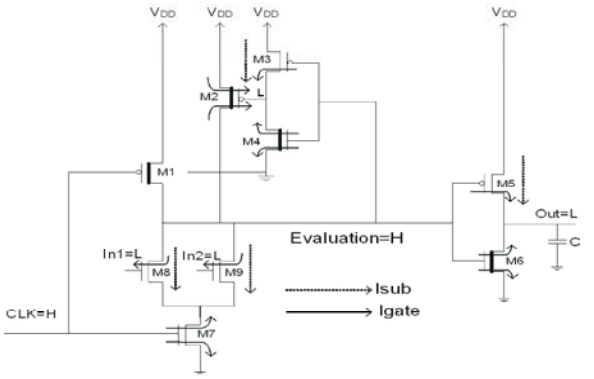

Fig. 8: Variation of subthreshold and gate oxide leakage current conduction path in standard dual-Vt footed domino OR2 circuit with CHIL state.

footer transistor, increases subthreshold leakage current and reduces gate oxide leakage current due to high-V_t transistors.

Proposed circuits: The proposed circuits simultaneously reduce both subthreshold and gate oxide leakage currents.

Proposed Circuit1: A high-V_t pMOS pull-up feedback transistor M8 is employed between the power supply and footer node (X) and its gate is connected to the dynamic node as shown in Fig.9. Keeper gate is directly connected to the output of the domino circuit. Removing the inverter between keeper and dynamic node reduces both leakage current and area. In the standby mode, clock is gated high, turning off the high-V_t pull-up transistor M1.When all the inputs are low (CHIL), all the transistors of the pull down network are turned off, dynamic node is maintained high and output node of the circuit is low. High dynamic node turns off transistor (M8), creates a small voltage at node (X) nearly to $|V_{tp}|$ of high-V_t pMOS transistor.

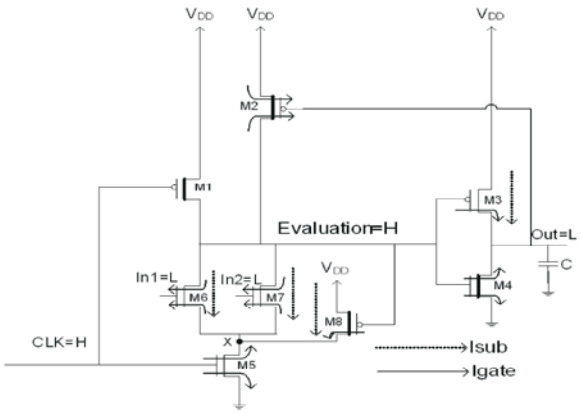

Fig. 9: Variation of subthreshold and gate oxide leakage current conduction path in proposed circuit 1.

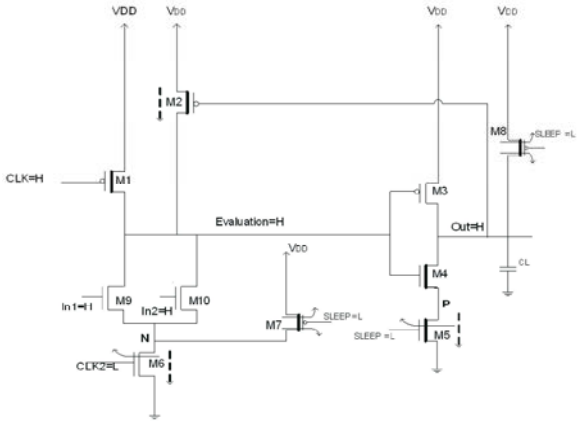

Fig. 10: Variation of subthreshold and gate oxide leakage current conduction path in proposed circuit 2.

There is exponential reduction in the leakage current due to negative bulk to source voltage of the pull down network and increase in the threshold voltage of the pull down network. There is also exponential decrease in the subthreshold leakage current due to reduction of gate-to-source voltage.

Leakage currents of the circuit are modeled as

$$I_{Sub} = W_{PDN}.\, J_{SPDN} + W_{M8}.\, J_{SHP} + W_{M3}.\, J_{SLP} \quad (7)$$

$$I_{gate} = W_{PDN}.\, J_{GTLN} + W_{M4}.\, J_{GFHN} + W_{M5}.\, J_{GFHP} + W_{M8}.\, J_{GFHP} + W_{M3}.\, J_{GFHP} + W_{M2}.\, J_{GFHP} \quad (8)$$

Where J_{SLP}, J_{SHP}, J_{GFLN}, J_{GFHN}, J_{GFLP}, J_{GFHP} and J_{GRLP} are subthreshold leakage current per width unit of low-V_t and high-V_t of pMOS, forward and reverse gate oxide leakage current density per width unit of low-V_t and high-V_t of nMOS and pMOS.

Proposed circuit 2: Three high-V_t sleep switch transistors M5, M7 and M8 are added to the standard dual-V_t footed domino gate to force the dynamic and output node into high voltage as shown in Fig.10. By adding the high-V_t transistor M5 in series with M4, speed of the circuit reduces. In active mode, sleep signal is set high and CLK2 is similar to CLK, sleep transistors M7 and M8 are cut-off and transistor M5 is ON. The proposed circuit works like standard dual-V_t footed domino gate.

In standby mode, CLK is gated high and CLK2 is gated low, M1 and M6 are cuts off. Sleep signal is set low voltage, sleep transistors M7 and M8 are turned ON and transistor M5 OFF. Sleep transistor M8 provides high voltage at output node. A high-V_t nMOS sleep transistor M5 is employed in series with M4 in order to eliminate the static DC current path through M8 and M4. A high-V_t pMOS sleep transistor M7 is employed between power supply and footer node N. When all inputs are high (CHIH state), dynamic node is remains high. Sleep transistor M7 provides high voltage at footer node N and its avoids both subthreshold and gate oxide leakage current in the pull down network. Gate oxide leakage current of transistor M1, M2, M3 and M4 are neglected because all terminals of these transistors have same potential.

Leakage currents of the circuit are modeled as

$$I_{sub} = W_{M2}.\, J_{shp} + W_{M5}.\, J_{SHN} + W_{M6}.\, J_{SLN} \quad (9)$$

$$I_{gate} = W_{m5}.\, J_{GRHN} + W_{M6}.\, J_{GRLN} + (W_{M7} + W_{M8}).\, J_{GRHP} \quad (10)$$

Where, J_{SLN}, J_{SHN}, J_{SHP}, $J_{GRLN,}$ J_{GRHN} and J_{GRHP}, are subthreshold leakage current per width unit of low-V_t and high-V_t of pMOS, forward and reverse gate oxide leakage current density per width unit of low-V_t and high-V_t of nMOS and pMOS.

Simulation Results: In this section, we presented simulation results of existing circuits and propose circuits.BSIM4 device models are used. The 2-input and 4-input footless domino AND gates (AND2 and AND4), 2-input, 4-input and 8-input footless domino OR gates and proposed circuit are simulated in a 45nm CMOS technology. The device parameters are (V_{tnlow}=|V_{tplow}|=.22V, V_{tnhigh}=.466V, V_{tphigh}=-.4118 V) and power supply is 0.8V [16]. The leakage power consumption is measured at 25°and 110°C respectively. Active mode power consumption is measured at 110°C. A 1GHz clock is applied to the circuits with load capacitance 1fF.To have reasonable comparison, all circuits have similar size.

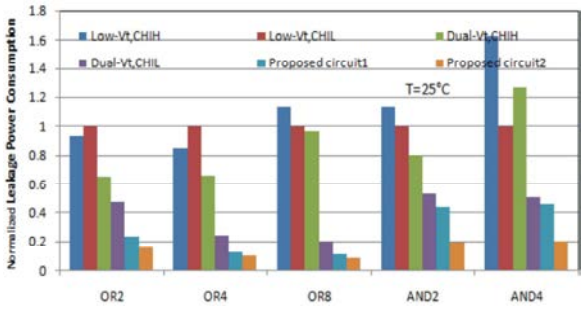

Fig. 11: Comparision of the leakage power consumption of the proposed circuits and the existing techniques. The leakage power consumption is normalized to the leakage power of the standard low-Vt technique with low inputs for each circuit.

Leakage Power Consumption at 25°C: At low temperature, gate oxide leakage is the highest source of leakage current and dominant over subthreshold leakage current. Variation of the total leakage power consumption of the standard low-V_t CHIH footed domino circuit, standard low-V_t CHIL footed domino circuit, standard dual-V_tCHIH footed domino circuit, standard dual-V_t CHIL footed domino circuit, proposed circuit1 and proposed circuit2 are shown in Fig.11. From the figure it is clear that standard dual-V_t technique reduces the leakage power consumption as compared to the standard low-V_t technique. In dual-V_t CHIH state, pull down network produced maximum forward gate oxide leakage current. In dual-V_t CHIL state, pull down network produced low reverse edge gate oxide leakage current. For low temperature, dual-V_t CHIL state is preferable for reducing gate oxide leakage current.

Table 2 shows total leakage power reduction by proposed circuit1 as compared to standard circuits in standby mode. The proposed circuit1 reduces the total leakage power consumption by 61% to 90% as compared to high inputs standard low-V_t circuits and 54% to 88% as compared to low inputs standard low-V_t circuits. Similarly, it reduces the leakage power by 44% to 85% as compared to high inputs standard dual-V_t circuits and 10% to 50% as compared to low inputs standard dual-V_t circuits.

Table 3 shows total leakage power reduction by proposed circuit2 as compared to standard circuits and proposed circuit1 in standby mode. The proposed circuit2 reduces the total leakage power consumption by 82% to 91% as compared to high inputs standard low-V_t circuits and 79% to 90% as compared to low inputs standard low-V_t circuits. Similarly, it reduces the leakage power by 75% to 90% as compared to high inputs standard dual-V_t circuits and 54% to 66% as compared to low inputs standard dual-V_t circuits. Proposed circuit2 reduces leakage power by 19% to 55% as compared to proposed circuit1.

Table 2: Total leakage power reduction provided by the proposed circuit1 as compared to the existing circuit technique at 25°C.

	OR2	OR4	OR8	AND2	AND4
Low-VT,CHIH	74.95%	84.1%	90.01%	61.3%	72.07%
Low-VT,CHIL	82.19%	86.47%	88.58%	55.57%	54.43%
Dual-VT,CHIH	64.32%	79.72%	85.27%	44.85%	64.28%
Dual-VT,CHIL	50.63%	44.79%	43.36%	15.91%	10.41%

Table 3: Total leakage power reduction provided by the proposed circuit2 as compared to the existing circuit technique and proposed circuit1 at 25°C.

	OR2	OR4	OR8	AND2	AND4
Low-VT,CHIH	82.82%	87.54%	91.95%	82.84%	87.21%
Low-VT,CHIL	83.98%	89.4%	90.81%	80.29%	79.15%
Dual-VT,CHIH	75.54%	84.11%	90.49%	75.54%	83.65%
Dual-VT,CHIL	66.15%	56.76%	54.4%	62.7%	59.08%
Proposed circuit1	31.44%	21.67%	19.48%	55.65%	54.23%

Leakage Power Consumption at 110°C: At high temperature, subthreshold leakage current is the highest source of leakage current and dominant over gate oxide leakage current. Variation of the total leakage power consumption of the standard low-V_tCHIH footed domino circuit, standard low-Vt CHIL footed domino circuit, standard dual-V_t CHIH footed domino circuit, standard dual-V_t CHIL footed domino circuit, proposed circuit1 and proposed circuit2 as shown in Fig.12. From the figure it is clear that standard dual-V_t technique reduces leakage power consumption as compared to standard low-V_t technique. Dual-V_t CMOS technology is more effective for reducing subthreshold leakage current. In dual-V_t CHIH state, all high-V_t transistors of the circuit are cut off, which reduces the subthreshold leakage current at the cost of high gate oxide leakage current. In dual-V_t CHIL state, all low-V_t transistors of the circuit are cut off, which produces maximum subthreshold leakage current with minimum gate oxide leakage current. For high temperature, dual-V_t CHIH state is preferable for reducing subthreshold leakage current.

Table 4 shows total leakage power reduction by proposed circuit1 as compared to standard circuits in standby mode. The proposed circuit1 reduces the total leakage power consumption by 88% to 95% as compared to high inputs standard low-V_t circuits, 83% to 96% as compared to low inputs standard low-V_t circuits. Similarly, it reduces the leakage power by 42% to 84% as compared to high inputs standard dual-V_t circuits and 22% to 55% as compared to low inputs standard dual-V_t circuits.

Table 4: Total leakage power reduction provided by the proposed circuit1 as compared to the existing circuit technique at 110°C.

Circuit	OR2	OR4	OR8	AND2	AND4
Low-VT,CHIH	93.47%	93.95%	95.55%	88.81%	93.23%
Low-VT,CHIL	95.28%	96.21%	94.49%	83.29%	89.58%
Dual-VT,CHIH	66.87%	76.14%	84.7%	42.32%	83.06%
Dual-VT,CHIL	50.57%	49.94%	49.75%	22.97%	55.59%

Table 5: Total leakage power reduction provided by the proposed circuit2 as compared to the existing circuit technique and proposed circuit1 at 110°C.

Circuit	OR2	OR4	OR8	AND2	AND4
Low-VT,CHIH	94.72%	95.1%	95.36%	94.76%	94.75%
Low-VT,CHIL	96.19%	96.93%	95.31%	92.17%	91.91%
Dual-VT,CHIH	73.24%	80.68%	86.98%	72.99%	86.85%
Dual-VT,CHIL	60.08%	59.46%	57.23%	63.93%	65.53%
Proposed circuit1	19.23%	19.01%	14.88%	53.16%	22.4%

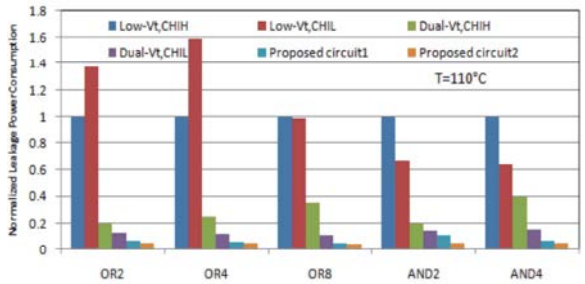

Fig. 12: Comparison of the leakage power consumption of the proposed circuits and the existing techniques. The leakage power consumption is normalized to the leakage power of the standard low-Vt technique with high inputs for each circuit.

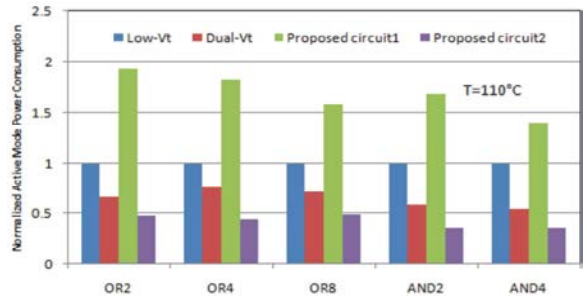

Fig. 13: Comparison of the active mode power consumption of the proposed circuits and the existing techniques. The active mode power consumption is normalized to the power consumption of the standard low-Vt technique for each circuit.

Table 5 shows total leakage power reduction by proposed circuit2 as compared to standard circuits and proposed circui1 in standby mode. The proposed circuit2 reduces the total leakage power consumption by 94% to 95% as compared to high inputs standard low-V_t circuits and 91% to 96% as compared to low inputs standard low-V_t circuits. Similarly, it reduces the leakage power by 72% to 86% as compared to high inputs standard dual-V_t circuits and 57% to 65% as compared to low inputs standard dual-V_t circuits. Proposed circuit2 reduces leakage power by 14% to 53% as compared to proposed circuit1.

Active Mode Power Consumption: Variation of the active mode power consumption of proposed circuits and standard circuits at 110°C is shown in Fig.13. From figure it is clear that standard dual-V_t footed domino circuits consume low active power as compared to standard low-V_t footed domino circuits.

Proposed circuit1 consumes more active mode power as compared to the standard circuits. It increases by 40% to 93% as compared to standard low-V_t circuits. Similarly it increases active power by 123% to 191% as compared to dual-V_t circuits. Proposed circuit 2 reduces active power by 50% to 64% as compared to standard low-V_t circuits. Similarly, it reduces active power by 27% to 39% as compared to standard dual-V_t circuits. Proposed circuit2 consume low active power by 69% to 78% as compared to proposed circuit1 due to short circuit short circuit current provided by transistor M8 in proposed circuit1. Drawback of proposed circuit1 has higher active mode power consumption and therefore proposed circuit2 is preferable for power reduction.

CONCLUSION

At room temperature, gate oxide leakage current is dominant over subthreshold leakage current. Similarly, at high temperature subthreshold leakage current is dominant over gate oxide leakage current. In a 45nm CMOS technology both subthreshold and gate oxide leakage current need to be suppressed. Standard dual-V_t with high inputs technique is preferable for reducing subthreshold leakage current as compared to standard dual-V_t low inputs.

Two new circuits are proposed in this paper to reduce both subthreshold and gate oxide leakage current at two temperatures 25°C and 110°C. First proposed circuit reduces leakage power by 54% to 96% as compared to standard low-V_t circuits. It reduces leakage power by 10% to 85% as compared to standard dual-V_t circuits. Second proposed circuits reduce leakage power by 79% to 96% as compared to standard low-V_t circuits. It reduces leakage power by 54% to 90% as compared to dual-V_t circuits.

Proposed circuit1 consumes more active mode power by 40% to 93% as compared to standard low-V_t circuits and 123% to 191% as compared to dual-V_t circuits. Proposed circuit 2 reduces active power by 50% to 64% as compared to standard low-V_t circuits and 27% to 39% as compared to standard dual-V_t circuits. Proposed circuit2 consume low active power by 69% to 78% as compared to proposed circuit1, due to short circuit short circuit current provided by transistor M8 in proposed circuit1.Drawback of proposed circuit1 has higher active mode power consumption and therefore proposed circuit2 is preferable for power reduction.

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