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Positive Feed Back Adiabatic Logic: PFAL Single Edge Triggered Semi-Adiabatic D Flip Flop

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Abstract: The technical constraints and market demands necessitated the urgency of efforts in development of low power circuits. Researchers are exploring all the different factors which affect the low power equations for the circuit. All these being realistic parameters have limits of their optimization. The device scaling, capacitance reduction, voltage scaling, activity factor improving using different set of encoding, speed performance constraints etc. have their physical limitations. Yet, their limiting values are near, but still debatable, with the progress of technology and tremendous amount of efforts all over the world by the researchers. In the scenario many researchers are trying to adopt different optimization and energy conservation principles for VLSI circuit design. The problem formulation is made in accordance, matching with the platform of other engineering fields and transforming, resolving and optimizing them to extract the desired power aware design with benefits attaining from the classical approach. Utilizing the concepts and fundamentals of adiabatic theory in mechanics for formulating the VLSI circuit design problems comes into such an efforts proposed and backed by several researchers. The basic principle in adiabatic logic circuits is to slow down the logic transition varying from logic 1 to logic 0 and vice versa, aiming in reducing the power dissipation. Many different approaches/ techniques are proposed for implementing adiabatic logic circuits. PFAL is one of these techniques which positively promise assisting in the power issues. This paper presents a dual rail, semi adiabatic PFAL D flip flop. Master slave configuration is used for implementing the positive edge flip flop. The basic buffer/inverter configuration is used for driving the functionality of the D flip flop after integrating extra transistors. Tanner ECAD tool is used for simulation and verification the circuit with 1.25 micron technology. The power dissipation for the circuit is 3.50E-02.

Key words: Low Power · Adiabatic logic · Positive Feed Back Adiabatic Logic · D Latch · D Flip Flop

INTRODUCTION

The advancement in the silicon technology has made it possible, the integration of millions of transistor in less area which enabled more and more functionality into same chip. This increasing number of functionality eventually causes the switching operation of the transistor to increase which leads to more dissipation. The fabrication technology has advanced at a much faster rate as compared to the packaging and cooling technology. The cooling technology sometimes plays a constraint in the integration of the number of functionalities in the subject area. Depending upon the packaging technology the cooling of the chip which is very critical in the robustness of the chip limits the transistor count that can be implemented keeping an eye on the highest level of performance at any particular time.

The need of the portable device is increasing rapidly not only because of the convenience of the people but as an essentiality of the social structure now a day. The security systems, surveillance systems, wireless controls, RFID systems, wireless sensor networks, huge automation systems and others, are now becoming essential part of the society. The space industry needs more and more compact ICs with as much as possible functionalities as the cost involved there, compelled, to have most efficient usage of the space available in space crafts, satellites and other devices. Also the robustness

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of the ICs is much more critical factor to make it qualify-able to be used. The portable device needs batteries to supply the chips. Here also the advancements in the battery technologies lag much far behind as compared to the IC technologies. To make up for this the trade offs are to be done.

Also with increase in the temperature of the ICs the IC failure rate increases as every 10 degree rise in temperature doubles the chip failure rate [1-4].

The electronic devices dissipate heat energy to the environment. Hence the hotter ICs are a concern for the environment as well. The dissipated heat energy contributes to the environment warming. Secondly to make the place appropriate for human usage, ACs are to be used which again dissipates heat to environment and also consumes electric power from the grids creating a concern for efficient utilization of the electric energy available.

Hence it is very important now to concentrate on low power circuits rather than only high performance circuits. In last few years there is dramatic shift in the approach of the industry, researchers to come up with the power efficient devices along with increased functionality and performance.

As we know that broadly the power dissipation can be classified as static and dynamic sources majorly due to current source, sub threshold MOS current, gate tunneling, capacitance involved operation speed, activity factor, etc [5]. The generalized power equation is stated as: P= CV2FA. Hence power can be reduced classically by 1) decreasing the capacitance involved in the path, 2) scaling down the operating voltage, 3) slowing down the operation of the circuit, 4) reducing the activity factor of the chip. All these different approach needs different techniques for reducing the power dissipation of the chip.

Adiabatic logic circuits are streamlined with these concepts only. These try to reduce the power by increasing the time required for changing the voltage swings at various levels. The adiabatic concepts is inherently taken from mechanical/ thermodynamics engineering which states “An adiabatic process is one in which no heat is gained or lost by the system” [6-8]. These adiabatic concepts are based upon the work of Landauer and Benett [9-11] and are proving to be very fruitful in reducing the power levels. These circuits can be broadly classified as semi/ partial adiabatic and full /complete adiabatic circuits depending upon the level of follow-ness of the circuit w.r.t. the principles/ concepts laid down by the adiabatic logic approach.

Positive Feedback Adiabatic Logic is a semi adiabatic approach which tries to increase the charging and discharging times maintaining the swing levels. It require presence of dual nature of input (complemented and un-complemented) and creates dual nature for the output as well.

In this paper authors have used the basic buffer/inverter circuit reported, to implement a positive edge triggered D flip flop based upon the adiabatic PFAL technique. Second section, describes the PFAL adiabatic techniques followed by circuit implementation in the next section. Results are reported in the subsequent section and lastly the work is concluded.

Positive feedback adiabatic logic was introduced in 1996 by Vetali [12-14] and shows very positive aspects in addressing the power issues. PFAL comes in dual rail logic family which requires availability of both the complementary and uncomplimentary inputs for the logic function. The logic function (F) and (Fbar) are implemented using NMOS networks alongside the two cross coupled inverts as latch known as sense amplifier which drives the two complementary outputs of the circuit. It consists of two PMOS and two NMOS switches which ultimately prevents the output terminals from degradation of logic levels [15-17]. One of the logic blocks connects the concerned input to the power clock with a low resistance path and on the same time the other function network provide a very high resistance in between the power clock and the other concerned output. But the inverter’s network provides the second output a conducting path to the ground. In this way one of the two outputs (either complementary or un-complementary one) is pulled up to the power clock and other down to the ground. The same is evident from the basic structure depicted in the Figure 1.

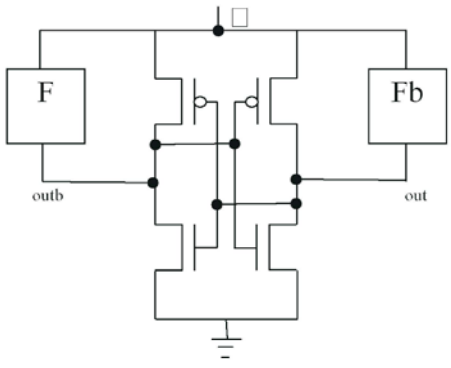

Fig. 1: Basic structure of PFAL

Positive Feedback Adiabatic Logic: PFAL use power clock instead of normal one as it is also used to energies the logic networks. That is no extra dc power source is used and a time varying ac signal is used to actuate the circuit elements along with the clocking control. In PFAL a 4 phase clock is used namely ideal, evaluate, hold, recover stages. Ideal stage is inherently used for pipeline of the different stages. During evaluation phase the logic is evaluated as per the input vectors which is kept retained during the hold stage. The charge is recovered back during the recover stage. But PFAL does not provide full recovery of charge and hence it is considered as partial recovery adiabatic logic family.

Tanner ECAD tool [18] is used for implementing the negative edge triggered, semi adiabatic, dual rail D flip flop. 1.25 micron technology is used. Tanner suit components S edit is used for schematic entry, Tspice is used for simulation and Wedit for waveform analysis. First the dual rail semi adiabatic D latch is implemented which is master slaved to form the dual rail semi adiabatic D flip flop. Both are verified for their functionality and found to work properly. The D latch is shown in Figure 2 and D flip flop is shown in Figure 3.

Circuit Implementation: The two circuits are verified with different set of test vectors covering several input combinations and results shown for 11001100. The implemented D latch has Model Definitions – 2, Computed Models – 2, Independent nodes – 4, Boundary nodes – 4 and Total nodes – 8. On the other hand D flip flop has Model Definitions – 2, Computed Models – 2, Independent nodes – 8, Boundary nodes – 5 and Total nodes – 13.

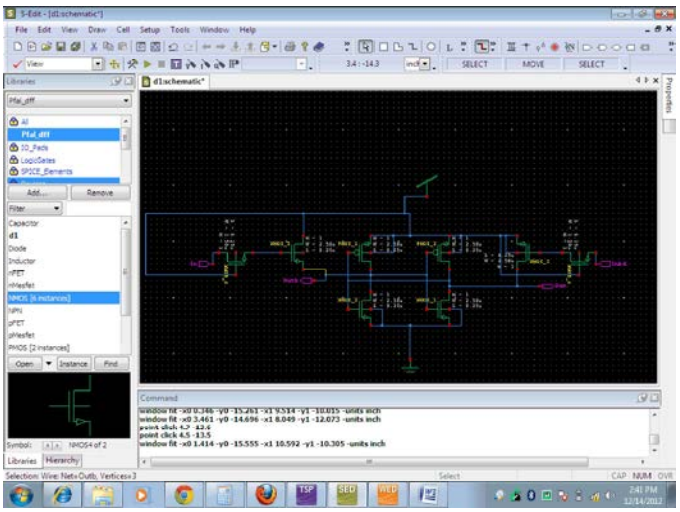

Fig. 2: Basic structure of PFAL D latch

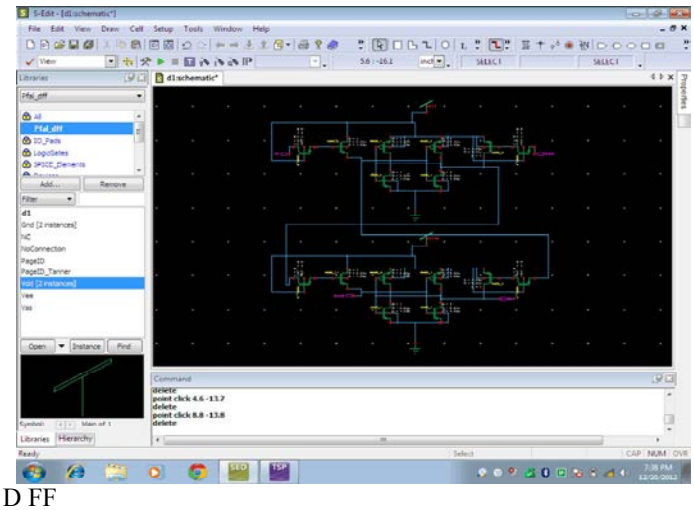

Fig. 3: Structure of PFAL D FF

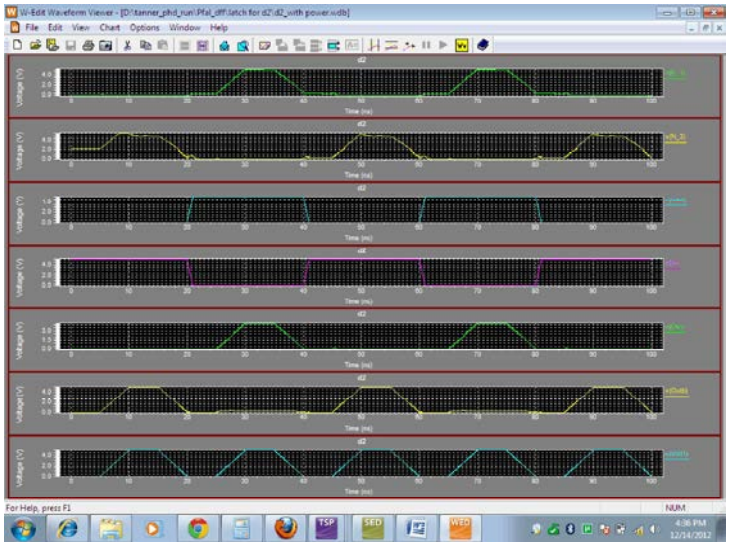

Fig. 4: Waveform for input 11001100

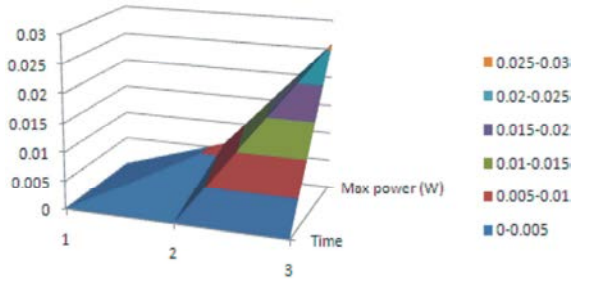

Fig. 5: Power dissipation curve

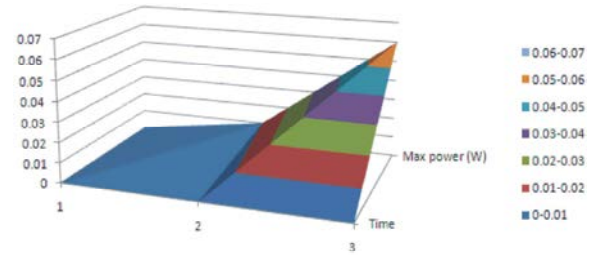

Fig. 6: Power dissipation curve

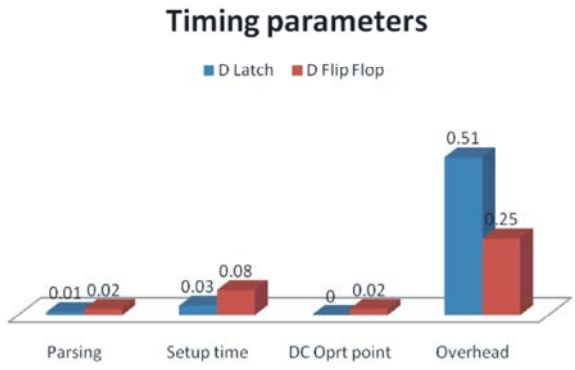

Fig. 7: Power dissipation curve

Table 1: Power results for latch

Power Results D Latch			
Vpulse_voltage from time 0 to 1e-007			
	5.96E-03		
Average power consumed			
Max power (W)	2.60E-02	3.00E-08	Time
Min power	0.00E+00	0	Time

Table 2: Power results for FF

Power Results D FF			
Vpulse_voltage from time 0 to 1e-007			
	3.50E-02		
Average power consumed			
Max power (W)	6.00E-02	3.00E-08	Time
Min power	0.00E+00	0	Time

RESULT

The simulation waveform is show in Figure 4. The power results are tabulated in Table 1 and curve is shown in Figure 5 for D latch and in Table 2, figure 6 for D flip flop respectively. The timing parameters for implemented D latch and d flip flop are shown in Figure 7.

CONCLUSION

The need of low power circuit design techniques is highlighted with classical approach for low power VLSI circuit having different set of parameter involved. The basic concept adiabatic circuit design process is described. The working of Positive Feedback Adiabatic Logic (PFAL) Circuit Design Techniques is provided with its basic structure. Utilizing the basic PFAL inverter/buffer D flip flop is

implemented, verified and analyzed. From the simulations the functionality of the implemented flip flop is found to be satisfactory.

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