American-Eurasian Journal of Scientific Research 11 (2): 125-134, 2016
ISSN 1818-6785

DOI: 10.5829/idosi.aejsr.2016.11.2.22771

Modelling and Control of 27-Level Inverte Using Unified Phase Shifted Modulation (UPPWM) for Power Systems

[1]P. Tamilvani and [2]K.R. Valluvan

[1]Department of EEE, EBET Group of Institutions, Kangayam-638108, India
[2]Department of ECE, Velalar College of Engineering & Technology, Erode, India

Abstract: Inverter serves a long variety of applications ranging from simple converting of battery power to sinusoidal AC to high power HVDC transmission of electricity for a very long distance. Inverters have constantly gone over many technological improvements, starting from the development of the switching gates technologies, improvements in their max power handling capacities and reduction in switching losses to improvement in the triggering circuitry. Developing of new pulse triggering techniques and their specific adjustments as per the demand. This paper presents the latest development of modelling and control of multilevel inverters. Along with the multilevel, we have worked on the carrier based Sine PWM modes, namely phase shifted pulse width modulation and level shifted pulse width modulation are can be used in the cascaded H-Bridge Inverter. This paper focus on phase shifted and level shifted pwm based cascaded multilevel inverter topology. It offer several advantages compared to the conventional level shifted inverter in terms of lower dv/dt stresses, lower electromagnetic interference, smaller rating and high efficiency. The proposed method has been designed an twenty seven level cascaded multilevel inverter by using phase shifted pulse width modulation technique and compare the Total harmonic distortion. The selected pattern has been exposed to give superior performance in total harmonics distortion. Simulation and experimental results confirm the feasibility of proposed method. The technique used to eliminate harmonics and to obtain approximate pure sinusoidal output waveform is Pulse Width Modulation technique. The models discussed in this paper have been simulated on Matlab/Simulink software and the respective THD has been determined by FFT analysis of the output waveform by the software.

Key words: Matlab/Simulink · Total Harmonic Distortion (THD) · Multilevel Inverters · PWM

INTRODUCTION

Various industrial applications have begun to require higher power apparatus in recent years. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power inverter structure has been introduced as an alternative in high power and medium voltage applications. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind and fuel cells can be easily interfaced to a multilevel inverter system for a high power application.

Inverters are the power electronic circuit, which converts the DC voltage into AC voltage. The DC source is normally a battery or output of the controlled rectifier. The output voltage waveform of the inverter can be square wave, quasi-square wave or low distorted sine wave. The output voltage can be controlled with the help of drives of the switches. The pulse width modulation techniques are most commonly used to control the output voltage of inverters. Such inverters are called as PWM inverters. The output voltage of the inverter contains harmonics whenever it is not sinusoidal. These harmonics can be reduced by using proper control schemes.

In the last few years, the necessity of increasing the power quality enhancement in industry has sustained the continuous development of multilevel inverters due to high efficiency with low switching frequency control method. The multilevel inverters improve the AC power quality by performing the power conversion in small

Corresponding Author: P. Tamilvani, Department of EEE, EBET Group of Institutions, Kangayam-638108, India.

voltage steps resulted in lower harmonics. The output voltage on the AC side can take several discrete levels of equal magnitude. The harmonic content of this output voltage waveform is greatly reduced, a smaller filter size and a lower EMI, if compared with a two level voltage waveform. Several topologies for multi-level inverters have been proposed over the years the most popular being the diode clamped, flying capacitor and cascaded H-bridge structures. One aspect which sets the cascaded H-bridge apart from other multi-level inverters is the capability of utilizing different DC voltages on the individual H-bridge cells which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher frequency Inverters.

The use of a multilevel inverter to control the frequency, voltage output (including phase angle) and real and reactive power flow at a dc/ac interface provides significant opportunities in the control of distributed power systems.

The proposed multilevel inverter includes an array of power semiconducting devices and dc voltage sources; it generates the output voltage with stepped waveforms. Compared to conventional multilevel inverters, proposed multilevel inverter is used to synthesize the output voltage and current with reduced harmonic distortion and lower electromagnetic interference (EMI). By increasing number of levels in the output of multilevel inverter, the output voltage will have more number of steps in generating a staircase waveform, which results in reduced harmonic distortion. However, the generation of large number of levels in the output will increase the number of devices and that will be controlled or compensated by the proposed multilevel inverter topology. That means the complexity of the equipment is minimized.

Previous Research: Numerous related research works are already existed in literature which based on different multilevel inverter topologies. Some of them are reviewed here.

A PV inverter, which is an important element in the PV system, is used to change dc power from the solar module into ac power. The need of several sources on the DC side of the converter makes multilevel technology gorgeous for PV applications. Because the Multi-Level Inverters (MLI) are classified into two types namely distinct source and Multisource MLI. Distinct source MLI has only one DC source and remaining are the Capacitors or Clamping Diodes. One type of distinct source MLI is the Neutral Point Clamped (NPC) MLI or also known as Diode Clamped Inverter (DCI). The DCI create the small step of staircase output voltage from several levels of DC capacitor voltages. The other type of distinct source MLI is Flying Capacitor (FC) MLI. It requires huge number of capacitors to clamp the device voltage to one capacitor voltage level [1-5].

The multilevel inverters can be divided into two groups from the view point of the dc voltage sources amplitudes: the symmetric and the asymmetric topologies. In the symmetric topology, the values of all of the dc voltage sources are equal. The asymmetric inverters have different DC voltage values. In order to increase the number of output voltage level, the values of the dc voltage sources are selected to be different, these topologies are called asymmetric [7-8].

V. Kamaldas *et al.* [10] Multilevel inverter is one of the most recent and popular type of inverter founds its applications in the system based on renewable energy. This paper describes a new Single-phase seven level inverter topology for solar photo voltaic (PV) system using a carrier based PWM control scheme. This new topology has reduced number of switches for an increased number of levels when compared to conventional seven-level multilevel inverter. Here CPWM switching scheme is used to control the switches in this multilevel inverter and this inverter is fed from a solar PV. In this proposed topology, six power electronic switches are used for a seven-level inverter. By using this inverter topology, the harmonics is reduced and efficiency is enhanced significantly. Simulation work is done using the MATLAB/SIMULINK software which validates the proposed method and finally Total Harmonic Distortion is analyzed.

Vincent Roberge *et al.* [11] implemented Genetic algorithm based Multilevel inverters to improve the high power inverters due to their high-voltage operation, high efficiency, low switching losses and low electromagnetic interference. A parallel implementation of the GA on graphical processing unit is proposed in order to accelerate the computation of the optimal switching angles for multilevel inverters with varying dc sources. GA is used to ignore solving the equation associated with the highest order harmonics. A reduction in the eliminated harmonics results in an increase in the degrees of freedom. As a result, the lower order harmonics are eliminated in more operating points. A 9-level inverter is chosen as a case study. The genetic algorithm (GA) for optimization purposes is used.

Pedram Sotoodeh *et al*. [12] presented the capability of a new single-phase wind energy inverter with flexible AC transmission system. The proposed inverter is able to

regulate active and reactive power transferred to the grid and which is placed between the wind turbine and the grid. Power factor can be controlled by using this inverter because of this inverter is equipped with distribution static synchronous compensator .The main objective of this his paper is to introduce new ways to increase the growth of renewable energy systems into the distribution systems. This will encourage the utilities and customers to use interactive supply of energy. Moreover, by using these types of converters will significantly reduce the total cost of the renewable energy application. In this paper, modular multilevel converter is used as the desired topology to meet all the requirements of a single-phase system such as compatibility with IEEE standards, total harmonic distortion (THD), efficiency and total cost of the system. This paper was implemented using 11- level inverter then the simulations have been done in MATLAB/Simulink.

Bindeshwar Singh *et al*. [13] have presented the concept of decreased harmonic distortion in the output waveform without decreasing the inverter power output using 11-level inverter. The proposed multilevel inverters have been attracting the industry in the recent decade for high-power and medium-voltage energy control. This paper presents the most important topologies like diode-clamped inverter (neutral- point clamped), capacitor-clamped (flying capacitor) and cascaded multilevel with separate dc sources. This paper also presents the most relevant modulation methods developed for this family of converters: multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination and space-vector modulation. Authors strongly believe that this survey article will be very much useful to the researchers for finding out the relevant references in the field of topologies and modulation strategies of multilevel inverter.

Zhong Du *et al*. [14] implemented cascaded H-bridge multilevel inverter using only a single dc power source and capacitors. Generally, the Standard cascaded multilevel inverters require *n* dc sources for 2*n* + 1 level. Without requiring transformers, the scheme proposed here allows the use of a single dc power source with the remaining n- 1 dc sources being capacitors, which is referred to as new modify new modified hybrid cascaded H-bridge multilevel inverter (HCMLI) in this paper. The proposed inverter can simultaneously maintain the dc voltage level of the capacitors and choose a fundamental frequency switching pattern to produce a nearly sinusoidal output. HCMLI using only a single dc source for each phase is promising for high-power motor drive applications as it significantly decreases the number of required dc power supplies, provides high-quality output power due to its high number of output levels and results in high conversion efficiency and low thermal stress as it uses a fundamental frequency switching scheme. This paper was implemented for 7- level HCMLI with fundamental frequency switching control and how its modulation index range can be extended using triple harmonic compensation.

D. Kalyanakumar *et al*. [15] investigated new modified new modified hybrid 7-Level H– bridge Inverter was used in a Distribution Static Compensator (DSTATCOM) in Power System industry, so that the proposed system benefits of low harmonics distortion with reduced number of switches to achieve the output over the conventional cascaded 7-level inverter and reduced switching losses. The proposed system is used to obtain the improved power factor, compensate the reactive power and suppress the total harmonics distortion (THD) drawn from a Non-Liner Diode Rectifier Load (NLDRL) of DSTATCOM, by using Sub-Harmonics Pulse Width Modulation (SHPWM) technique is used as control for the switches of HSL H – bridge Inverter. The proposed new modified new modified hybrid seven levels H – bridge implemented using MatLab/Simulink simulation software for shunt compensation of a 4.5 kV distribution system.

Proposed Twenty Seven Level Inverters: In this work, the asymmetric 27 level inverter is presented. This inverter is designed to avoid the regeneration problem - power flow from the load to the inverter - in some of the power cells. This is achieved by obtaining the firing angles associated with the power cells considering a minimum load voltage THD. Finally, a power flow analysis is accomplished and simulated results show the feasibility of this approach. Fig. 1 shows the 27 level proposed inverter.

The traditional two or three levels inverter does not completely eliminate the unwanted harmonics in the output waveform. When the number of levels increases, the total harmonic distortion decreases significantly. This proposed method produce the pulses using Matlab/Simulink based embedded controller for twenty level asymmetrical cascaded multilevel inverter. Each H-bridge inverter can produce 27 different voltages, the output levels are 13Vdc,, 12Vdc, 11Vdc, 10Vdc, 9Vdc, 8Vdc, 7Vdc, 6Vdc, 5Vdc, 4Vdc, 3Vdc, 2Vdc, Vdc, 0, -Vdc, -2Vdc, -3Vdc, -4Vdc, -5Vdc, -6Vdc, -7Vdc, -8Vdc, -9Vdc, -10Vdc, -11Vdc, -12Vdc -138Vdc.

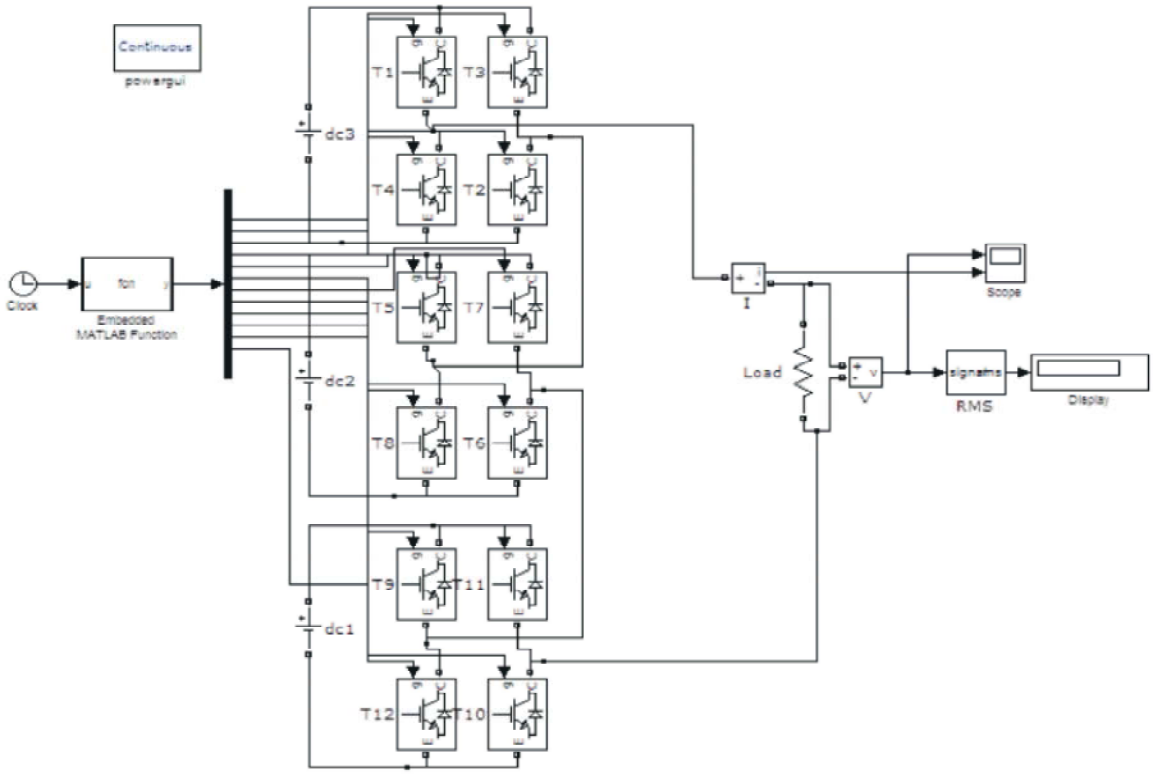


Fig. 1: Enhanced H-Bridge inverter for 27 level inverter

Phase Shifted Sine PWM Scheme: Fig. 2 shows the Phase Shifted PWM all the triangular carriers have the same frequency and same peak-peak amplitude. But there is a phase shift between any two adjacent carrier waves. For m Voltage levels (m-1) carrier signals are required and they are phase shifted with an angle of $\theta = (360°/m-1)$. The gate signals are generated with proper comparison of carrier wave and modulating signal.

In general, a multilevel inverter with m voltage levels requires (m-1) triangular carriers In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by PhCR = 360°/(m-1).

Switching Pattern Scheme: The switching sequence values are calculated dynamically as mentioned in the following section. Switching times T1 & T2 (for sector 1) or T2 & T3 (for sector 2) is calculated during each sampling period and implemented accordingly.

Here we demonstrate calculation for Sector 1, which can be similarly followed for other sectors by substituting their required adjacent voltage space vectors. T1, T2, T0 & T7 are calculated by Volt-Second integral of VREF for a given sampling period in the sector.

We have,

$$V_{ref} = V_1 \cos\theta + V_2 \sin\theta$$

$$V_{ref} = V_1 T_1 + V_2 T_2$$

By Volt-Second Integral Of

$$\frac{1}{T_s}\int_0^{T_s} V_{ref}\,dt = \frac{1}{T_s}\left[\int_0^{T_0} 0\,dt + \int_0^{T_1} V_1\,dt + \int_0^{T_2} V_2\,dt + \int_0^{T_7} 0\,dt\right]$$

$$V_{ref}\cdot T_s = V_1 T_1 \cos\theta + V_2 T_2 \cos(60-\theta)$$

Solving For T0, T1 and T2 & T7 Gives:

$$T_1 = 3/2\left[(V_{ref}/v3)\cos\theta - (V_{ref}/3)\sin\theta\right]$$

$$T_2 = V_{ref}\sin\theta$$

where,

$V_1 = V_{dc}\,(V_{dc}/v3)$

Above Equations are derived for Sector 1, similarly other sector equations are to be derived for their respective switching time calculations.

These type of inverter scheme is to get the better sinusoidal output compared with low level inverters.

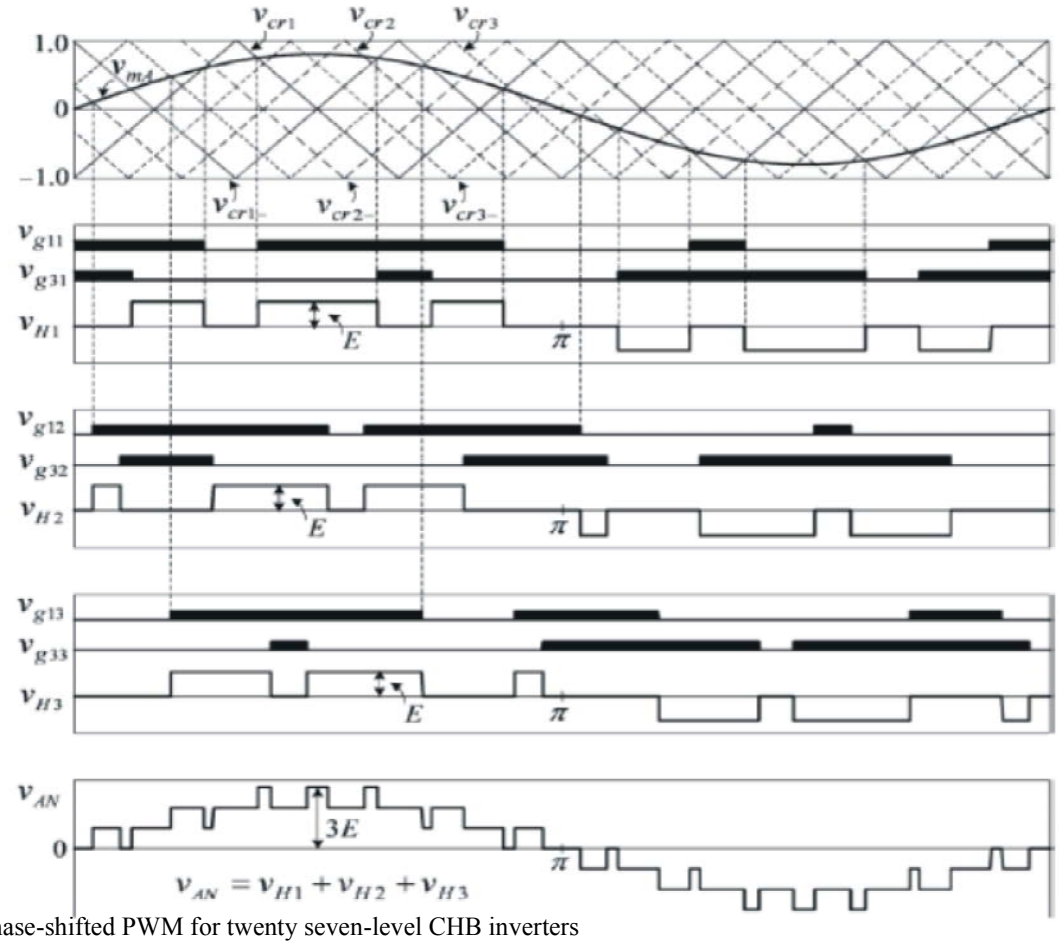


Fig. 2: Phase-shifted PWM for twenty seven-level CHB inverters

Table 1: Switching time for a sector 1

Sector	Upper Switches (S_1, S_3, S_5)	Lower Switches (S_4, S_6, S_2)
1	$S_1 = T_1 + T_2 + T_0/2$	$S_4 = T_0/2$
	$S_3 = T_2 + T_0/2$	$S_6 = T_1 + T_0/2$
	$S_5 = T_0/2$	$S_2 = T_1 + T_2 + T_0/2$
2	$S_1 = T_2 + T_0/2$	$S_4 = T_1 + T_0/2$
	$S_3 = T_1 + T_2 + T_0/2$	$S_6 = T_0/2$
	$S_5 = T_0/2$	$S_2 = T_1 + T_2 + T_0/2$
3	$S_1 = T_0/2$	$S_4 = T_1 + T_2 + T_0/2$
	$S_3 = T_1 + T_2 + T_0/2$	$S_6 = T_0/2$
	$S_5 = T_2 + T_0/2$	$S_2 = T_1 + T_0/2$
4	$S_1 = T_0/2$	$S_4 = T_1 + T_2 + T_0/2$
	$S_3 = T_2 + T_0/2$	$S_6 = T_1 + T_0/2$
	$S_5 = T_1 + T_2 + T_0/2$	$S_2 = T_0/2$
5	$S_1 = T_2 + T_0/2$	$S_4 = T_1 + T_0/2$
	$S_3 = T_0/2$	$S_6 = T_1 + T_2 + T_0/2$
	$S_5 = T_1 + T_2 + T_0/2$	$S_2 = T_0/2$
6	$S_1 = T_1 + T_2 + T_0/2$	$S_4 = T_0/2$
	$S_3 = T_0/2$	$S_6 = T_1 + T_2 + T_0/2$
	$S_5 = T_2 + T_0/2$	$S_2 = T_1 + T_0/2$

The asymmetrical multilevel inverter is used to obtain a high resolution. By this method decrease the input voltage and get better efficiency in a 27-level multi-level inverter structure. The asymmetrical hybrid technique is used to improve the level of inverter and extends the design flexibility and reduces the harmonics.

RESULTS AND DISCUSSION

Simulations are done to observe the output waveform, calculate the Total harmonic Distortion THD, perform FFT analysis and observe the dominant harmonics created and derive conclusions accordingly. Various PWM techniques are also compared on the basic of their THDs, Data bus utilizations and other parameters.

The simulation of phase shifted Sine PWM as done as shown in the Figure 3. The simulation parameter setting was as below:

VDC-1 = 100V VDC-2 = 100V ma = 1 mf = 15 i.e. fC = 750Hz

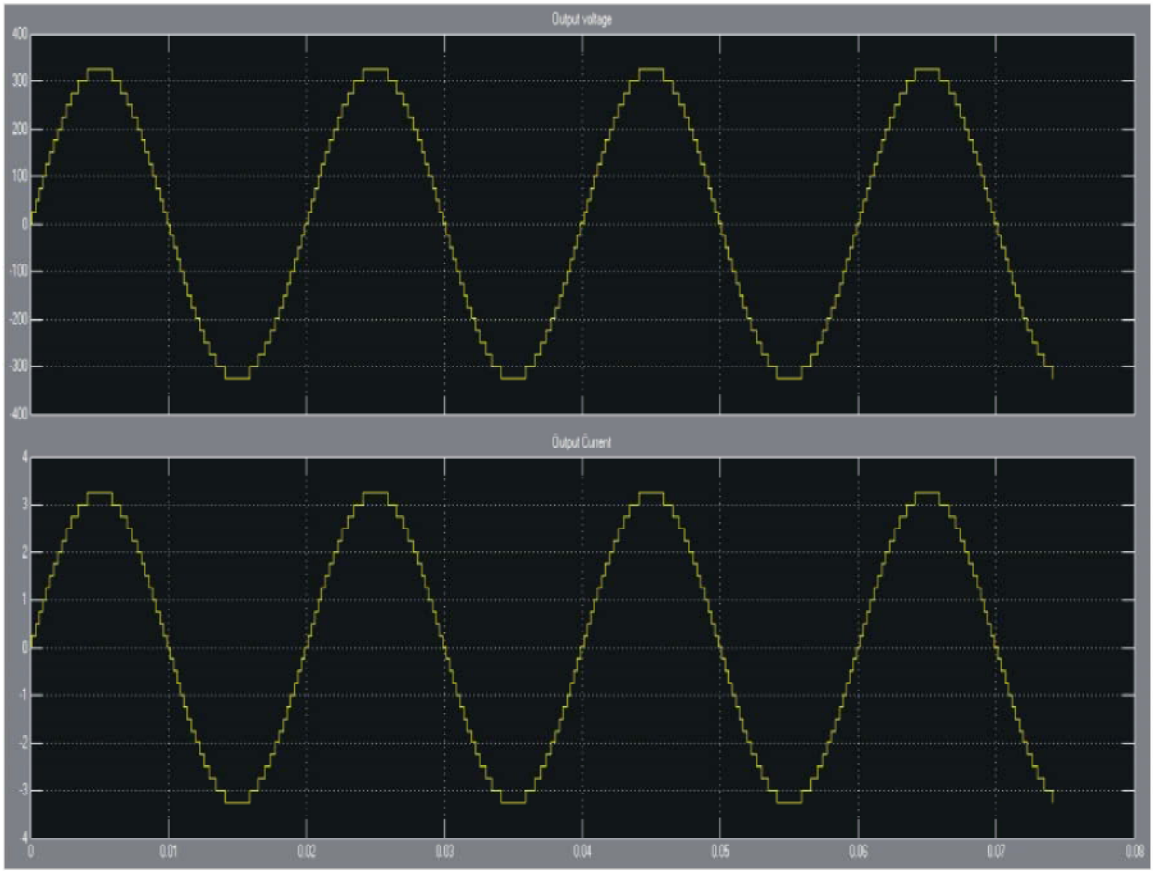


Fig. 3: Simulation results of proposed 27 Level inverter for Voltage and current with respect to time

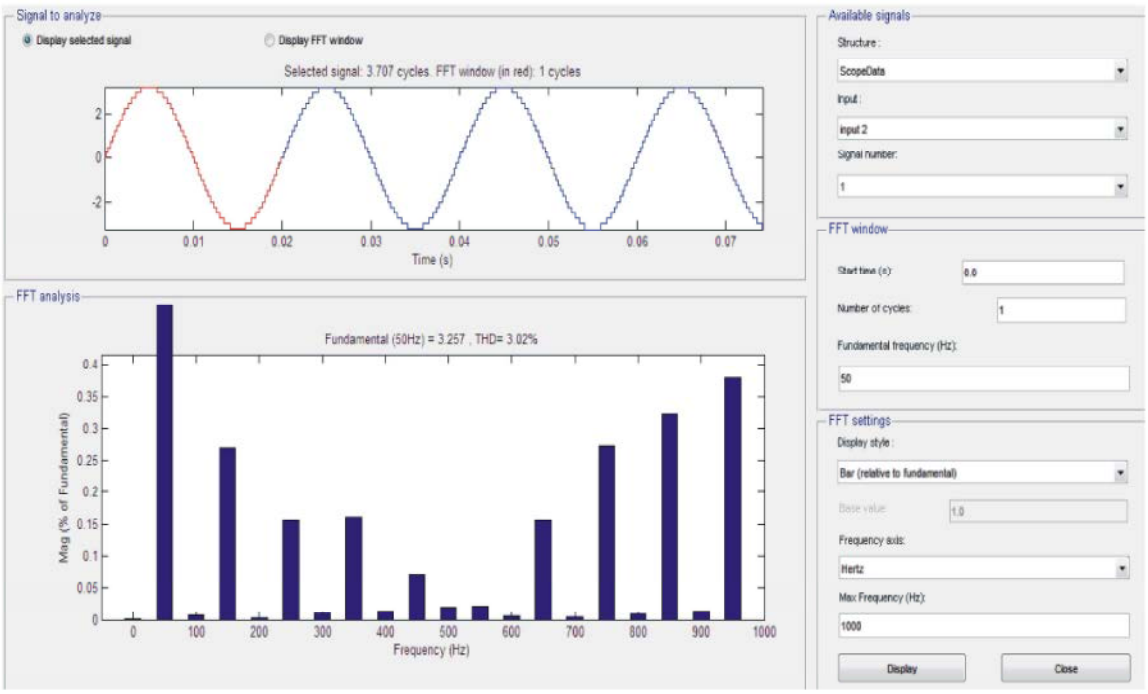


Fig. 4: THD Analysis %

Table 2: Comparison between SPWM, UPPWM and CLPWM for 27-level inverter

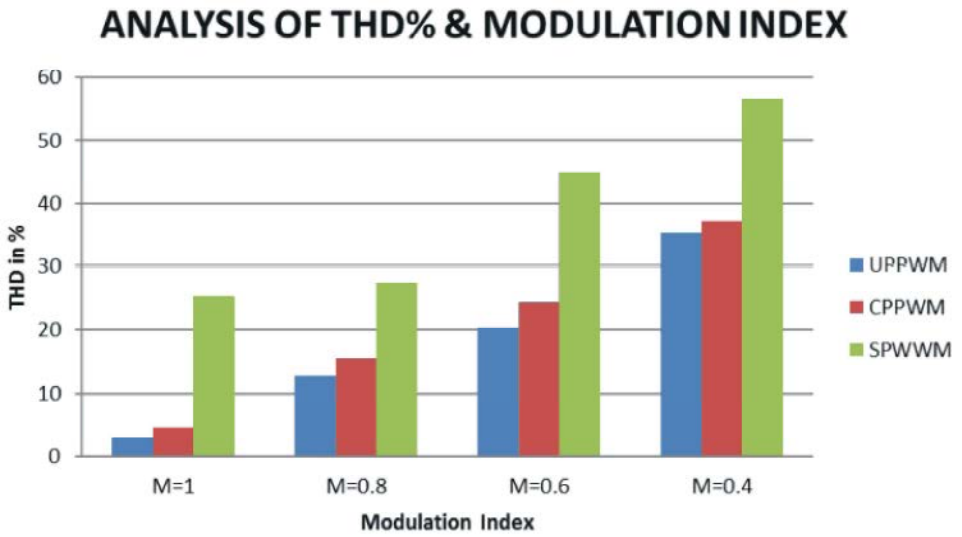
Parameters	SPWM for 27 level	Existing CLPWM	Proposed UPPWM
THD	13.58%	4.69%	3.02%
Switching strees	more	less	less
Number of switches	28	12	12
Switching losses	More	Less	Very less
Energy conversion efficiency	Good	Better	Best

Table 3: Comparison between phase shifted(UPPWM) and level shifted(CLPWM)

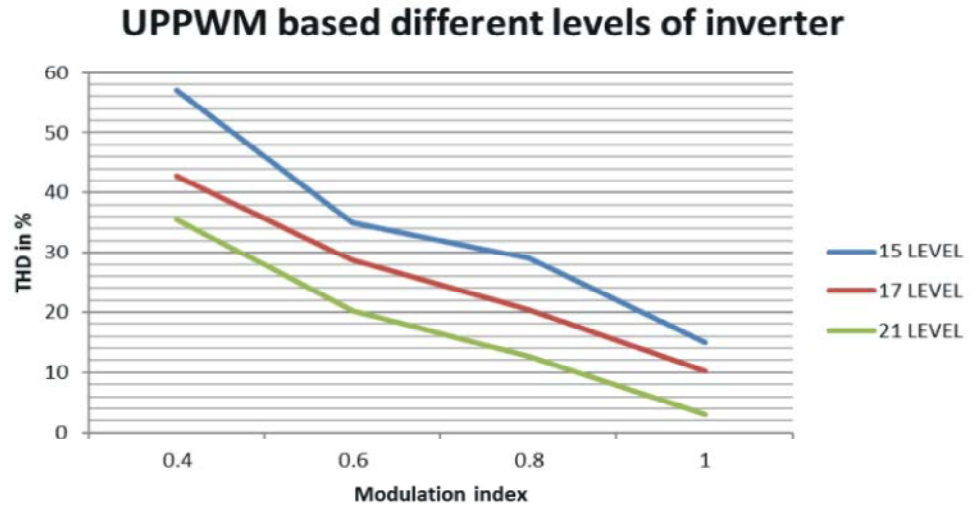
Comparison	Phase Shifted Modulation	Level Shifted Modulation (IPD)
Device switching frequency	Same for all devices	Different
Device conduction period	Same for all devices	Different
Rotating of switching patterns	Not required	Required
Line to line voltage	Good	Better

Table 4: THD (%) Analysis of CLPWM & UPPWM based on Different modulation index values

Modulation Index	UPPWM(THD%)	CLPWM(THD%)	SPWM(THD%)
1	3.02	4.96	25.25
0.8	12.78	15.54	27.42
0.6	20.34	24.33	45
0.4	35.56	37.21	56.63



Graph 1: Analysis of THD Vs Modulation Index



Graph 1: Analysis of UPPWM based different levels of inverter

In this proposed system of a simulation result is the output voltage, output current and step level will be displayed with respect to time. The maximum step level of 27-Level displayed. And the voltage level for various steps displayed. The output voltage per steps with the time will be displayed. The range of voltage is up to ±300V and ±3 amp can be delivered.

The harmonic spectrum of output voltage is shown below. The reduction of THD is used to evaluate the performance of the multilevel inverter. In the FFT analysis, one cycle of output stepped waveform of 27-level inverter is shown in Figure 6(a). on the basis of this waveform the total harmonic distortion in 27-level inverter is calculated by FFT analysis and the calculated THD with its plot has been shown in Figure 6(b) below.

The main attention behind the objective of proposed twenty seven level inverter topologies is to achieve the high power quality, low total harmonic distortion and better power factor. The harmonic content can be measured in terms of total harmonic distortion by using FFT analysis harmonic spectrum. The proposed multilevel inverters have been validated using MATLAB/ SIMULINK software and the comparison of results on basis of analysis has been tabulated below.

Comparitive Results Between Clpwm and UPPWM: THD analysis of CLPWM and UPPWM were compared and tabulated from Table 2-4. It was observed that UPPWM generates lesser THD for every corresponding CLPWM for any given ma.

The comparison between the total harmonic distortion with respect to the various modulation index for UPPWM, CPPWM, SPWM of 27 level cascaded inverter is shown below in Graph 1. It can be observed that the THD is better in UPPWM at m=1 has the THD of 3.02% .

Multilevel cascaded H-bridge inverters of fifteen, seventeen, twenty seven and thirty one levels have been simulated using Matlab/simulink. The THD calculation is done by the FFT analysis of output waveform of each inverter and it was found that, as the levels in the inverters are increased the THD is decreased.

The comparison between the total harmonic distortion with respect to the modulation index for UPPWM based 15, 17 and 21-level cascaded inverter is shown below in graph 2. It can be observed that the THD is better in 21- level inverter.

CONCLUSION

In this paper, 27-Level Cascaded multilevel inverter has been designed with unified phase shifted PWM techniques. And compare the total harmonic distortion of 27 –level inverter for different PWM techniques. This technique is used to improve the level of the inverter and extends the design flexibility and reduces the harmonics. Multilevel inverter is obtain output with high resolution. When the number of level increase total harmonic distortion should be decreased. The 27-level Cascaded multilevel inverters with THD characteristics are verified through simulation results by using MATLAB. The simulation results are give better quality of systems with low harmonic characteristics.

REFERENCES

1. Rodriguez, J., J.S. Lai and F.Z. Peng, 2002. “Multilevel Inverters: Survey of Topologies, Controls and Applications, ” IEEE Transactions on Industry Applications, 49(4): 724-738.
2. Lai, J.S. and F.Z. Peng, 1996. “Multilevel Converters-A new Breed of Power Converters, ” IEEE Trans. Ind. Applicat., 32: 509-517.
3. Tolbert, L.M., F.Z. Peng and T. Habetler, 1999. “Multilevel Converters for Large Electric drives, ” IEEE Trans. Ind. Applicat., 35: 36-44.
4. Nabae, A., I. Takahashi and H. Akagi, 1981. “A New Neutral-point Clamped PWM inverter, ” IEEE Trans. Ind. Applicat., IA-17, pp: 518-523.
5. Li, Y., D.M. Vilathgamuwa and P.C. Loh, 2004. "Design, analysis and real-time testing of a controller for multibusmicrogrid system", IEEE Trans. Power Electron., 19(5): 1195-1204.
6. Hatziargyriou, N., H. Asano, R. Iravani and C. Marnay, 2007. "Microgrids", IEEE Power Energy Mag., 5(4): 78-94.
7. Katiraei, F., R. Iravani, N. Hatziargyriou and A. Dimeas, 2008. "Microgrids management", IEEE Power Energy Mag., 6(3): 54 -65. 8. Pan, C.T., C.M. Lai and M.C. Cheng, 2010. "A novel integrated single-phase inverter with an auxiliary step-up circuit for low-voltage alternative energy source application", IEEE Trans. Power Electron., 25(9): 2234-2241.
8. Infield, D.G., P. Onions, A.D. Simmons and G.A. Smith, 2004. "Power quality from multiple grid-connected single-phase inverters", IEEE Trans. Power Del., 19(4): 1983-1989.

9. Wang, J., 2008. "Practical design considerations of power electronics in new modified new modified hybrid and fuel cell vehicles, " in Proc. IEEE VPPC, Harbin, China, pp: 1-6.
10. Vincent Roberge, Mohammed Tarbouchi and Francis Okou, 2014. 'Strategies to Accelerate Harmonic Minimization in Multilevel Inverters Using a Parallel Genetic Algorithm on Graphical Processing Unit, IEEE Transactions On Power Electronics, 29(10).
11. Pedram Sotoodeh and Ruth Douglas Miller, 2014. Design and Implementation of an 11-Level Inverter With FACTS Capability for Distributed Energy Systems'IEEE Journal of Emerging and Selected Topics in Power Electronics, 2(1).
12. Bindeshwar Singh' New multilevel inverter topology with reduced number of switches'.
13. Zhong Du, 2009. IEEE, Leon M. Tolbert, Burak Ozpineci and John N. Chiasson, 'Fundamental FreSuency Switching Strategies of a Seven-Level new modified new modified hybrid Cascaded H-Bridge Multilevel Inverter' IEEE Transactions on Power Electronics, 24(1).
14. Sivakumar, K., Anandarup Das, Rijil Ramchand, Chintan Patel and K. Gopakumar, 2010. A new modified new modified hybrid Multilevel Inverter Topology for an Open-End Winding Induction-Motor Drive Using Two-Level Inverters in Series With a Capacitor-Fed H-Bridge Cell' IEEE Transactions on Industrial Electronics, 57(11).
15. Kalyanakumar, D., V. Kirbakaran and K. Ramash Kumar, 'new modified new modified hybrid Seven Level H- Bridge Inverter Based Dstatcom Control Using Sub-Harmonic Pulse Width Modulation Techni Sue'.
16. Bharath, K. and J. Satputaley, Single Phase Asymmetrical Cascaded Multilevel Inverter Design for Induction Motor'
17. Lu, S., K.A. Corzine and M. Ferdowsi, 2007. "A uniSue ultracapacitor direct integration scheme in multilevel motor drives for large vehicle propulsion," IEEE Trans. Veh. Technol., 56(4): 1506-1515.
18. Babaei, E., S.H. Hosseini, G.B. Gharehpetian, M.T. Haque and M. Sabahi, 2007. "Reduction of DC voltage sources and switches in asymmetrical multilevel converters using a novel topology", Electric Power Systems Research, 77: 1073-1085.
19. Patangia, H. and D. Gregory, 2006. "Implementation of a multilevel SPWM inverter for capacitive loads", Industrial Technology IEEE International Conference, pp: 283-287.
20. Timothy, L., 2002. "The Power Electronics Handbook", CRC Press Industrial Electronics Series Press.
21. Ewanchuk J., J. Salmon and A.M. Knight, 2009. "Performance of a high-speed motor drive system using a novel multilevel inverter topology", IEEE Transactions on Industry Applications, 45: 1706-1714.
22. Leon, J.I., S. Vazquez, R. Portillo, L.G. Franquelo, J.M. Carrasco, P.W. Wheeler and A.J. Watson, 2006. "Three-dimensional feed forward space vector modulation applied to multilevel diode-clamped converters", IEEE Transactions on Industrial Electronics, 56: 101-109.
23. Shukla, A., A. Ghosh and A. Joshi, 2010. "Flying-capacitor-based chopper circuit for DC capacitor voltage balancing in diode-clamped multilevel inverter", Industrial Electronics, IEEE Transactions on, 57: 2249-2261.
24. Calais M., V.G. Agelidis, L.J. Borle and M.S. Dymond, 2000. "A transformerless five level cascaded inverter based single phase photovoltaic system", IEEE Proc., 3: 1173-1178.
25. Park, S.J., F.S. Kang, S.E. Cho, C.J. Moon and H.K. Nam, 2005. "A novel switching strategy for improving modularity and manufacturability of cascaded-transformer-based multilevel inverters", Electric Power Systems Research, 74: 409-416.
26. Lai, Y.S. and F.S. Shyu, 2002. "Topology for new modified new modified hybrid multilevel inverter", IEE Proceedings on Electric Power Applications, 149: 449-458.
27. Rech, C., H. Pinheiro, H.A. Grundling, H.L. Hey and J.R. Pinheiro, 2002. "Analysis and comparison of new modified new modified hybrid multilevel voltage source inverters", IEEE 33rd Annual Power Electronics Specialists Conference, 2: 491-496.
28. Li, L., 1999. "Optimal surplus harmonic distribution in selected harmonic elimination PWM technique for multilevel inverters", The 25th Annual Conference of Industrial Electronic Society, 2: 589-594.
29. Zhang, H., 2000. "Multilevel inverter modulation schemes to eliminate common-mode voltages", IEEE Transactions on Industry Applications, 36: 1645-1653.
30. Chen, Y.M., C.H. Hsieh and Y.M. Cheng, 2001. "Modified SPWM control schemes for three-phase inverters", IEEE International Conference on Power Electronics and Drive Systems, 2: 651-656.

31. Radan, A., A.H. Shahirinia and M. Falahi, 2007. "Evaluation of carrier-based PWM methods for multi-level inverters", IEEE Industrial Electronics Int. Symposium, pp: 389-394.
32. Jeevananthan, S., R. Nandhakumar and P. Dananjayan, 2007. "Inverted sine carrier for fundamental fortification in PWM inverters and FPGA based implementations", Serbian Journal of Electrical Engineering, 4: 171-187.
33. Geethalakshmi, B., K. Delhi Babu, C.M. Varma and P Dananjayan, 2007. "Performance evaluation of three phase cascaded H-bridge multilevel inverter based on multi carrier PWM techniques", International Conference on Advances in Energy Research.
34. IEEE, Recommended practices and requirements for harmonic control in electrical power systems, IEEE 519-1992, Standard.