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Reducing Switching Activities Through Data Encoding in Network on Chip

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Abstract: As technology shrinks, the overall power dissipation in communication system is due to the links. In this paper, we present a data encoding scheme to reduce power dissipation in the network on chip (NoC). The proposed end to end data encoding scheme takes the benefits of wormhole switching and concentrate number of transition occurred between the network interfaces. The idea presented is based on the packets are encoded before they are injected into the network which minimize both the coupling switching activity and the switching activity in the network on chip links. The transition occurred in four types. Each types as its own criteria, four types of transition are compared and synthesized with respect to power as a parameter.

Key words: Network on chip (NoC) · Data encoding · Coupling switching activity

INTRODUCTION

Network on chip is an emerging paradigm for communications within large VLSI systems implemented on a single silicon chip. It improves the scalability and power efficiency of system on chip. In NoC the power dissipation in the links is starts to compete with the communication system. The data encoding technique is introduced to reduce the bit level transition occurred in the link, data packets contain more bit transition in the links that leads more power dissipation [1]. Driver and receiver on the bus use the bus invert method to code and decode the information, it reduces the switching activity but the performance is degraded in the NoC [2]. The modified boundary shift coding takes the advantage of parity bit scheme and it is used for crosstalk avoidance with simpler encoder and decoder circuits but it needs fewer numbers of additional wires in on chip interconnection [3].

The three dimensional tool determines the best path for the communication flow for NoC topology and contains traffic between many different cores [4]. Bus invert method contains the data pattern in random manner that are injected via links leads to reduce the switching activity and it is not suitable for deep submicronmeter technology [5]. The coupling switching activity is reduced by bus invert coding method in that the links are inverted which is based on hamming distance. There is a crosstalk effects occurred in between the links that is reduced by bus placement technique in that bus lines are nonuniformly spaced. This would lead the design complexity in the buses [6].

The power consumption is not only due to the transition activities but also due to the input and output pins so that working zone encoding method is introduced to encode the lines. This method is effective for data only and instruction only traces whereas it is not suitable for instruction data traces [7]. The major goal of data encoding technique is reduces the switching activity and coupling switching activity by the flits are encoded when they are inserted into the network interface [8]. The proposed method focus on reducing the number of transition that leads less power dissipation.

Overview of Proposal: Data encoding technique concentrates on link level power dissipation which minimizes the switching activity and coupling switching activity and it is based on odd inversion condition (Table I). The flits are data encoded before they are inserted into the network interface except the header flit [9]. Data encoding techniques referred the end to end encoding scheme [10]. It takes the wormhole switching

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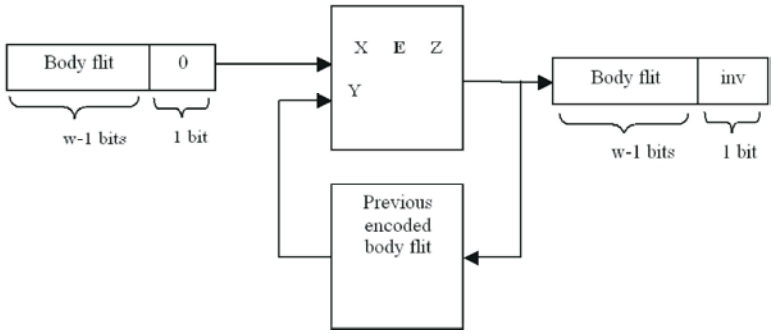

Fig. 1: Encoder Architecture Scheme

Table I: Odd inversion effect

Time	Normal		Odd inverted	
t-1	Type 1	01,10	Type 2	01,10
t		00,11		10,01
	Type 1	00,11	Type 3	00,11
		10,01		11,00
	Type 1	00,11	Type 4	00,11
		10,01		10,01
t-1	Type 2		Type 1	
t	01,10		01,10	
	10,01		11,00	
t-1	Type 3		Type 1	
t	00,11		00,11	
	11,00		10,01	
t-1	Type 4		Type 1	
t	00,11,01,10		00,11,01,10	
	00,11,01,10		01,10,00,11	

Table II: K-map realization for transition

X0	X1	Y0	Y1	Type1	Type2	Type3	Type4
0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	0
0	0	1	0	1	0	0	0
0	0	1	1	0	0	0	1
0	1	0	0	1	0	0	0
0	1	0	1	0	0	1	0
0	1	1	0	0	1	0	0
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	0
1	0	0	1	0	1	0	0
1	0	1	0	0	0	1	0
1	0	1	1	1	0	0	0
1	1	0	0	0	0	1	0
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	0
1	1	1	1	0	0	0	1

techniques with the goal of reducing the switching activity and coupling switching activity in between the links [11]. The same sequences of flits are passes through all interconnects which reduces the power dissipation.

Proposed Encoding Scheme: The data encoding techniques are transparent with respect to the NoC fabrication. In encoding scheme there is no modification in links and routers architecture. Transition occurred in on chip interconnection is classified as four types [9]. Type 1 transition occurred when one line switches and the other line unchanged, type 2 transition occurred when one line switches from high to low and other line switches from low to high, type 3 transition occurred when both lines are simultaneously switches and type 4 transition are no changed [12].

Encoding scheme based on inversion on odd bits condition, it consider the total link width of w bits. The header flit is not encoded, the w bits of the input is encoded and passed through link. The last bit indicates whether the odd bit inversion taken place or not. The generic block diagram is shown in Fig. 1. The encoder block E, it is inbuilt into the network interface, is responsible for inversion occurrence. To make the decision the first input flit is compared with previous encoded flit.

The integration of w-1 bits and last one bit is w bit, represent the first input of the encoder. The previous encoded flit is given as a feedback that is the second input of the encoder. The encoder consists of three blocks (i) Transition block (ii) Majority voter (iii) odd bit inversion.

The first (second encoded) input body flit are denoted by X_i (Y_i) where i=0, 1,……,w-2. The last bit of the flit is indicating as 1 when the inversion is taking place otherwise it is indicate as 0 bit [12]. In encoding logic, each Ty block takes the input flits in a two adjacent bits ways (e.g., X1X2Y1Y2, X2 X3Y2Y3….etc).

- Transition: it set the output as 1 when any types of transitions are occurred and the architecture is implemented using the k map realization as shown in Table II.

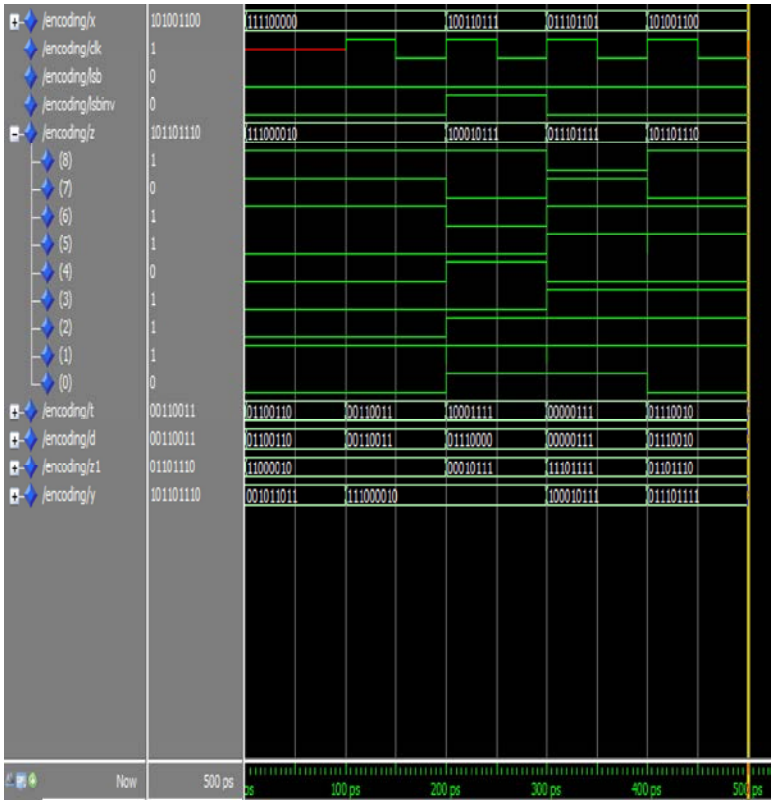

Fig. 2: Simulation of Type 1 Encoder

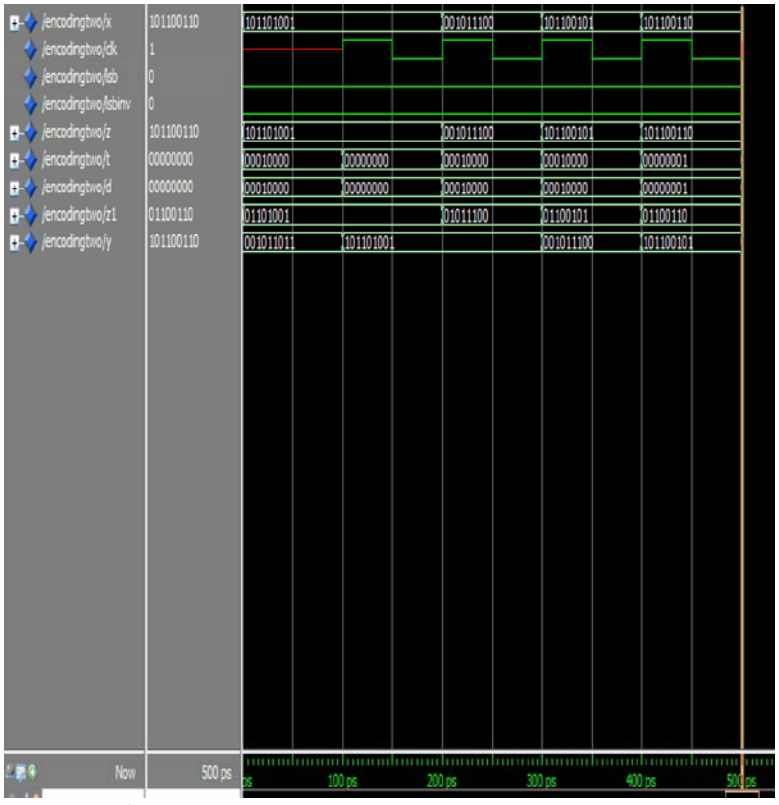

Fig. 3: Simulation of Type 2 Encoder

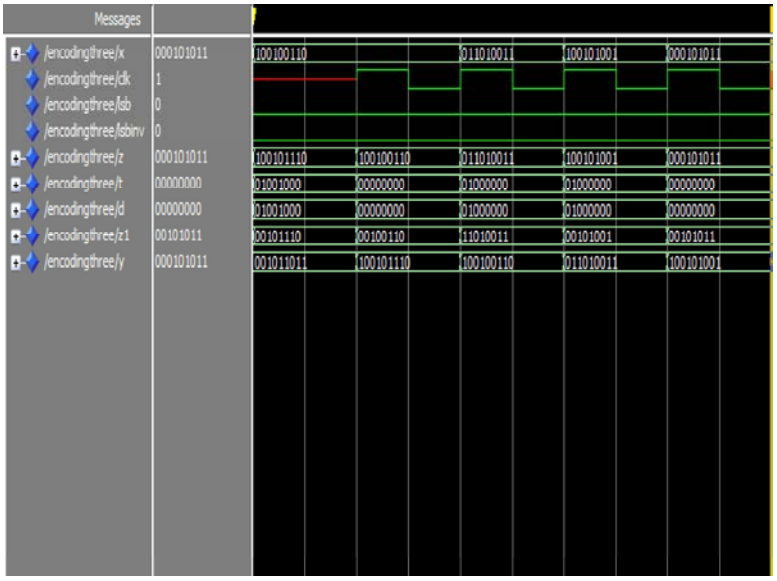

Fig. 4: Simulation of Type 3 Encoder

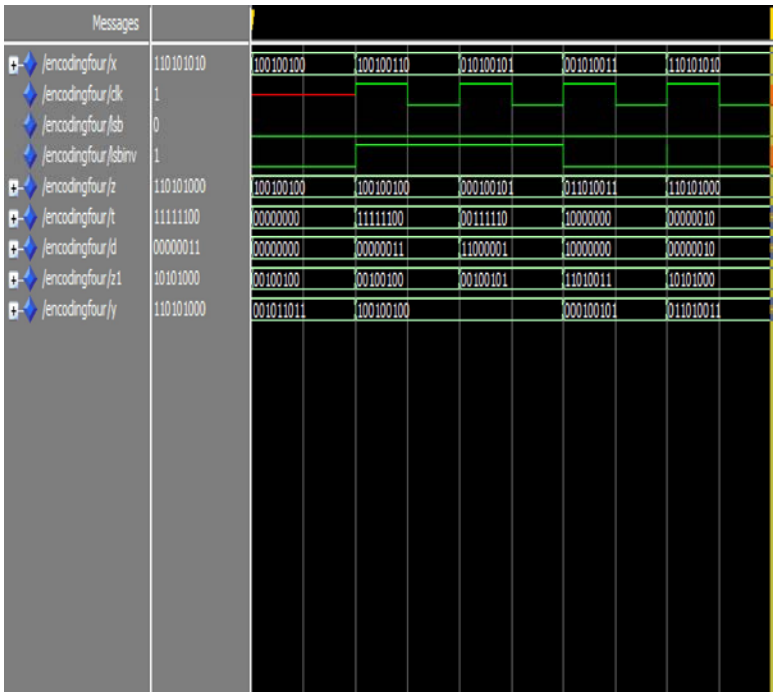

Fig. 5: Simulation of Type 4 Encoder

- Majority voter: it checks the condition (Ty> 0.5 * w-1) and makes the decision whether the complement is needed or not if the complement is taken it is indicated as 1 otherwise 0 in the last bit. The weight is chosen based on the number of transition.
- Odd bit inversion: it compares the first input and majority voter output and it performed the inversion only on the odd bit not on even bits that reduces the number of transition.

Experimental Results: The end to end data encoding technique is simulated and synthesized using ModelSim 6.5e and Quartus II tool and the simulation results for four types of transition are shown in Fig. 2, 3, 4 and 5. The synthesis results for four types of transition are shown in Table III. The packets are encoded and passes through the links except the header flit.

Table III: Comparison Results

Transition types	Power
Type 1	69.22mW
Type 2	69.24mW
Type 3	69.26mW
Type 4	69.27mW

RESULTS AND DISCUSSION

In NoC the overall power dissipation is due to the link power dissipation. The data encoding scheme aimed at reducing switching activity and coupling switching activity which is mainly responsible for link power dissipation. The proposed end to end data encoding scheme takes the benefits of wormhole switching. All types of transition are designed using verilog HDL and synthesized using Quartus II design. The power dissipation is calculated by power play analysis tool. The results shows that the power dissipation of type 1 transition are less compared to other transition types and it saves power dissipation up to 7%. In this encoding technique a significant amount of power dissipation is minimized without any performance degradation.

CONCLUSION

It improves the scalability and power efficiency of system on chip. In NoC the power dissipation in the links is starts to compete with the communication system. The data encoding technique is introduced to reduce the bit level transition occurred in the link, data packets contain more bit transition in the links that leads more power dissipation. Driver and receiver on the bus use the bus invert method to code and decode the information, it reduces the switching activity but the performance is degraded in the NoC.

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