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Low Power Modified Wallace Tree Multiplier Using Cadence Tool

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Abstract: A big obstacle in designingreliable CMOS mixed signal systems with high yields is Process variation; it gives a lot variation in speeding up of the multiplier circuit. In the previous work it has been proved the numerous availability of the multiplier process, where to minimize the variation in voltage gain due to variations in process supply voltage and temperature for common trans-conductance is a tedious task.This in turn gives decreased parasitic capacitance on the dynamic node of the circuit. For the high speed multiplier process we use a 4*4 Wallace tree multiplier designed in Cadence spectre tool of 180nm technology which uses low leakage high speed full adders for the fast multiplication compared to the previous available multiplier schemes from olden days. These full adder uses current comparison based domino logic to achieve low leakage and high speed for our proposed scheme. This shows a relative power reduction when compared to the other multiplier techniques using standard full adders and other technologies. We also present measured results demonstrating that our technique alleviates voltage gain variations caused by supply voltage changes with different power variations and delays. The proposed multiplier consumes power of 0.54 mW.

Key words: Multiplier · CMOS analog integrated circuit · Process compensation · Process variation · Self-biasing

INTRODUCTION

The advancements in multimedia, communication systems and real-time signal processing let to major advantages. The multiplier is an important part of most digital signal processing methods that use nonlinear functions DCTorDWT. As these processors operate by repetitive multiplication and addition, their speed becomes a major factor and determines the performance of the entire calculation. The multiplier operation can be partitioned into 3 stages as follows: i) the first stage, namely Partial Product Generation (PPG), which provides the bit-by-bit multiplication of the multiplicand and the multiplier, ii) the second stage, namely Partial Produce Addition (PPR), which actuates the speed of the multiplier by providing the reduction of partial products and iii) the final stage, namely Carry Propagate Addition (CPA), in which various [n:2] compressors have been employed to achieve lower delay and latency in the high speed multipliers.

To employ the processors for digital signal processing applications, the modified Wallace tree multiplieruses different [n:2] compressors circuits to obtain low power and high speed operation in the Arithmetic Logic Unit (ALU). In digital CMOS design, the effective power-delay product is commonly used to evaluate the value the merits of designs [1].

Array Multiplier is purely based on the shift and add algorithm. By multiplying the multiplicand with one bit of the multiplier the partial products are generated. It is then shifted to the left in the order of the multiplier bit and then the intermediate partial products are added to give the final result as shown in Figure [1].

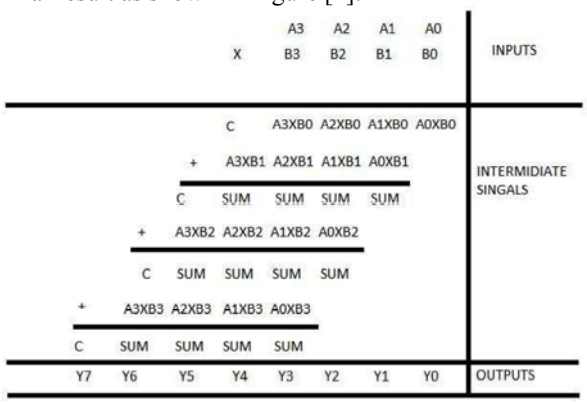

Fig. 1: Basic principle of the 4X4 array multiplier

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Here the LSB of the first partial product becomes the least bit of the product too and the rest of the bits of the partial product are added to the second shifted partial product. The LSB of the addition turns to be the next bit of the product. This process is followed until the last partial product is added to the sum of the earlier additions and the result of this addition are then placed in the product [2].

Since this process takes much time we go for Improved Baugh Wooley multiplier that provides least power, area and delay. The major aim is to implement high-speed, low-power multiplier using add and shift method of Baugh Wooley Multipliers for an efficient process. The restraint of this multiplier is its size. With an increase in the size of the operand, arrays grow in size at a rate equal to the square of the operand size. The large size of full arrays typically prohibits their use, except for small operand sizes and on special purpose math chips where a major portion of the silicon area can be assigned to the multiplier array.

A Wallace tree multiplier is an upgraded version of tree based multiplierarchitecture. Wallace tree multiplier use algorithm of carry save addition to decrease the latency. The proposed modified Wallace tree multiplier is explained in the chapters below.The rest of the paper is organized intofollowing sections. In section II, the background of the multiplier is discussed with various literatures and the Improved Baugh Wooley Multiplier is presented in section III. In section IV the proposed modified Wallace tree multiplier is explained and section V with the simulation results of the modified Wallace tree multiplier is explained. Finally, in section VI the work is concluded.

Literature Survey: BhupenderPratap Singh, Rakesh Kumar. "Design & Implementation 8-Bit Wallace Tree Multiplier", in this paper 8 bit Wallace tree multiplier is proposed. It's found that by using compressor methods, the Speed of Wallace treemultiplier can be improved. For minimizing the number of partial products, halfadder and full adder are used in this Wallace tree multiplication. In this process carry save adder is also used in thelast stage to accumulate the last bits. The main goals attained in this proposed multiplier are the decrease in the area ofmultiplier circuit and increase in the speed of multiplier [3].

P. A. Irfan Khan and Ravi Shankar Mishra, "Comparative Analysis of different Algorithm for Design of High-Speed Multiplier Accumulator Unit (MAC)", in this paper it is stated that the Baugh-Wooley algorithm is comparatively a straightforward way of doing signed multiplications. The Baugh-Wooley multiplier reduces the partial products which are given to the MAC unit. It leads to the low power consumption.By using Baugh-Wooley multiplier the speed of the circuit has been increased and due to pipelining technique the power consumption is also very less as compared to the Wallace tree multiplier. This author also stated that, if it is possible to reduce the power consumption of the Baugh-Wooley multiplier so that the MAC unit speed will increase [4].

G. Shireesha, Dr. G. Kanaka durga, "Design and implementation of Wallace tree multiplier using kogge stone adder and Brent Kung adder", in this paper to perform multiple multiplications on different data pathsthe authors have used a fixed point Wallace tree multiplier architecture. When employing Kogge Stone and Brent Kung adders in the Wallace tree multiplier, more number of multiplications are performed with a burden of fewer extra carry save adder stages. The modified n-bit Wallace tree multiplier structure can be divided into four (n/2) x (n/2) multiplier, two nx(n/2) multiplier and one nxn bit multiplier that are performing multiplication in parallel. Whereas the well-known Carry Look Ahead adder is used in the existing Wallace tree multiplier design. By embodying parallel prefix adders the speed can be improved and the area can be reduced in the proposed Wallace tree multiplier. The Brent Kung (BKA) adder is used to reduce the area and Kogge Stone (KSA) adder is used to increase the speed [5].

I. Hussain, r. K. Sah, m. Kumar, "Performance comparison of Wallace multiplier architectures", this work includes performance comparison review of different Wallace multiplier architectures.At the end of this review it is observed that Wallace multiplier architecture provides better performance in terms of power, delay and area when efficient adders are used [6].

M.Satheesh, D.SriHari, "Design and Implementation Radix-8 High Performance Multiplier Using High Speed Compressors", in this work a Radix-4 Booth multiplier with 3:2 compressors and Radix-8 Booth multiplier with 4:2 compressors are presented. The design is methodizedfor m × n multiplication where m and n can reach up to 126 bits. Carry Look ahead Adder is used as the ultimate adder to enhance the speed of operation. Finally the performance improvement of the proposed multipliers is ratified by implementing a higher order FIR filter [7].

Savita Nair, R.H.Khade, AjitSaraf, "Design and analysis of various 32bit multipliers in an approach towards a fast multiplier",in this paper various multipliersare designed to perform multiple multiplications on different arithmetic units. All the designs are structured for 32 × 32 bit multiplication. The multipliers

compared here are an Array Multiplier, a Modified Booth Multiplier, a Wallace tree Multiplier and also a Modified Booth Wallace tree Multiplier. The results are analysed to find out the fastest multiplier of all the four multipliers [8].

Mani KunnathettuRajee, Tessly Thomas, Alphy Manuel, Anju Rachel Thomas, RiboyCheriyan, "FPGA Implementation of an Efficient High Speed Wallace Tree Multiplier", in this paper Wallace tree multiplication is designed, investigated and evaluated. And it is found that the delay of traditional Wallace tree multiplier can bereducedby using compressor techniques. Here in this paper the Wallace tree is constructed with the help of compressors such as 3:2compressors in the conventional manner. This concludes that the reduction in the delay by that improving the speed of the multiplication can be achieved by minimizing the number of adders used in a multiplier [9].

AparnaV. Kale, Prof. M. D. Patil, "modified booth recoder for efficient add-multiply operator", in this paper the design uses different structured recoding techniques for the implementation of the Modified Booth encoder incorporating in FAM. Apart from the implementation of recoding techniques, the comparison of the existing and the designed Modified Booth recoder is provided [10].

PouyaAsadi, "A New Partial Product Reduction Algorithm using Modified Counter and Optimized Hybrid Network", in this experimentation a new multiplier, using efficient components is proposed. It uses more effective adder cells, that reduce critical path and wiring in compare with Existing architectures. The proposed adder uses fourteen transistors and has modified structure that increases speed and reduces critical path. The partial product reduction step uses an advanced wiring technique that reduces noise and critical path. Presented tree uses less transistor and noise problem in contrast with traditional partial product reduction methods. Final addition uses an improved carry networkto add two final operands very efficiently. This decreases power consumption and reduces delay. It combines ideas of different conventional adders in order to design a new hybrid adder. Proposed multiplier increases speed about 11 percent, decreases transistor count about 12 percent and have less noise problem when comparing with conventional Wallace algorithms and in compare with previous algorithms [11].

Prof. G. D. Dalvi, Miss. Prajakta P. Chaure, "Review on Implementation of a High Performance Multiplier Using HDL",inthisresearch experimentations the authors implementeda high performance multiplier using few techniques which are very essential. Using the essential techniques we will dissipate more power and consume much more area and that resultin the increases in reliability and the performance of the multiplier. In this paper we are using some available operation that will help us to increase overall performance and increasing the reliability [12].

Anna Johnson, Mr.Rakesh S, "High Speed Non Linear Carry Select Adder Used in Wallace Tree Multiplier and In Radix-4 Booth Recorded Multiplier",abrand-newapproach for reduction is proposed in this paper for reducing the area and delay of SQRT CSLA architecture. In this work, the reduction in the number of gates equips as great advantage in the reduction of area and also the delay. The comparison displays that the modified SQRT CSLA has a marginally larger delay, but the area of the 16-b modified SQRT CSLA is significantly reduced respectively. The delay of the proposed design shows a decrease for 16-b sizes, indicating the success of the method. Therefore the modified CSLA architecture is low area, efficient and simple for VLSI hardware implementation. Therefore the modification in XOR gate can further reduces the area whereas no delay is observed by change in XOR gate. Using this regular and modified CSLA in Wallace tree multiplier and radix-4 booth recorded multiplier results in great advantages. High speed multiplication is the specialty of using this CSLA [13].

C.Dhivya, M.Thiruppathi, R.Sowmiya, "Design of 8x8 Wallace multiplier using mux based full adder with compressor", this work provides a comparison between the compressor based Wallace multiplier and the Wallace multiplier with MUX based full adder. Comparative study of the multipliers was done and the results were tabulated. The result shows that the compressor based Wallace multiplier architecture results in better performance in terms of area and speed. The advantage of this work is to design an efficient multiplier with reduced area. The restriction is when the bit size was increased the area will get increased. Hence this work concludes that an efficient method of designing a multiplier is the compressor with MUX based full adder technique [14].

Keshaveni N., "High Speed Area Efficient 32 Bit Wallace Tree Multiplier",this work is area efficient and faster than the existing methods. One of the authors [6] concluded that a 32-bit Wallace tree multiplier consumes a total number of 2704 slice LUTs. Table I shows the comparison of the area of various types of Wallace tree multipliers and delay is compared in Table II for various Wallace tree multipliers. Therefore by comparing these results with the present work, it can be concluded that the present work is faster and area efficient than the existing methods. And also, it is shown that, in the present work,

the time, 5 ns, required for the 32 bit Wallace tree multiplication, is not yet reported in the literature. As a future work, the design can also be focused on floating point multiplication [15].

Jinimol P George and Ramesh P, "Wallace Tree Multiplier using Compressor", in this worka high speed parallel multiplier is efficiently implemented using both these approaches is depicted. In this work the multipliers are designed by using the Radix-8 Booth Algorithm and also the Radix-32 Booth algorithm with various compressors. The number of partial products is n/3 or [n/3+1] in Radix-8 Booth algorithm while it is reduced to n/5 or [n/5+1] in Radix-32 Booth algorithm, with n is the bit-width of the multiplier. This results in reduction of the number of partial products to be added results in increasing the speed of operation. The Carry Save Adders (CSA) is used to efficiently accumulate the partial products which reduce the time as well as the chip area. To further improvement in the speed of operation, the final level uses carry-look-ahead (CLA) adder [16].

Improved Baugh Wooley Multiplier: In this section the modification of multiplier is explained. The height of the longest column is increased by two using the conventional Baugh Wooley Multiplier method, which leads to a larger delay over the carry save adder tree. As shown in Tabular bit form 4.3 and height of the column is 7, demanding a carry save adder level extra. Then remove b4from the fourth column and in the third column b4entries is written, which have four entries and can reduce the extra delay. Thus, the entries in the first column become six with the maximum number of entries.

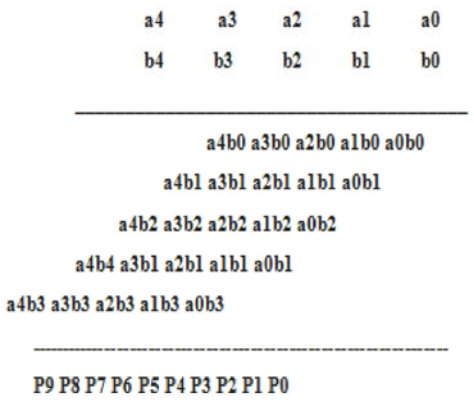


Fig. 2: The Schematic Diagram of a 5-by-5 Improved Baugh-Wooley array multiplier

All weighted negatively a4b4terms can be transferred to the bottom row, which leads to the last row of two with the numbers of two negative, where the operation of subtraction is necessaryfrom the sum of all positive elements. As an alternative of subtracting a4b4 the two's complement can be added b4times. The ImprovedBaugh Wooley algorithm for 5 X 5 bit multiplier is shown in Figure [2] and the schematic diagram shown in Figure [3].

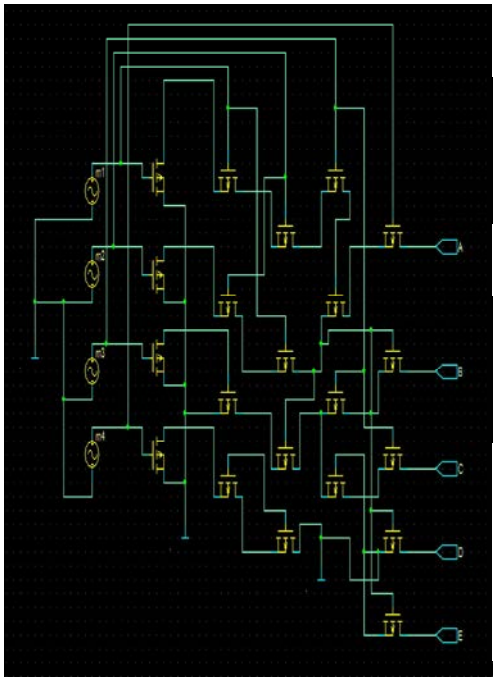


Fig. 3: Schematic Diagram ofImproved Baugh Wooley Multiplier

The multiplier of 5-bit signed was designed and simulated using cadence technology, layout them in Encounter and the analysis of dissipation of average dynamic power is carried out. The Improved Baugh Wooley architecture is 109X faster than array multiplier conventional and 102X faster than Baugh Wooley. Baugh Wooley consumes more power as compared to conventional Baugh Wooley. Further, to reduce the power the proposed design is implemented using latest technological node and precised some of the significant design concepts [17-20].

Here the right structure is selected before optimization of the elaborate circuit. Also, determine the critical timing path through the circuit. The power and speed traded off through circuit sizing choice, supply voltage and transistor thresholds. It can be clear that there is a tremendous possibility in multiplier design of various architectures. The Improved Baugh Wooleythis carry save adder is used for 2's complement signed multiplication. The proposed design is simulated and provides better performance of power reduction and increase the speed.

Proposed Modified Wallace Tree Multiplier: Major limitation of existing multiplier is its size that is its area consumption and power consumption. With an increase in the size of the operand, arrays grow in size at a rate equal to the square of the operand size. The large size of full adder arrays typically prohibits their use in this multiplier, except for small operand sizes or on special purpose math chips in which a major portion of the silicon area will be assigned to the multiplier array. Another problem with array multiplier is that some of the adders in the array are left unutilized.

A fast process for multiplication of two numbers was developed by C.S. Wallace in 1964. He observed that it is possible to find structures which perform the addition operations in parallel manner resulting in less delay and power. We know that Wallace introduced a different way of parallel addition of the partial product bits that uses a tree of carry save adders as an arraywhich is known as Wallace Tree structure. TheWallace tree structure provides an efficient hardware implementation of a digital circuit that multiplies two integers with one another. In order to perform the multiplication of two numbers with the Wallace method, partial product matrix which produces partial product is produced and reduced to a two-row matrix by using a carry save adder and the left out two rows are summed using a fast carry-propagate adder to form the final product.

This advantage becomes more pronounced that the multipliers of bigger than 16 bits will consume large area and produce delay. This tree method increases speed because of the addition of the partial products. In this architecture, all the partial product bits in each column are added together by a set of counters in parallel manner without propagating any carries. Another set of counters is used in the architecture that reduces this new matrix and this process is carried out, until a two-row matrix is generated. Wallace method uses a 3-step process for the multiplication operation.

- Forming Bit Products
- Using a carry-save adder the bit product matrix is then reduced to a 2-row matrix.
- The remaining two rows are summed with a fast carry-propagate adder that produces the final product of the multiplication process.

The block diagram of the proposed Wallace treemultiplier is shown in the figure above.This multiplier uses a Booth encoder that encodes the multiplicand with respect to sign bits. This encoded data is given to the partial product generator and adder array that generates the partial product. Then the partial product is given to the n-bit adder that produces the final product of the given input. It is an efficient digital circuit implementation that multiplies two integers and produces the final product. The Wallace tree has three steps:

- Multiplying each bit of the arguments, by each bit of the other, yielding n^2 results. The wires carry different weights depending on position of the multiplied bits.
  - Then the number of partial products is reducedto two by layers of full and half adders.
  - Then the wires are grouped into two numbers and add them with a conventional adder.

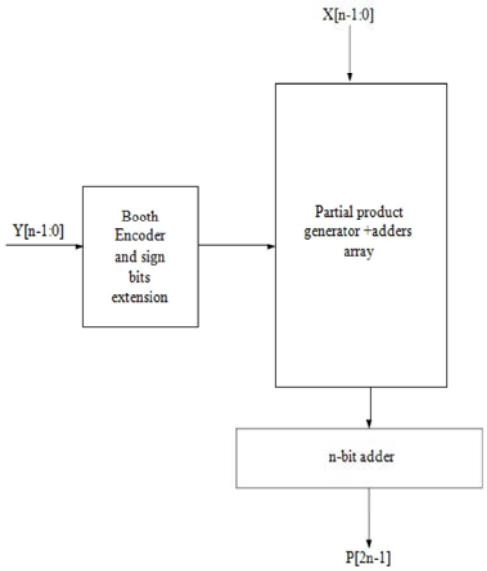


Fig. 4: Block diagram of the modified structure

The second phase works as long as three or more wires are there with thesame weight add a following layer:

- Any three wires are taken with the same weights and input is given to them to a full adder. The result will be an output wire of the same weight for these wires and an output wire with a higher weight for each three input wires.
- Then three may be two conditions, if there are two wires of the same weight, give their input into a half adder.
- If there is just one wire left, connect it to the next layer.

Wallace developed a different way of partial product addition in parallel manner using a tree of carry save adders, known as “Wallace Tree”. Whenperforming the multiplication of two numbers with the Wallace method, partial product matrixwill be reduced to a two-row matrix

by employing a carry save adder and the left out two rows are summed with a fast carry-propagate adder to form the product.

Table I: Truth table of n-bit Adder

INPUTS				CIN=0		CIN=1		
A	B	C	D	CARRY	SUM	CARRY	SUM	COUT
0	0	0	0	0	0	0	1	0
0	0	0	1					
0	0	1	0	0	1	1	0	0
0	1	0	0					
1	0	0	0					
0	0	1	1					
0	1	1	0					
1	1	0	0	0	0	0	1	1
1	0	0	1					
1	0	1	0					
1	1	0	0					
0	1	1	1					
1	1	1	0	0	1	1	0	1
1	1	0	1					
1	1	1	0					
1	1	1	1	1	0	1	1	1

Simulation Results: The proposed Wallace tree multiplier is design in Cadence Virtuoso tool of 180nm Technology. The Booth encoder, partial product generator, n-bit adder are designed separately and are converted into symbols using cell view tool of virtuoso. The symbols of the blocks are interconnected with each other as shown in the block diagram of the proposed multiplier. The block diagram is shown in the figure [4]. The adder circuit that is modified in this multiplier is shown in the figure [5] the schematic design of the adder in the virtuoso tool is shown in the Figure [6].

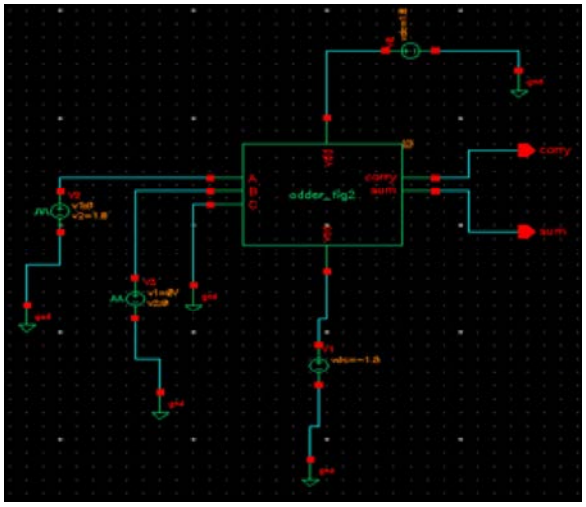


Fig. 6: Adder in the proposed multiplier

The Adder that is modified in the proposed Wallace Tree array multiplier is sketched and created as symbols in the virtuoso tool. Then it is connected with the input source and output. The output is examined to verify the functioning of the adder.

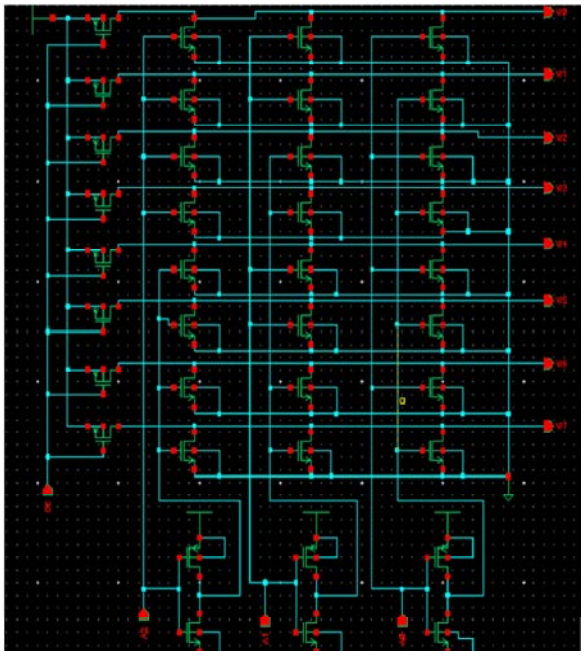


Fig. 7: Organization for eight partial products

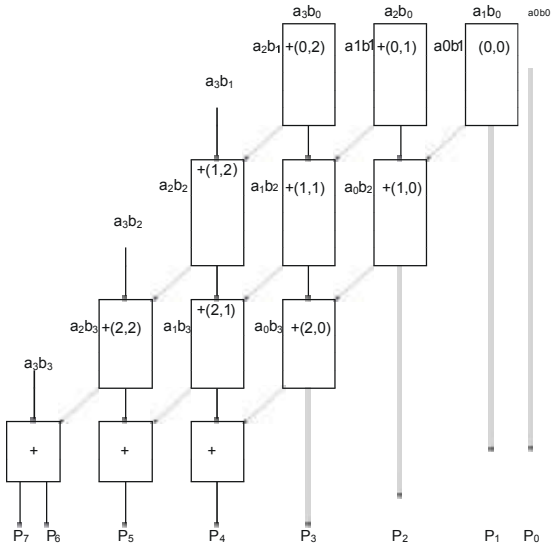


Fig. 5: Adder Array

In the same way the partial product generator is designed as shown in the figure [7]. Then the circuit is converted to symbol and then tested and its output is examined to verify the functionality of the partial product generator.

The circuits are tested and the outputs are got under various testing condition. Initially all the sub-blocks such as Booth encoder, partial product generator, n-bit adder are tested and verified separately. Then the final structure of Modified Wallace tree is tested and verified. The Transient analysis output of the proposed multiplier is shown in the figure [9]. Here in the figure the multiplier is tested with the sinusoidal signal input and the output is verified. Then the multiplier is tested with the pulse signal and the output is verified. The transient analysis of the proposed multiplier with pulse input is shown in the figure [10].

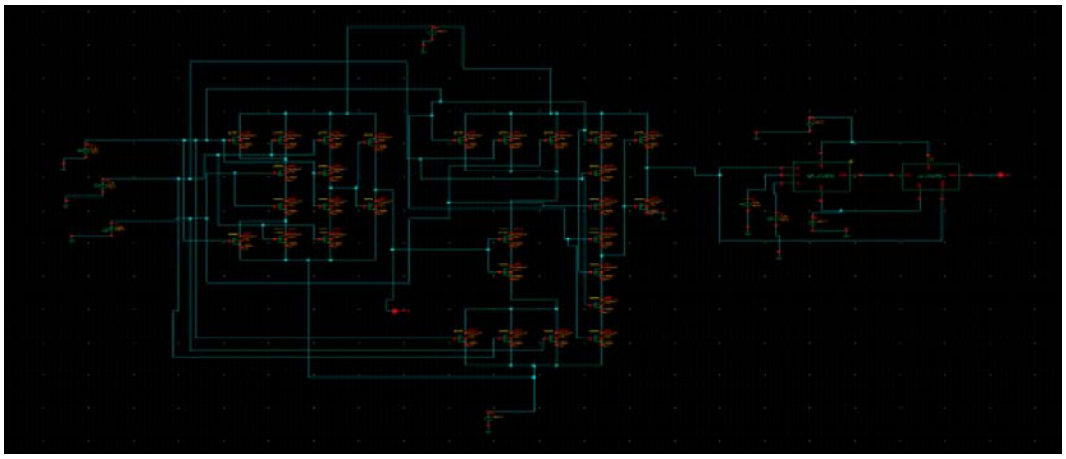


Fig. 8: n*n modified Wallace tree structure

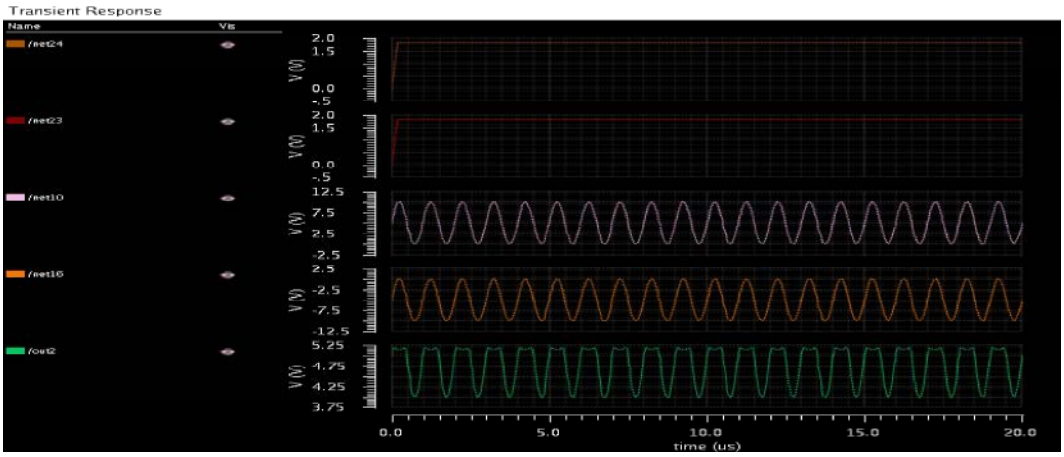


Fig. 9: Transient analysis of the proposed multiplier

Fig. 10: Transient analysis of the proposed multiplier with pulse input

The DC analysis is also carried out to the multiplier to verify its performance, the analysis of the multiplier is shown in the figure [11]. Then the analysis of the circuit that is carried out to measure the output voltage output of the circuit. This transient analysis is shown in the figure [12].

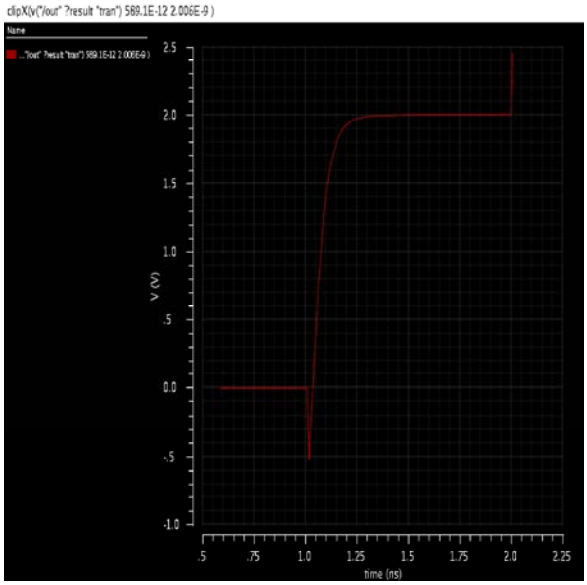


Fig. 11: DC analyses

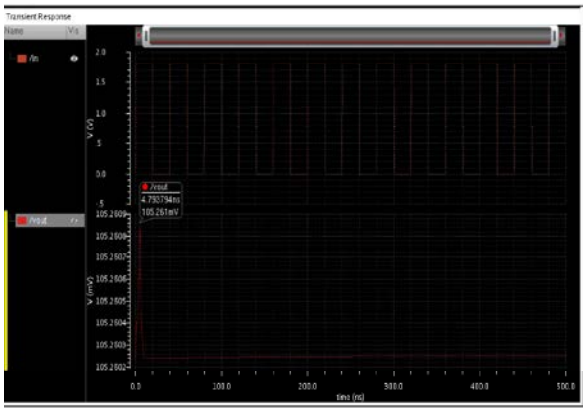


Fig. 12: Transient analyses

Then the power analysis of the proposed Wallace tree multiplier is carried out. The power analysis results in the power consumption of 0.54 mW. This power analysis is shown in the figure [13]. The power is the main cause of the multiplier circuits which is reduced to minimum of 0.54 mW that makes this multiplier effective that of the existingmultipliers. Then the Area consumption and number of buffers used by the proposed multiplier is calculated using Cadence spectre tool of 180nm.

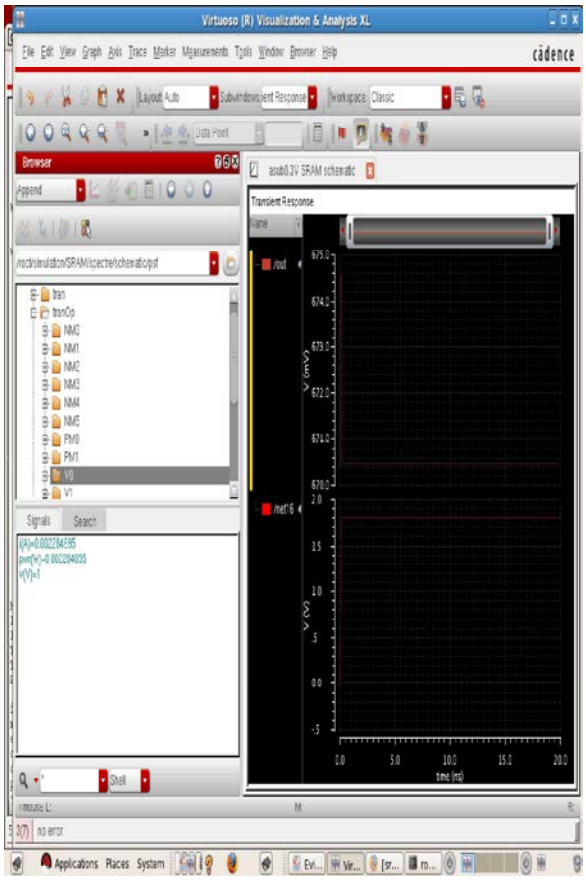
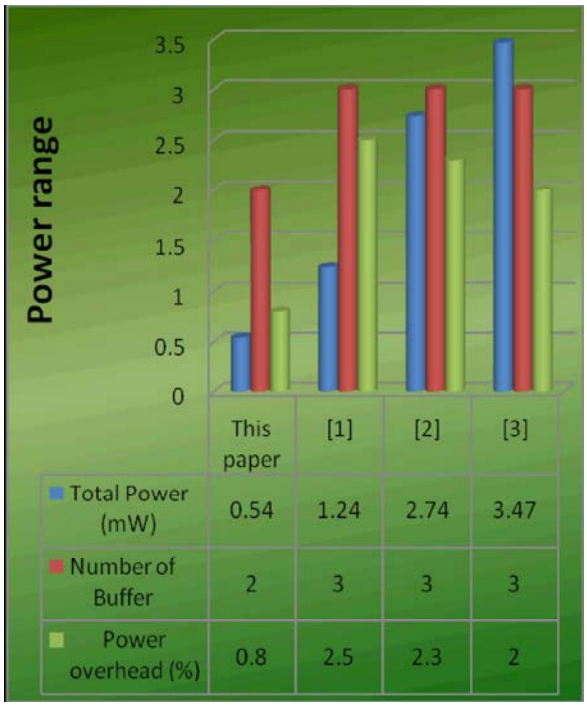


Fig. 13: Power analysis

Finally the parameters of proposed multiplier is compared with the existing multiplies and found efficient. The tabulation the parameter comparison is shown in the Table [II]. The chart comparison of the power consumption of the proposed multiplier with other existing multiplier is shown in the figure [14].The layout design is done in an effort at valuing the multiplier area. Designs were entered using Cadence RTL compiler and Encounter planning of floor, powerand routing is carried out.The Cadence Virtuoso is used for pre layout and simulation of post layout is executed using the NCSU AMI06 CMOS technology.

Table II: Parameter comparison

	Total Power (mW)	Area mm^2	Number of Buffer	Power for every clustering
Proposed Multiplier	0.54	20	2	0.8
[1]	1.24	32	3	2.5
[2]	2.74	33.4	3	2.3
[3]	3.47	34.5	3	2.0



	This paper	[1]	[2]	[3]
Total Power (mW)	0.54	1.24	2.74	3.47
Number of Buffer	2	3	3	3
Power overhead (%)	0.8	2.5	2.3	2

Fig. 14: Power comparisons

CONCLUSION

In this research work a modified Wallace tree multiplier is proposed with the modification in the adder block of the circuit. Here the multiplier is designed with the Booth encoder, partial product generator, n-bit adder. This multiplier gives the optimum results and is verified with the simulation results.The power consumption of this multiplier is found to be of 0.54mW and it is the minimum power consumption than that of the existing multipliers. This n*n modified Wallace tree multiplier produce the efficient output with the modified n-bit Adder circuit at the last stage of the process. This modified n-bit adder works better than that of the CSLA adder used in the existing. In spite of the modification in adder circuit the proposed multiplier consumes less area of 20mm^2. In future this multiplier can be further modified in several blocks such as encoder and partial product generator in order to make the multiplier circuit even more efficient and effective.

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