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A Novel Design for Testability of Multiple Precharged Domino CMOS Circuits

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Abstract: In this paper a novel multiple precharge design scheme has been proposed that makes the domino circuits testable with respect to transistor stuck-open and stuck-on faults. Albeit domino CMOS circuits are sensitive to parasitic effects such as charge sharing, which cause the redistribution of charge between dynamic node and parasitic capacitances of internal nodes. The prime solution of above problem is to use secondary transistors to precharge the internal nodes of the domino circuits during precharge phase. However, these extra added transistors are not readily testable for stuck-open faults. Undetected stuck-open faults affect the consistency of the circuit. The circuits are simulated in HSPICE using TSMC 0.18-μm CMOS technology for the Design for Testability (DFT). The simulated results of proposed circuit are promising in terms of testability as compared to reported circuits.

Key words: Design for testability . Domino CMOS . noise margin . stuck-at faults . ATPG

INTRODUCTION

Domino CMOS circuits falls under the category of Dynamic CMOS logic, which gives advantage in terms of testability over static CMOS circuits [1]. The inherent problem with Domino CMOS circuit is that it suffers from noise margin problem due to charge redistribution between parasitic capacitances at the internal nodes of the circuit, which may result false output [2]. Domino is nonratioed logic with faster switching speed and less silicon area required as compare to the full static CMOS logic [3-5]. Due to this characteristic Domino circuits have been usually used in high performance critical circuits for example CMOS microprocessors [6-9]. Domino logic consists of a single clock, which is used to precharge the dynamic node of the circuit in precharge phase and to evaluate the function made by NMOS network in evaluation phase. During the precharge phase (Clock = 0) the internal node F' (dynamic node) is charged to high (logic 1) through the PMOS MCP and thus output is discharged to low (logic 0). During evaluation phase (Clock = 1) the function is evaluated through the pull down network consists of NMOS transistors only. During the evaluation phase the transition of node F (F') can be low (high) depending upon the input conditions. During evaluation phase the Dynamic node F' may be left floating if pull down network (PDN) is in open state, which results in charge leakage from dynamic node F' due to leakage currents. This problem can be overcome by use of keeper transistor [10].

Charge Sharing take place in evaluation phase, when overall NMOS network is in open state, but some of its input make transition from low logic to high (i.e., $0 \rightarrow 1$) and turn-on few transistors. This results in redistribution of charge stored on dynamic node over internal parasitic node capacitances. This problem can be overcome by using secondary precharge transistors.

The transistor stuck-on or stuck-open faults are usually caused by physical failure that results in either conducting or nonconducting state of a transistor are modeled by the transistors stuck-on (TSON) and transistor stuck-open (TSOP) faults, respectively [11]. Domino CMOS logic is more readily testable as compare to full static CMOS. Full static CMOS logic requires two test patterns to detect a single TSOP fault, the first test vector is initializing vector and second to test the TSOP fault. This test procedure may fail due to circuit delays. While in the case of Domino logic circuit most of the TSOP faults can be detected by using only single test vector, which cannot be invalided due to arbitrary signal delay. This remains valid in the case of multiple faults in the circuit [12-14]. The TSON faults can be detected by using current monitoring techniques, but in case of CMOS it's not appropriate as we goes into deep submicron technology, while in case of domino logic most of the TSON faults can be detected by using logic tests.

Let us consider the Fig. 1, in the precharge phase the voltage on C1 (V_{c1}) is VDD, at the time of evaluation phase only transistor MN11 is ON and transistors MN21, MN22, MN23 are OFF. It will be

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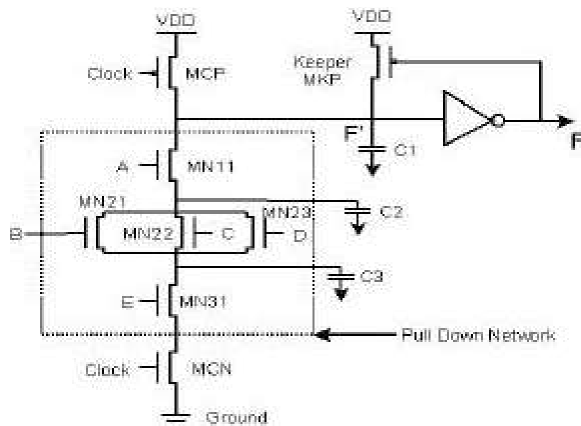


Fig. 1: Standard domino CMOS circuit

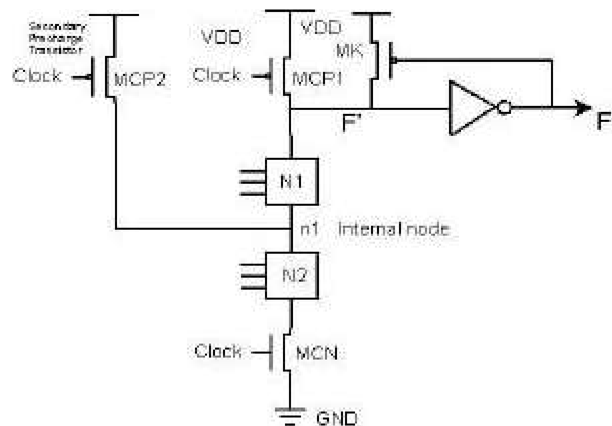


Fig. 2: Standard multiple precharge domino CMOS circuit

result in the distribution of charge stored on C1 over C2 via transistor MN11, which in turn may change the logic level at node F' and output F. The most effective approach to overcome this problem is to precharge the critical internal nodes of the circuit to VDD during precharge phase with the help of secondary precharge transistors as shown in Fig. 2.

In Fig. 2 transistor MCP2 is used as secondary precharge transistor, which charges the internal node n1 to VDD in the precharge phase. The TSON fault at transistor MCP2 can be detected by applying current monitoring techniques, while the TSOP fault is not testable.

In this paper we have proposed a novel multiple precharging designs to overcome undetected TSOP fault problem. The testability issue has been reported to solve the undetected TSOP problem associated with secondary precharge transistors [15].

TESTABLE REALIZATIONS OF DOMINO CMOS LOGIC

Domino CMOS circuits enjoy area, delay and testability advantages over static CMOS circuits. The area advantage comes from the fact that the PMOS network of a domino CMOS gate consists of only one transistor. This also results in a reduction in the capacitive load at the output node, which is the basis for the delay advantage. The testability advantage will become obvious because most of the stuck-open and stuck-on faults requires only single test vector. The term permanent fault refers to the presence of a fault that affects the functional behavior of the circuit permanently. Digital circuits have the property that the domain of values of the input and output signals is binary (logic 0 or logic 1) [1].

To test a domino logic circuit it will be helpful to develop a gate level model of that circuit. It helps to generate gate-level test patterns, which can be used to detect faults. A gate-level model for a domino CMOS circuit can be obtained by NMOS network, just by replacing the series connections by AND gate and parallel connection by OR gate. For example in Fig. 1 the transistors MN21, MN22, MN23 are in parallel so that can be modeled as three input OR gate and these three along with MN11 and MN31 are in series modeled as three input AND gate, with inputs A, E and output of OR gate. There is no need to model inverter because the inversion produced by domino logic is cancelled by the inverter. Similarly clocked transistors & keeper transistors need not to be modeled separately. The faults present on these transistors can be detected by the test vectors we get for the gate-level circuit.

All single transistor stuck-open faults (TSOPFs), transistor stuck-on faults (TSONFs) and stuck-at faults (SAFs) in domino CMOS circuit can be tested by simply deriving a test set for all single SAFs in its gate-level model.

A stuck-at 0 fault at the input of any transistor in the pull down network (PDN) is equivalent to TSOP fault at that transistor, while stuck-at 1 fault is equivalent to TSON fault. Therefore we can detect all single TSOP and TSON faults in the NMOS network (N1 & N2) in the evaluation phase along with stuck-at faults at the dynamic and output node by generating test patterns by any ATPG tool for corresponding gate-level model.

A TSOP fault at the clocked NMOS (MCN in Fig. 2) can be modeled as a stuck-at 1 at node F' or stuck-at 0 at output F. Likewise, a TSOP fault at the clocked PMOS (MCP1 in Fig. 2) can be modeled as a stuck-at 0 at node F' or stuck-at 1 at node F. Similarly TSOP fault at the PMOS of the inverter is equivalent to stuck-at 0 at node F. A TSOP at NMOS of inverter will result in stuck-at 1 at node F and it needs two vectors to

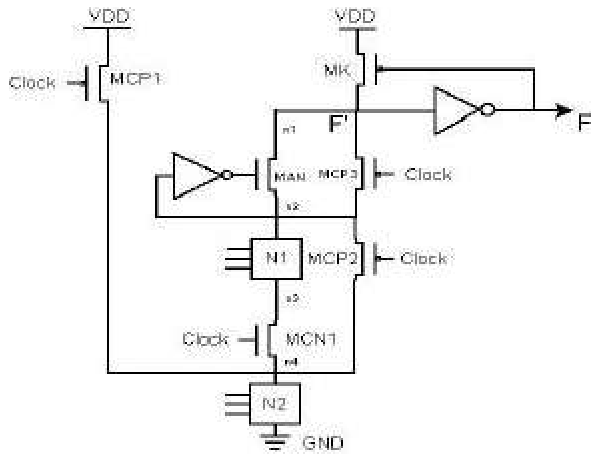


Fig. 3: Proposed multiple precharge domino CMOS circuit

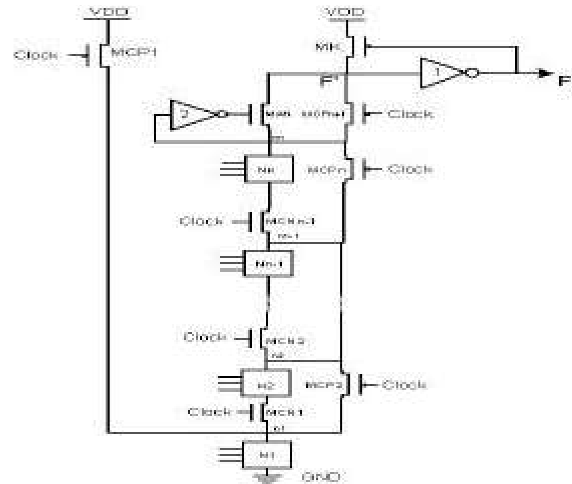


Fig. 4: Generalize circuit for proposed design

detect this fault by mean of 1 to 0 transitions at node F. First (initialization vector) is to make node F at logic 1 and second (test vector) is to make transition from logic 1 to logic 0 at node F. In the same way a TSOP fault at the clocked PMOS transistor (MCP1) can be detected.

The TSON fault for the transistors in the inverter can be detected by using current monitoring techniques. Likewise TSON fault for primary precharge transistor (MCP1 in Fig. 2) can be tested with current monitoring. Finally, a TSON fault at the clocked NMOS transistor is not robustly testable but it is not harmful for the functionality or the noise margins of the circuit and can be omitted.

In case of keeper transistor (MK) and secondary precharge transistor (MCP2) TSOP faults are not strongly testable. The TSON fault at secondary precharge transistor (MCP2) can be detected using current monitoring techniques, while in case of TSON fault at keeper transistor (MK) it will not be an efficient technique, because the keepers are weak transistors.

Next section will present a new multiple precharge scheme to detect the TSOP and TSON faults associated with the Secondary Precharge transistor and improve the overall testability of Domino CMOS circuit.

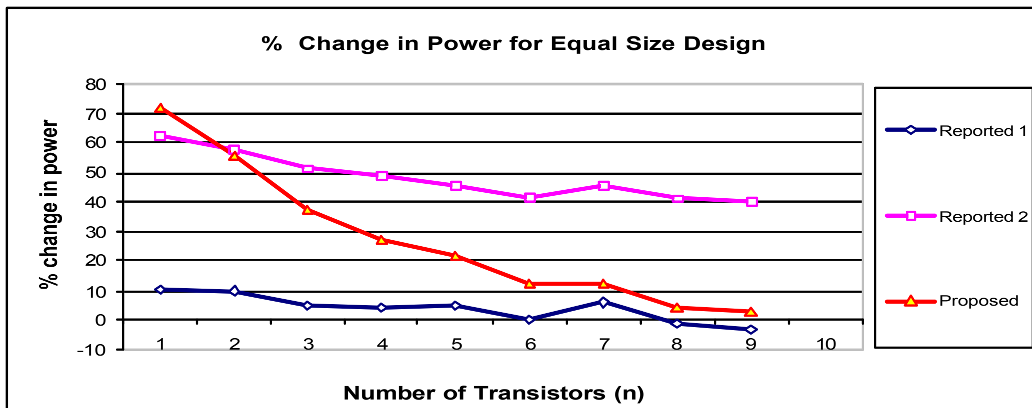
A NOVEL TESTABLE MULTIPLE PRECHARGE TECHNIQUE

To overcome the fault detection problem associated with the secondary precharge transistors we are making a chain of PMOS transistors starting from VDD, passing through critical internal nodes and ending at the dynamic node F'. Along with this we are shifting up the position of clocked NMOS (MCN in Fig. 3) and placing it in between two NMOS blocks. We are also adding one activation NMOS (MAN in Fig. 3) with one inverter as shown in Fig. 3. It will help to overcome the test invalidation problem associated with previously published scheme [15].

In the fault free case the precharging of internal nodes and the dynamic node F' is done through MCP1 and MCP2 and MCP3 shown in Fig. 3. A TSOP fault at any of the precharging transistors (i.e. MCP1, MCP2, MCP3) can be detected using a pair of test vectors, first vector (initializing vector) to set node F' to logic 0 that is both network N1 and N2 must be ON (Conducting state) in the evaluation phase and second vector (test vector) to set node F' to logic 1 (VDD) that is network N1 is OPEN (Nonconducting state) and N2 is ON (Conducting State) in the evaluation phase of test vector. If fault is present in any of the clocked PMOS node F' will not precharge to logic 1 (VDD) and remains low and the fault is detected.

The gate level model for the Fig. 3 will be same as for Fig. 2 as explained earlier. To generate the test patterns we used TetraMax (ATPG) Tool. First initialization vector can be derived by an ATPG for a stuck-at 0 fault at the gate output node F, while second test vector can be derived for a stuck-at 1 fault at one of the inputs of N1 network at the logic gate-level model. The TSOP faults at activation NMOS and clocked NMOS can be detected by vectors which is used for stuck-at 1 fault at F' or stuck-at 0 fault at F.

To detect TSON fault at clocked PMOS transistor MCP1 we need a single vector that lets network N2 in conducting state during evaluation phase and apply current monitoring techniques. Similarly TSON fault at transistor MCP2 can be detected by a single vector that sets network N1 to a nonconducting state and network N2 to a conducting state during the evaluation phase. The test vector for this fault can be generated as a stuck-at 1 fault at any one of the input of network N1.



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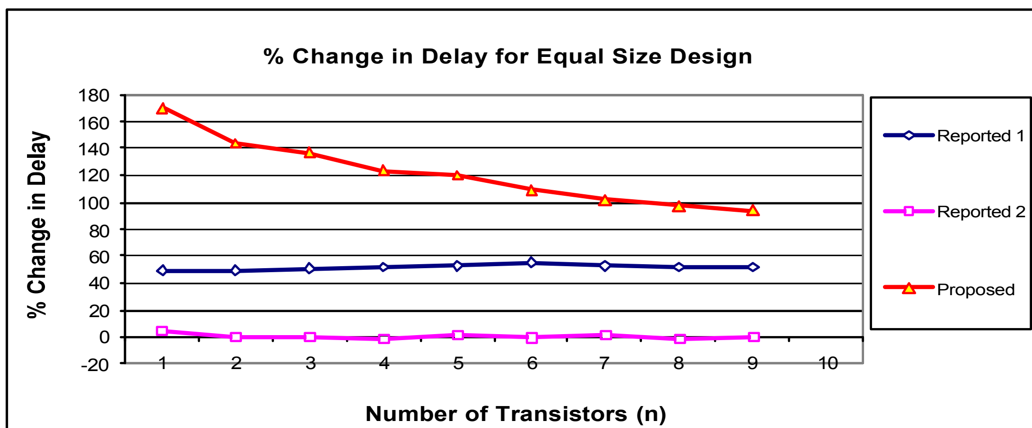

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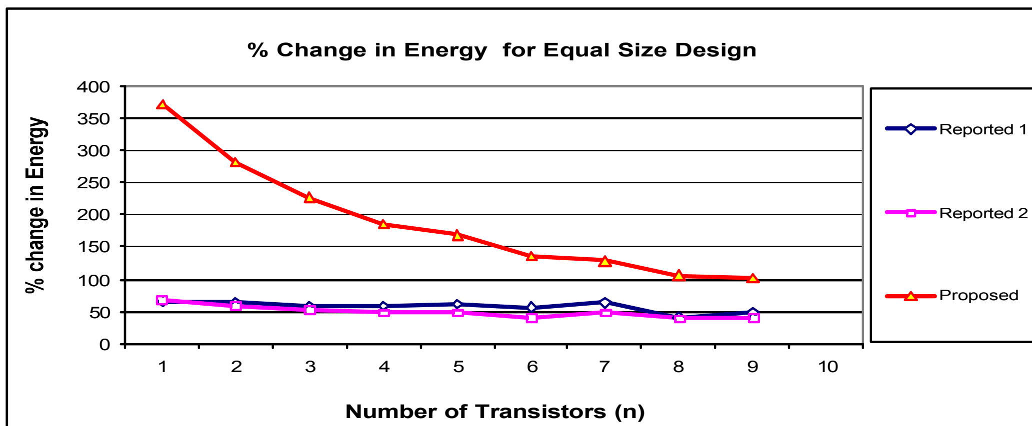


(c)

Fig. 5: Percentage changes for equal size design with respect to circuit in Fig. 2

The TSON fault at MCP3 is undetectable but it's not harmful from the functionality point of view. The TSOP and TSON fault detection for transistors of second inverter is same as for first inverter except the fact that TSOP fault at its NMOS is undetectable, but it will not affect the overall functionality of the circuit. TSON faults at activation transistor (MAN) and clocked transistor (MCN) is not robustly testable, but these will not affect functionality of the transistor. Rest of the transistors for TSOP and TSON faults can be detected as in standard Domino circuit.

The generalize circuit diagram of the proposed circuit is shown in Fig. 4. The rule is that the internal nodes those connected to the source of clocked NMOS

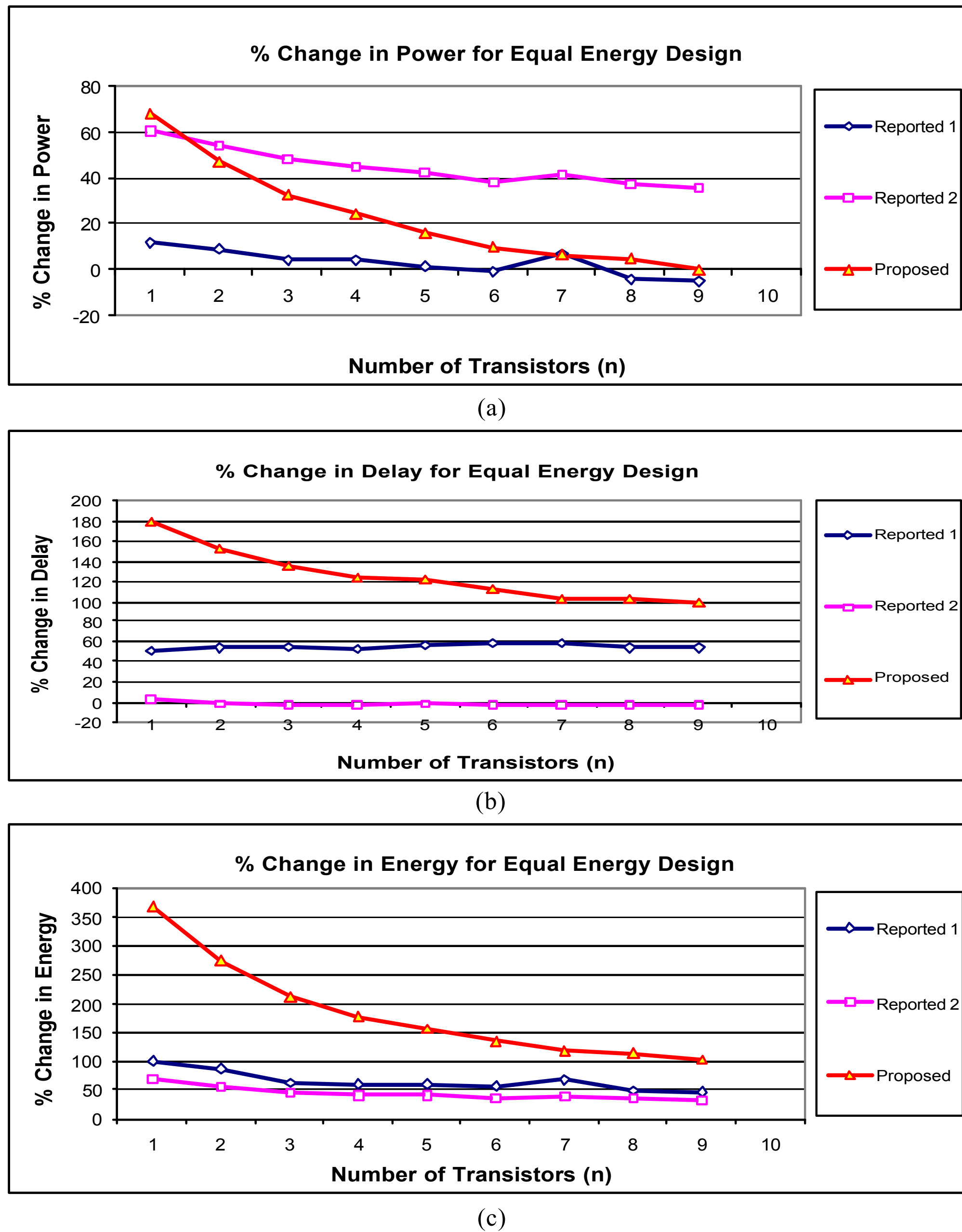


Fig. 6: Percentage changes for equal energy design with respect to circuit in Fig. 2

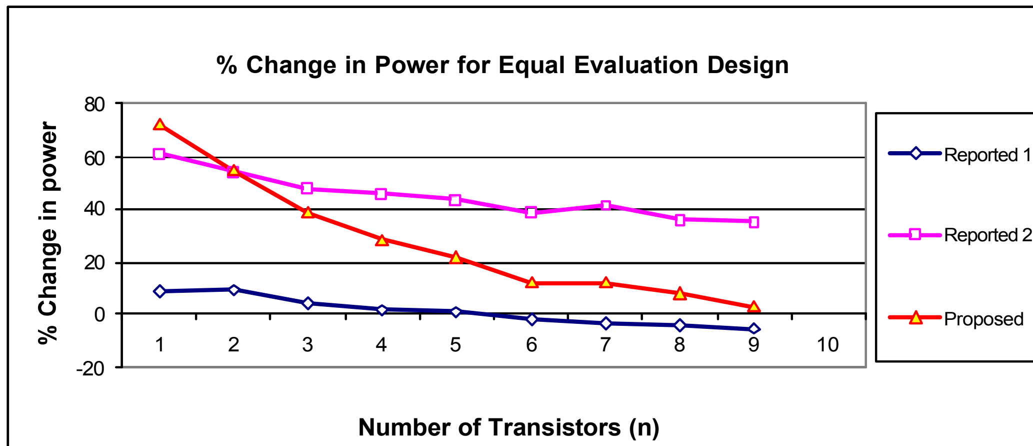
transistor should be precharged through a chain of clocked PMOS transistors. The gate level circuit diagram consists of realization of all NMOS network (OR gate) and output of each gate will feed to an n-input AND gate. The testing procedure will be same as explained above for Fig. 3.

SIMULATION RESULTS AND DISCUSSION

All the circuits are simulated in HSPICE using TSMC 0.18-µm CMOS technology (MOSIS) for Design for Testability (DFT). The W/L ratios for standard circuit are shown in Table 1.

The proposed circuit (Fig. 3) along with standard multiple precharge circuit and two reported circuits [15] are simulated for the following configuration: Equal sized transistors, Equal energy dissipation per cycle and Equal Evaluation delay times.

The percentage change in power, delay and energy with respect to standard multiple precharge domino circuit for proposed circuit and reported circuits [15] for above three configurations are shown in Fig. 5. For



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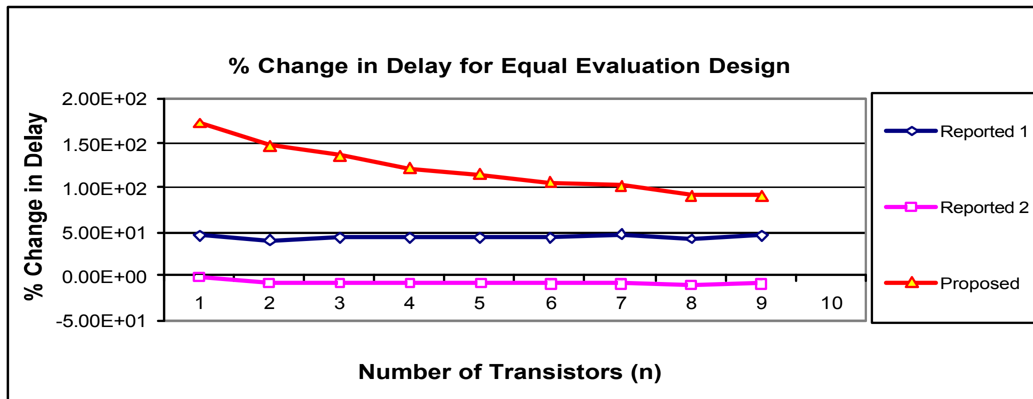

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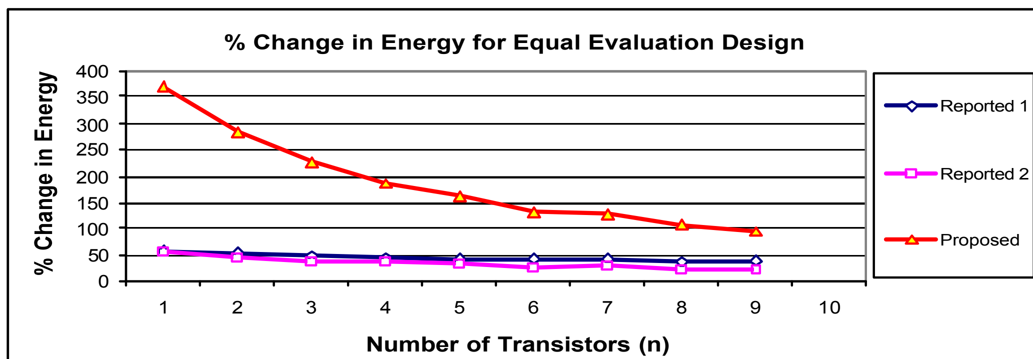

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Fig. 7: Percentage changes for equal evaluation delay time with respect to circuit in Fig. 2

Table 1: W/L ratios for various transistors

Standard Circuit	W / L Ratio (µm / µm)
Precharge transistors	0.70/0.18
Network N1	0.35/0.18
Network N2	0.39/0.18
Keeper transistor	0.27/0.18
Clocked NMOS	0.43/0.18
Inverter PMOS	0.81/0.18
Inverter NMOS	0.35/0.18

equal size transistors with respect to standard multiple precharge design as the number of transistor in each NMOS network increases from two to ten the percentage increase in power, delay and energy in first reported circuit is vary from + 10.5%to-3%, 50% to 52% and 65% to 41% respectively.

In case of second reported circuit the percentage increase in power, delay and energy is vary from 63% to

40%, +4% to-3% and 69% to 40% respectively. In case of proposed scheme the percentage increase in power, delay and energy is vary from 72% to 3%, 171% to 94% and 371% to 101% respectively.

The percentage change in power, delay and energy with respect to standard multiple precharge domino circuit for proposed circuit and reported circuits [15] for Equal Energy Design is shown in Fig. 6.

For equal energy dissipation per cycle with respect to standard multiple precharge design as the number of transistor in each NMOS network increases from two to ten the percentage increase in power, delay and energy in first reported circuit is vary from +12% to-5%, 51% to 54% and 995% to 47% respectively.

In case of second reported circuit the percentage increase in power, delay and energy is vary from 61% to 36%, +3% to-3% and 66% to 32% respectively. In case of proposed scheme the percentage increase in power, delay and energy is vary from 68% to 0.4%, 178% to 100% and 367% to 101% respectively.

The percentage change in power, delay and energy with respect to standard multiple precharge domino circuit for proposed circuit and reported circuits [15] for Equal Evaluation Delay Time Design is shown in Fig. 7.

For equal evaluation delay design with respect to standard multiple precharge design as the number of transistor in each NMOS network increases from two to ten the percentage increase in power, delay and energy in first reported circuit is vary from +9% to-5%, 45% to 40% and 58% to 36% respectively.

In case of second reported circuit the percentage increase in power, delay and energy is vary from 61% to 35%,-9% to-5% and 60% to 24% respectively. In case of proposed scheme the percentage increase in power, delay and energy is vary from 72% to 2.9%, 173% to 90% and 370% to 96% respectively.

CONCLUSION

The simple design for testability technique for multiple precharge Domino CMOS circuits has been proposed. The design is capable to overcome the charge sharing problem with improved testability with reference to TSOP and TSON faults. The test vectors were obtained by ATPG tool for all stuck-at faults at the gate level of corresponding circuit. Domino CMOS circuits are fast as compare to full static CMOS circuits and hence suitable for fast and critical circuit applications like microprocessors.

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