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A New Mixed Gate Diffusion Input Full Adder Topology for High Speed Low Power Digital Circuits

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Abstract: This paper mainly presents Mixed Gate Diffusion Input Full Adder based on static CMOS inverter topology. In this proposed mixed Full Adder topology, GDI Full adders are followed by inverters in the long Full Adder chain to improve the performances as compared to conventional single topology Full adder chain. For any circuits reducing the speed and power dissipation are the important constraints. By changing the number of full adders between two consecutive inverters the delay, the dynamic and leakage power dissipation can be optimized. Delay and power has been evaluated by HSPICE simulation using TSMC 0.35µm and 0.18µm CMOS technologies considering minimum power design. The simulation results reveal better delay and power performance of proposed mixed full adder topology as compared to existing mixed Full Adder topologies at both 0.35µm and 0.18µm CMOS technologies.

Key words: Full adder . gate diffusion input . mixed topology . high performance . VLSI

INTRODUCTION

The performance of the complex logic arithmetic circuits is affected by the individual performance of the Full adder circuits that are reported in the literatures [1, 2]. Therefore, careful design and analysis is required for Full adder circuits. The overall speed of the arithmetic circuit is derived by the speed performance of the Full Adder block. So delay (input carry to output carry) of long Full Adder chain is required to be minimized. Most of the VLSI applications, such as digital signal processing, image and video processing and microprocessors [3], extensively use arithmetic operations which requires very high speed carry computation [4, 5]. The examples of the most commonly used arithmetic operations are addition, subtraction, multiplication and accumulate, etc. In every Full Adder chain, a critical path exist which is shown as gray line in Fig. 1. This critical path signifies that the worst case propagation delay is to be determined from input carry to output carry in the chain. In conventional single topology long full Adder chain, same types of Full Adders are cascaded such as the carry output of one block is connected to carry input of next stage. Thus, enhancing its performance is critical for enhancing the overall module performance. The design should also have a lesser number of transistors to implement Full Adder circuits. The most important performance parameters for future VLSI systems are speed, power consumption and area.

CONVENTIONAL HIGH SPEED SINGLE FULL ADDER TOPOLOGIES

There are two types of single Full Adder topologies depending upon driving/ non-driving capability of the Full Adders. In full adders with driving capability input and output are decoupled e.g. Mirror Full Adder [6] shown in Fig. 2(a) while in full adders without driving capability input and output terminals are not decoupled such as Transmission Gate (TG) [7] and Gate Diffusion Input (GDI) Full Adders shown in Fig. 2(b) and 2(c) respectively because there is no inverter connected at the output side.

A TG Adder is a faster one with lower power dissipation only when used in small chain. But when it is cascaded to form a long chain, its high speed performance is degraded due to lack of driving capability of TG FA.

A GDI cell is a lowest power design technique found in literature [8]. This design can implement a wide variety of logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to TG and Mirror Full Adder), while improving logic level swing and static power characteristics and allowing simple top-down design by using small cell library [9]. To have a look on the working of GDI Full Adder before and after application of inverter for all possible combination of inputs is shown in Table 1 and 2, respectively.

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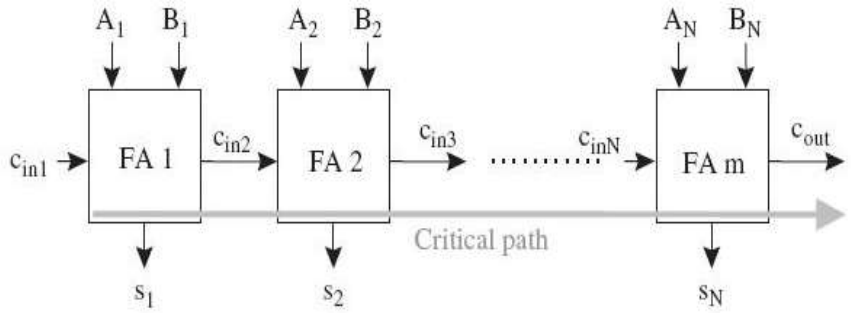

Fig. 1: Critical path in full adder chain

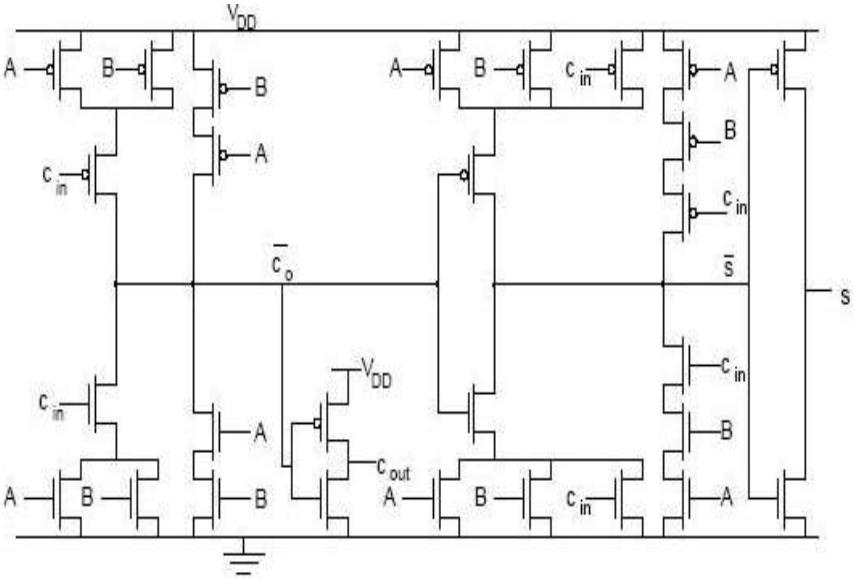

Fig. 2(a): Mirror full adder

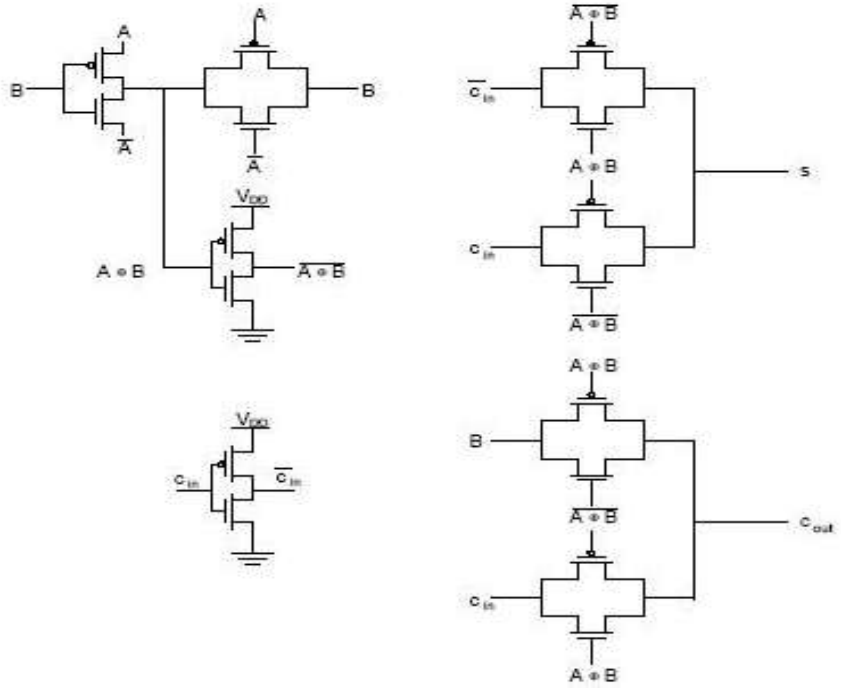

Fig. 2(b): Transmission gate full adder

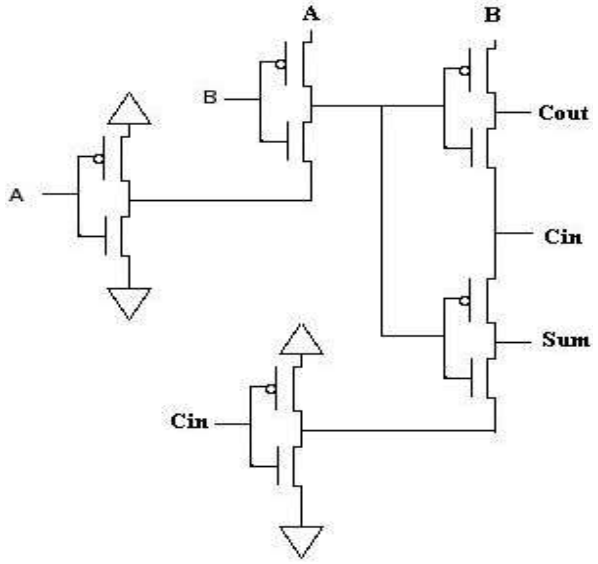

Fig. 2(c): Gate diffusion input full adder

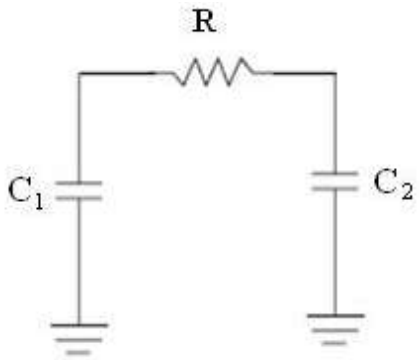

Fig. 3: RC equivalent of GDI full adder

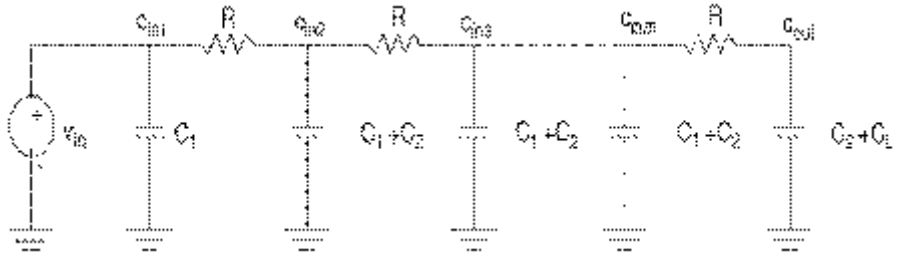

Fig. 4: RC equivalent of GDI FA chain

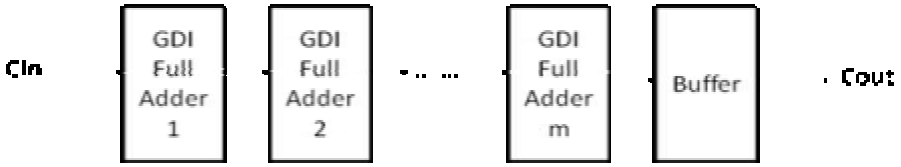

Fig. 5: Mixed GDI full adder based on inverter topology

Table 1: Truth table of GDI adder before application of inverter

Inputs		Output	
A	B	Sum	Cout
0	0	Degraded	Degraded
0	1	Degraded	Degraded
1	0	Full swing	Full swing
1	1	Full swing	Full swing

Table 2: Truth table of GDI adder after application of inverter

Inputs		Output	
A	B	Sum	Cout
0	0	Full swing	Full swing
0	1	Full swing	Full swing
1	0	Full swing	Full swing
1	1	Full swing	Full swing

Table 3: Comparison of different single full adder topologies using 0.35µm CMOS technology

Full Adders	Delay (ps)	Power (µw)	PDP (fJ)
GDI FA	4.19	2.57	0.010
TG FA	5.18	1.82	0.094
Mirror FA	111.50	10.00	0.111

Table 4: Comparison of different single full adder topologies using 0.18µm CMOS technology

Full adders	Delay (ps)	Power (µw)	PDP (fJ)
GDI FA	1.943	0.682	0.001
TG FA	3.815	0.784	0.003
Mirror FA	76.410	2.180	0.166

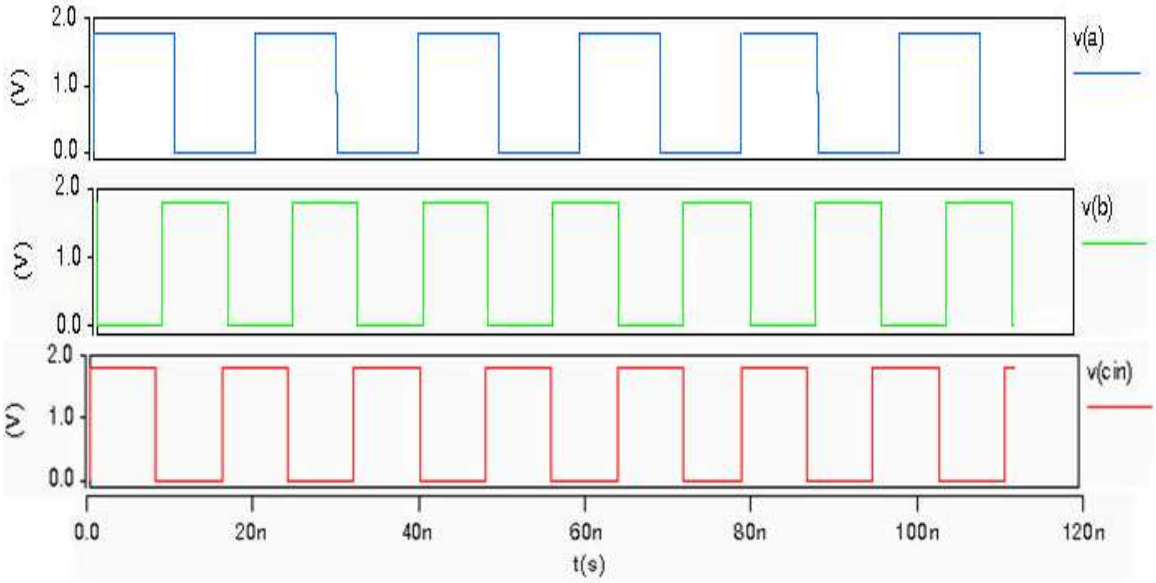

Fig. 6 (a): Timing Input waveforms for mixed GDI full adder based on inverter topology

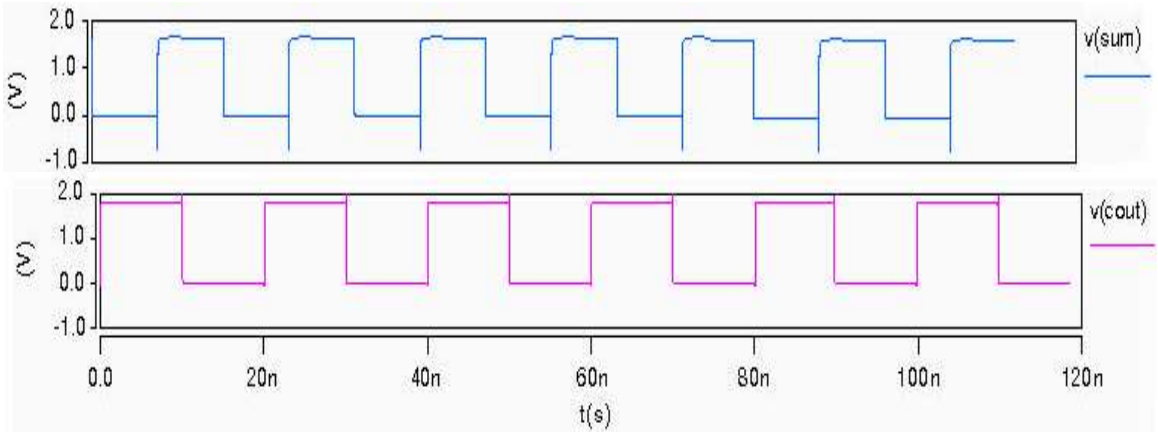

Fig. 6(b): Timing output waveforms for mixed GDI full adder based on inverter topology

A comparative performance of single Full Adder topologies using 0.35µm and 0.18µm CMOS technologies is shown in Table 3 and 4 respectively which reveal that GDI Full Adder is fastest with lowest power consumption as compared to TG and Mirror Full Adders.

To improve the speed performance of single topology long Full Adder chain, a mixed Full Adder topology is proposed. In this topology static CMOS inverter gates are inserted in the chain to optimize the delay and power which is discussed in next section.

A GDI cell can be represented by one resistor (R1) and two capacitors (C1 and C2) which shown in Fig. 3. The values of this resistor and capacitors depend upon the CMOS Technology used [10].

PROPOSED MIXED GDI FULL ADDER BASED ON INVERTER TOPOLOGY

In spite of high speed and low power performance of single GDI adder, its speed performance is degraded when cascaded within a long chain because it is equivalent to a RC ladder network which is shown in Fig. 4. As it is well known that the delay of single topology chain is a quadratic function of the number of Full Adders so for the long single topology chain the delay becomes unacceptably high. To limit this problem mixed topology strategy is adopted. This strategy includes the interruption of inverters (static gate) within the chain which is shown in Fig. 5. The interruption of inverters not only minimizes the delay from input carry to output carry but also the delay equation becomes

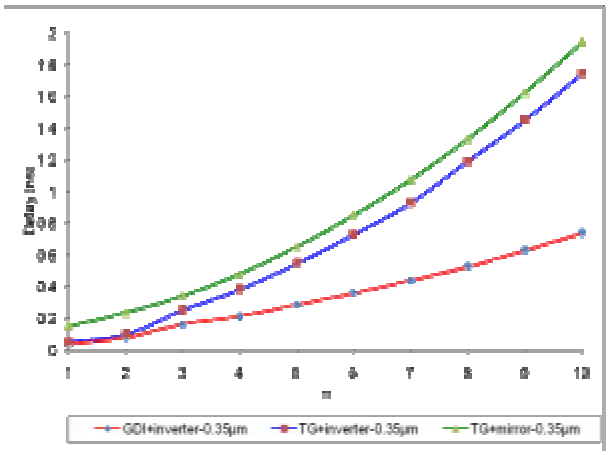

Fig. 7: Delay versus m for different mixed topologies using 0.35µm CMOS technology

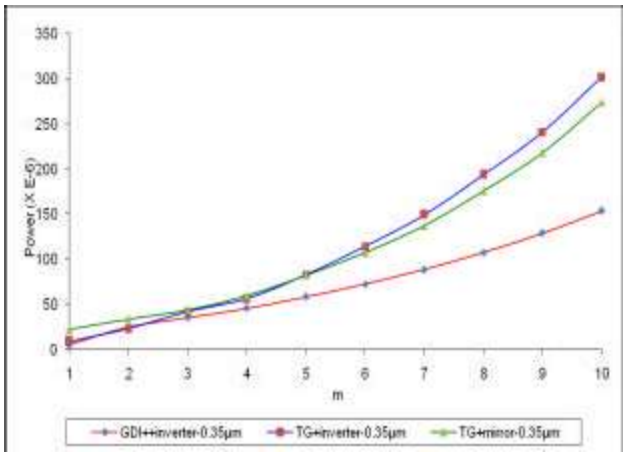

Fig. 9: Power versus m for different mixed topologies using 0.35 µm CMOS technology

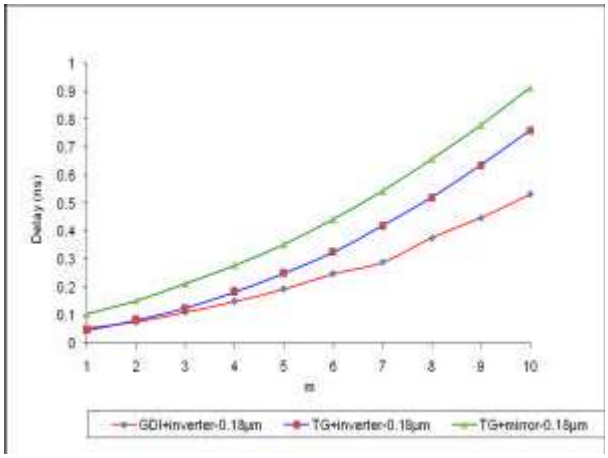

Fig 8: Delay versus m for different mixed topologies using 0.18µm CMOS technology

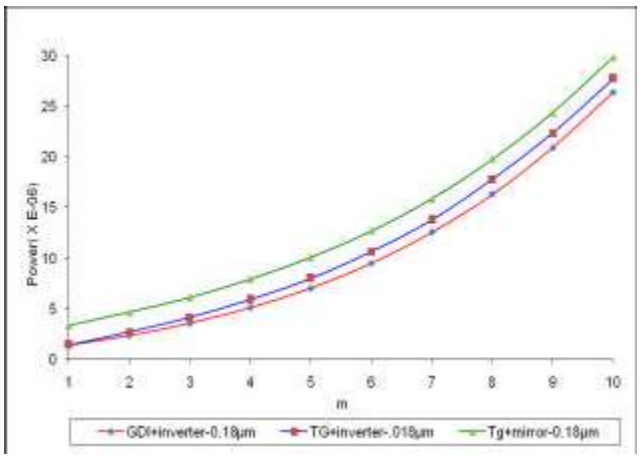

Fig. 10: Power versus m for different mixed topologies using 0.18µm CMOS technology

linear function of n (number of full adders). In this strategy a long chain consisting of n full adders is broken into mixed topology chain with m = $m_{optimum}$ resulting overall delay of the chain equals to n times delay per bit. Analytically from RC delay equations shown below delay is found to be optimum for m = 2. RC delay equation for conventional single topology GDI adders represents that the propagation delay is proportional to square of m (number of bits) which becomes unacceptably high for large values of m. Propagation delay for single topology chain consisting of m GDI Full Adders by applying the Elmore delay approximation [11] is given by equation 1.

$$\tau_{PD,GDI} = 0.69\left[R(C_1+C_2)\frac{m(m+1)}{2}+nR(C_L-C_1)\right] = 0.69R(C_1+C_2)\left[\frac{m(m+1)}{2}+n\frac{(C_L-C_1)}{(C_1+C_2)}\right] \quad (1)$$

Now for the mixed topology chain the overall delay is sum of delay of single topology and buffer whose delay equation is as follows.

$$= 0.69R(C_1+C_2)\times\left[\frac{m(m+1)}{2}+\frac{(C_{in,stati\_gate}-C_1)}{C_1+C_2}\right]+\tau_{PD,stati\_gate} \quad (2)$$

For determining the number of Full Adders between two consecutive inverters i.e. m so that the delay is minimum, this equation is differentiated with respect to m and equate to zero. i.e.

$$\frac{d\tau_{PD,reload}}{dm}=0$$

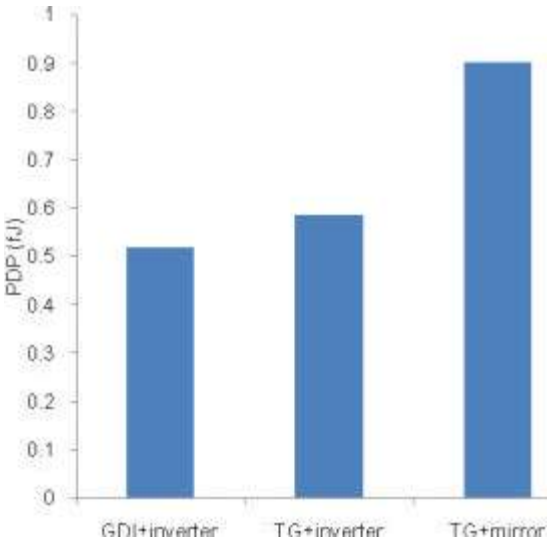

Fig. 11: PDP for different mixed topologies using 0.35µm CMOS technology

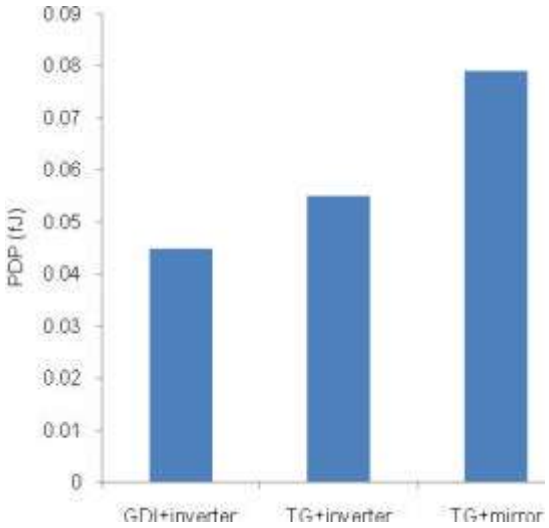

Fig. 12: PDP for different mixed topologies using 0.18µm CMOS technology

By solving the above equation the optimum value of m is

$$m_{optimum} = \sqrt{\frac{2P_{D,static\_gate}}{0.69R(C_1 + C_2)}} \quad (3)$$

SIMULATION RESULTS

Proposed Mixed GDI Full Adder based on inverter topology circuit is simulated on HSPICE using TSMC 0.35µm and 0.18µm CMOS Technologies considering minimum power design (i.e. minimum transistor size).

Table 5: Performance parameters for mixed topologies at 0.35 µm

	Delay per bit (ps)	Power per bit (µw)	PDP per bit (fJ)
GDI +inverter	42.09	10.31	0.518
TG +inverter	50.88	11.50	0.585
TG +mirror	79.79	11.29	0.900

Table 6: Performance parameters for mixed topologies at 0.18 µm

	Delay per bit(ps)	Power per bit(µw)	PDP per bit(fJ)
GDI +inverter	38.31	1.185	0.045
TG +inverter	41.05	1.345	0.055
TG +mirror	51.06	1.550	0.079

Timing Input waveforms for Mixed GDI Full Adder based on inverter topology is shown in Fig. 6 (a). The input combinations are applied to the proposed topology circuit in such a way that effect of input carry is transferred to output carry as delay is to be evaluated Cin to Cout which is depicted in Fig. 6 (b). The delay versus m for different mixed topologies using 0.35µm and 0.18µm is shown in Fig. 7 and 8 respectively. It shows that delay rises with the increases in m for the proposed as well as reported topologies. However, the delay per bit of the proposed topology is lesser than the reported topologies. It has been theoretically demonstrated in literature [12] that power is a linear function of number of cascaded Full Adders in mixed topology chain which is verified from the results of power versus m for different mixed topologies shown in Fig. 9 and 10. Additionally, the power of n bit adder chain equals to n times the power per bit. The PDP results for GDI Full Adder based on inverter topology and reported TG + inverter and TG + mirror adder using above said 0.35µm and 0.18µm CMOS Technologies are shown in Fig. 11 and 12.

COMPARISON OF DIFFERENT MIXED TOPOLOGY CIRCUITS

Delay, power and PDP per bit of the proposed mixed GDI Full Adder interrupted by inverter and previously reported mixed TG + inverter and TG +mirror topologies [13, 14] has been evaluated using TSMC 0.35µm and 0.18µm CMOS Technologies with HSPICE simulations considering minimum power design. These simulation results at 0.35µm and 0.18µm CMOS technologies are shown in Table 5 and 6 respectively, which reveals that delay, power and PDP per bit of proposed mixed topology are lesser than the reported topologies.

The delay is measured between the time when the changing input reaches its 50% voltage level to the time when the resulting output reaches its 50% voltage level for both rise and fall output transitions. Delay per bit is the total delay divided by number of stages to implement Full Adder design. The proposed GDI +inverter circuit give the better performance than the reported circuits in terms of delay per bit. The proposed circuit is 17 to 47% and 7 to 25% faster than the reported circuits at 0.35µm and 0.18µm CMOS technologies respectively.

The power consumption is measured with the same input settings as for the propagation delay measurement [15, 16]. Subsequently the average dynamic power of proposed circuits is 8 to 10% and 12% to 24% lower than the reported circuits at 0.35µm and 0.18µm CMOS technologies respectively.

The power-delay product per bit (PDP) measured in fJ is defined as the product of the delay per bit and the average power consumption per bit. The PDP per bit for the proposed circuit has been improved by 11.45% to 42% and 18% to 43% at 0.35µm and 0.18µm CMOS technologies respectively.

CONCLUSION

In this paper a new mixed GDI Full Adder topology has been presented. HSPICE simulations were performed to evaluate delay, power and PDP of the proposed and previously reported topologies using TSMC 0.35µm and 0.18µm CMOS technology. The design adopts interruption of inverter to alleviate the problem of signal degradation during propagation through long chain. This proposed mixed Topology is analyzed to exploit the high speed potential and low power feature of GDI Full Adder. So proposed GDI Full Adder based on inverter is a better one as compared to existing topologies as far as delay, power and PDP is concerned. On the basis of simulation results obtained it is culminated that the proposed topology is suitable for high speed low power arithmetic circuits. Another advantage of it is the high degree of design freedom as the same can be used for a wide range of applications. This greater flexibility affords significant design efforts.

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