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A Novel Mixed Mode Current and Dynamic Voltage Full Adder

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Abstract: A novel mixed mode current and dynamic voltage CMOS 1-bit full adder cell is presented. In this new design, by combination of voltage and current mode circuits and adopting the advantage of each circuit in the finest way, we obtain the highest possible speed. The results are validated through HSPICE Simulation with 0.18 um and 1.8v, Vdd.

Key words: Current mode . Dynamic voltage . CMOS VLSI design . Full adder

INTRODUCTION

The current mode circuits have now developed into a solid competitor for the voltage mode circuits. Free algebraic summation, simplicity of the design and accessible approach to the desired speed by adjusting the current and several other ascendancies, have induced the current circuits to acquire a particular position in the logic styles. Notwithstanding all these advantages, the structured gates in the current mode possess some weak points which are originated from essence of voltage element. For instance, high noise acceptability of current mode gates, have always been an obstacle in the technique of operative circuits. Instead, voltage mode gates, in contrary of the current mode gates, were used for many years.

These gates are much older than their newer counterparts, so called as current mode circuits and the deficiencies in them have over time been improved. High resistance against noise, simplicity of the design, considerable logic production, uncomplicated production of the inputs and some other positive features confirm partial dominance of built logic in this mode, over the current mode circuits.

Thus, if there is a gate which possesses both modes of voltage and current outputs, it can enjoy the benefits of both designs.

Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as microprocessors and application specific DSP architectures. In addition to its main task, which is adding two numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, address calculation, etc. In most of these systems the adder lies in the critical path that determines the overall speed of the system. That is why enhancing the performance of the 1-bit full adder cell (the building block of the adder) has been of a continuous interest [1-3].

Since the available sources had been of voltage type previously, the internal circuits of preliminary gates were traditionally built according to inputs and outputs of voltage. All the famous logic families have been designed in this mode.

As mentioned before, several logic styles have been used in the past to design full adder cells. Some of these logic styles are listed in next section. In addition we review previous dynamic full adders. Then we present the new mixed mode current and dynamic full adder. The circuit simulation for delay performance and the results are analyzed and compared in section Results and Discussion.

MATERIALS AND METHODS

Review of full adder design of different CMOS logic styles: Several alternates of static CMOS logic styles have been used to implement low-power 1-bit adder cells [2, 4-6]. In general, they can be largely divided into two major categories: The complementary CMOS and the pass-transistor logic circuits. The complementary CMOS full adder (C-CMOS) of Fig. 1(a) is based on the CMOS structure with PMOS pull-up and NMOS pull-down transistors. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage and arbitrary transistor sizes [12].

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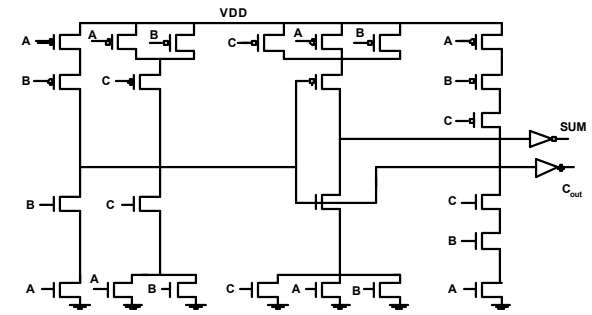
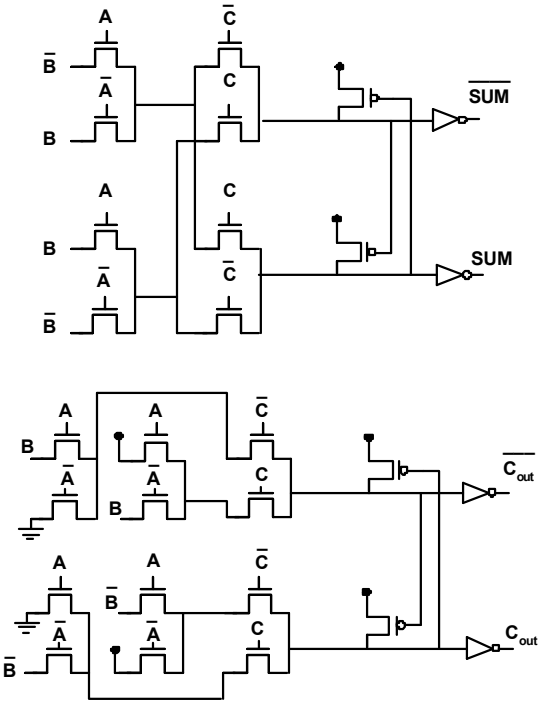


(a)



(b)

Fig. 1: Full adder cells of different logic styles. (a) C-CMOS, (b) CPL

The complementary pass transistor logic (CPL) [10] full adder with swing restoration is shown in Fig. 1 (b). Its dual-rail structure uses 32 transistors (henceforth "*n* transistors" is abbreviated as *n* T) [4, 6]. The output is a weak logic "1" when "1" is passed through a NMOS and is a weak logic "0" when "0" is passed through a PMOS. Therefore, output inverters are also used to ensure the drivability [12].

The remaining full adder designs, which are not shown in this paper, are TFA, TGA, 14T and 10 T Hybrid Logic styles.

Transmission gate logic circuit is a special kind of pass-transistor logic circuit [7, 9]. It is built by connecting a PMOS transistor and a NMOS transistor in parallel, which are controlled by complementary control signals. Both the PMOS and NMOS transistors will provide the path to the input logic "1" or "0" respectively, when they are turned on simultaneously. Thus, there is no voltage decline problem whether the 1 or the 0 is passed through it [12].

Lesser transistor count adder circuits have been proposed, most of which use the non full swing pass transistors with swing restored transmission gate techniques. This is exemplified by the state-of-the-art design of 14T and 10T. Hybrid logic design style uses more than one logic style for their implementation cascaded cells [12].

Existing dynamic full adders: Voltage mode in a general shape contains two networks. Each of these networks contains transistors which behave like a switch. The pull up network is responsible to produce logical "1" and the pull down network is responsible to produce logical "0". In these circuits a group of switches is connected and the other group is disconnected in every instant. So we need two groups of switches in constructing these gates, which usually have a contrary operation with each other and is dependant to the output function. The CMOS family gates, are good example for comprehension of the structure of these circuits [15]. This function will cause increasing in input capacitor of each gate. In dynamic design with purpose of decrease in area of chip and increasing speed, one of the pull down or pull up networks will be removed and it will be replaced with a transistor, which controlled by signal. With this clock, the normal functions of circuit are divided into two phases, pre-charge and evaluate (Fig. 2). In pre-charge phase, the output node is loaded to vdd or GND. In evaluate phase, the output node is changed in situation as provisional.

The advantages of dynamic logic consist of decrease in chip as compared with CMOS static logic, less parasite capacitor, high speed in each gate and consequently speed up of the whole circuit.

The NP Complementary dynamic CMOS full adder [16, 17] is shown in Fig. 3(a). It is anchored in dynamic CMOS designing in two levels, with NORA (NP) technique.

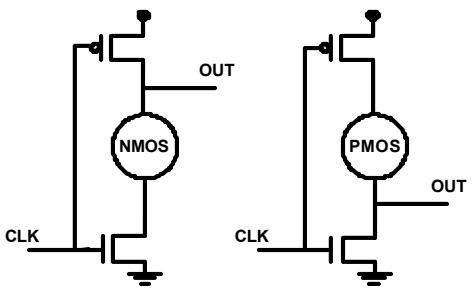


Fig. 2: Schematic of dynamic circuits

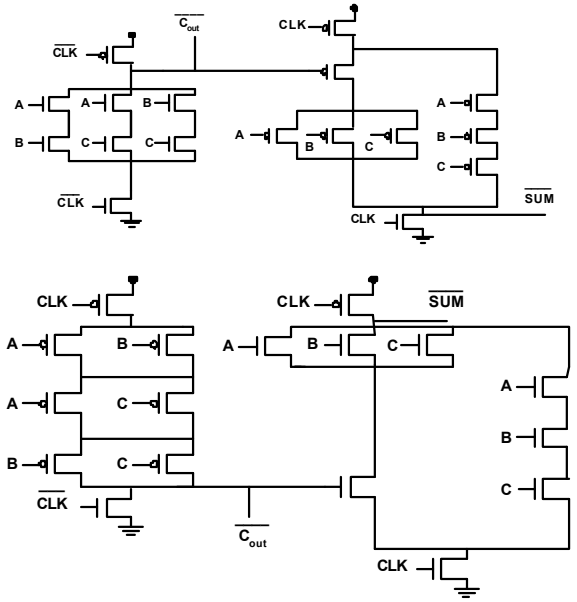


Fig. 3: Dynamic full adder (a) NP, (b) PN

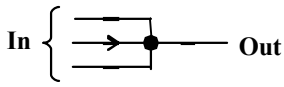


Fig. 4: Three input adder in current mode

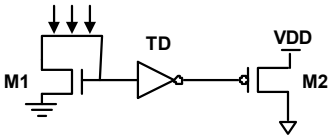


Fig. 5: General aspects of logic gates in current mode, with a source output

Novel mixed mode current and dynamic voltage full adder: In this section the Novel mixed mode current and dynamic full adder is presented. To produce sum we use current mode based on Majority Function.

The designed circuits in current mode use the natural traits of current for logic circuits. For example, according to the KCL rule, the sum of input currents to one point is always equal to sum of the output currents from that point. In this discipline, Fig. 4 could be a three input adder in current mode [18].

As it can be observed in Fig. 4, with a short circuit of three lines as the input lines and one line as output we built a 3-bit adder. With the same pattern, if we want to have an n-bit adder in a current mode, we must consider a short circuit of n+1 line and then one line as an output and the other n lines as the input lines. In this mode, with use of the natural traits of current, we could implement different aspects of logic gates in an interesting fashion.

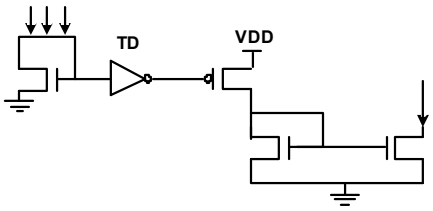


Fig. 6: General shape of logic gates in current mode, with sink output

Consider Fig. 5 [18]. In the Circuit illustrated in Fig. 5, both inputs and outputs are of current in gender. M1 transistor converts quantities of the input currents into voltage and provides it to an inverter. The threshold voltage of the inverter is pointed out with TD and provided to the designer [14, 18].

M2 transistor is switched on and off under the control of the inverter, thus connects and disconnects the output current. Despite of the constant shape of this circuit, it can implement the functions of AND, OR, Majority Function, Minority Function and many other functions. In the circuit illustrated in Fig. 5, the only variant is the quantity of TD. If different quantities of TD are specified, the produced functions in the output of this circuit are also changed. As an instance, with a threshold detector from 0.5 OR gate, with the threshold detector from 2.5 AND gate and also with TD from 2 majority function shall be obtained [18].

In this design, the constant general shape of these gates could be encountered as advantage which simplifies the process of designation. The circuit in Fig. 6 is same as the circuit of Fig. 5 with a difference that is the output which is sink instead of source [18].

The majority function is a logic circuit that performs a majority vote to determine the output of the circuit. In this part, we describe how the circuit of the full adder based on majority function could be designed.

The full adder can be operated as follows: given the three input A, B and *Cin*, it is desired to calculate two 1-bit outputs SUM and *Cout*. Fig. 7 illustrates (a) the truth table and (b) the logic equations of full adder cell.

As previous equations show, C_{out} can be implemented with three inputs Majority function as shown in Fig. 8(a) and if we invert the output of the circuit, C_{out} is produced with Majority Not function circuit as shown in Fig. 8(b).

The new notion that has been implemented in pattern of this circuit in Current Mode to produce SUM has been illustrated in Fig. 9.

According to Fig. 10, initially, C_{out} is produced according to the Majority Not Function and then C_{out} with two option and three input of A,B and C with

Majority function	SUM	C_{out}	C_{in}	B	A
0	0	0	0	0	0
0	1	0	1	0	0
0	1	0	0	1	0
1	0	1	1	1	0
0	1	0	0	0	1
1	0	1	1	0	1
1	0	1	0	1	1
1	1	1	1	1	1

(a) $C_{out} = AB + AC + BC$

(b) $Sum = \overline{Cout}\ (A + B + C) + ABC$

Fig. 7: (a) Truth Table (b) Logic equations of full adder cell

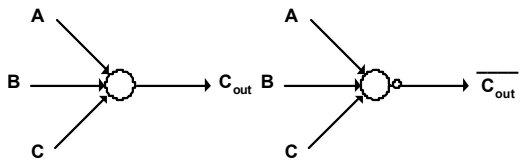


Fig. 8: Logic gates for (a) Majority function, (b) Majority not function

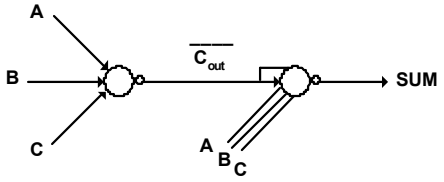


Fig 9: Full adder based on majority function and majority not function

each one option is presented to a Majority Function to produce Sum.

In this pattern of majority not function in voltage mode (Dynamic) is the matching part of majority function in current mode.

Table 1: Truth table of $\overline{C_{out}}$ SUM and majority function

Majority function	Sum	$\overline{C_{out}}$	C	B	A
0	0	1	0	0	0
1	1	1	1	0	0
1	1	1	0	1	0
0	0	0	1	1	0
1	1	1	0	0	1
0	0	0	1	0	1
0	0	0	0	1	1
1	1	0	1	1	1

With regard to the designed circuit and the truth table, C_{out} enters into the M9 transistor gate and to provide it with tow option, since we are in the Current Mode, the current which is pulled from the M_9 Transistor must be twice as much as the current from $M_{10\text{-}12}$. So:

$$\left(\frac{W}{L}\right)_{M9} = 2\left(\frac{W}{L}\right)_{M10,11,12}$$

According to Table 1, Threshold Detector of Not Gate of this circuit is 2.5.

RESULTS AND DISCUSSION

The two static full adders: C-CMOS, CPL and the two Dynamic full adders: NP-C-CMOS, PN-C-CMOS and proposed mixed mode full adder are all simulated using 0.18 um CMOS process. The supply voltage is 1.8V and the frequency is 100 MHz. The threshold voltage of the NMOS and PMOS Transistors are around 0.39 and 0.42 v. HSPICE Circuit simulator is used for simulation.

The output wave form of previous full adder is shown in Fig. 11 and the output wave form of proposed full adder is shown in Fig.12.

Delay comparison: Because the input of the circuit is voltage, the pattern of output wave of the suggested

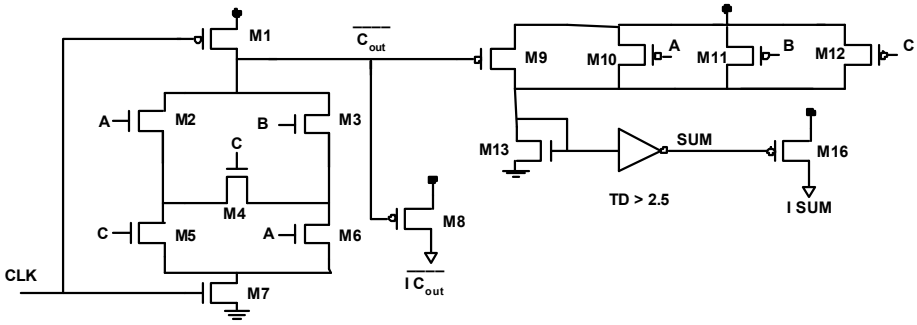


Fig. 10: Proposed mixed mode full adder

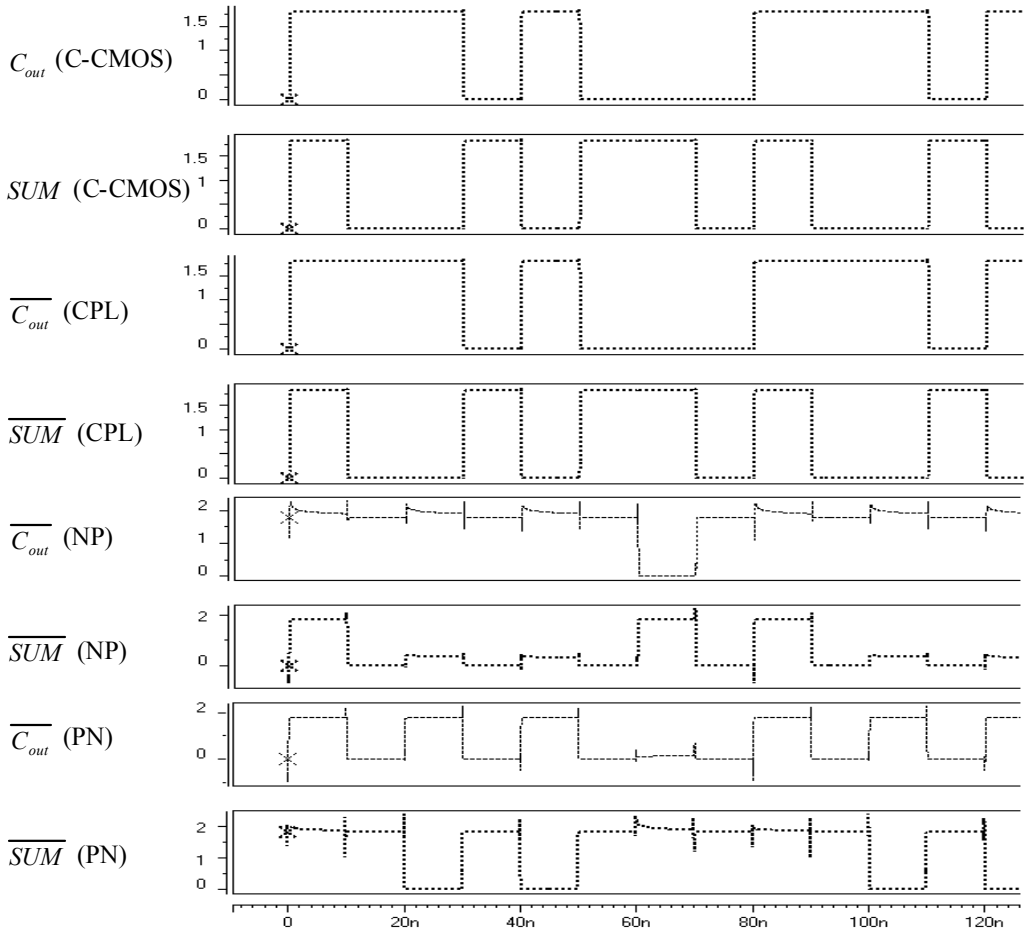


Fig. 11: The output waveform of voltage mode full adder(1.8 v,100MHz)

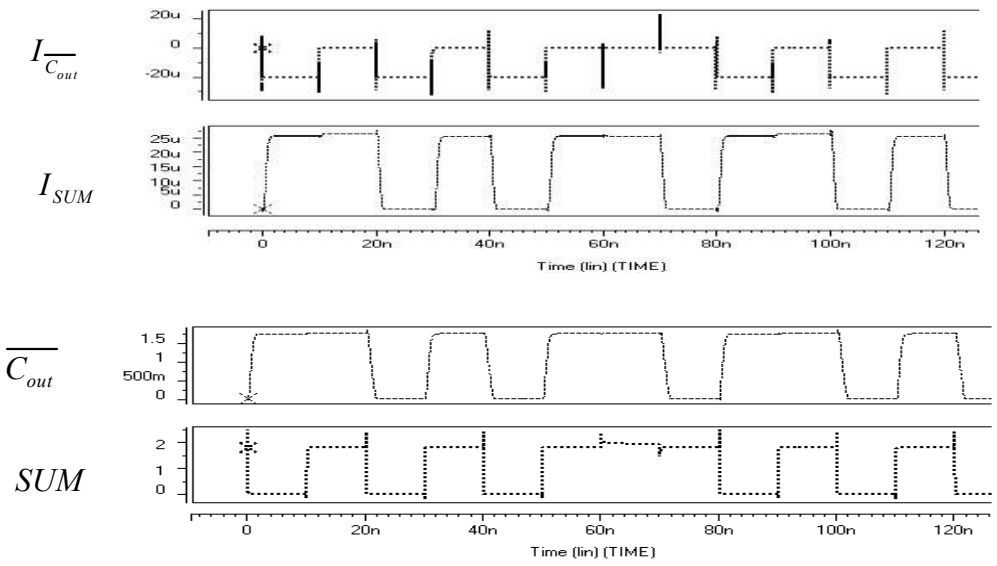


Fig. 12: The output Waveform of proposed circuit, (a) voltage output, (b) current output

Table 2: Simulation results for the proposed full adder in 0.18 um technology at 100 MHz and 1.8v, Vdd

Delay (ns)	Logic style
0.135	C-CMOS
0.130	CPL
0.129	NP-C-CMOS
0.128	PN-C-CMOS
0.028	Mix Mode (proposed)

circuit which is shown in Fig. 12(a) is also voltage. {V($\overline{C_{out}}$) and V(Sum)} has been shown as well.also in Fig.12(b) the current output wave form is illustrated. The value of delay achieved in recommended value of Vdd (1.8v) intended for all full adders are shown in Table 2. Since the input is voltage and also $\overline{C_{out}}$ is calculated in the voltage mode, the calculated delay in this circuit is $\overline{C_{out}}$ delay.

The proposed full adder produces C_{out} in a high speed pace, then this style can be used to first, generate C_{out} in each cell and then calculate sum, for instance, Ripple and Carry look-ahead adder, to obtain full speed full adder.

CONCLUSION

In this paper we proposed a new mixed mode current and dynamic voltage full adder. Simulation results illustrate a significant improvement in term of propagation delay specially this improvement is highlighted the most in the case of some propagation adder like ripple and carry look-ahead.

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