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A Voltage-Mode Sample and Hold Circuit Based on the Switched Op-Amp Techniques

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Abstract: The design of a simple, fast and accurate sample and hold circuit using a switched op-amp configuration is presented. The unique characteristic of this sample and hold circuit is the cancellation of charge injection effects due to the symmetrical output switched transistors circuit and device configuration. The clock-feed through effect is also reduced by applying the effect of clock pulses to the sources of the main output switched transistors. The circuit is designed using a 2.6 V supply at a clock frequency of 1 MHz. The output error due to an input signal of 1 V peak to peak at frequencies of 20 KHz and 100 KHz is less than 0.25 mV and 0.6mV respectively. Simulation results of second harmonic distortion using 0.25µm CMOS technology at input frequencies of 20 KHZ and 100 KHz is 86 dB and 72.5 dB below the signal level respectively at 1 volt peak to peak input.

Key words: Analog-digital converter . Sample and hold . Switched op-amp . Charge injection

INTRODUCTION

An important role in the design of data-converter systems is played by Sample-and-hold (S/H) circuits. A switched-capacitor (SC) technique utilizes the excellent properties of on-chip capacitors and MOS switches while permitting the realization of numerous analog sampled-data circuits. However, channel charge injection and clock feedthrough are the two major sources of errors when the switches are turned off [1, 2]. Though many switching techniques [3, 4] and circuit topologies such as switched opamp and Miller techniques [5-8] have been proposed and developed. However the nonlinearity effect caused by charge injection and clock feedthrough still limits circuit performance, particularly in high-resolution data converters. The charge transferred onto the hold capacitor while the transistor is turned off determines the total error as a result of charge injection. Charge injection and clock feedthrough are the primary errors that set the maximum usable resolution of an S/H. In this work by using a single ended switched opamp, an accurate S&H is designed. The charge injection due to the output transistors is cancelled by designing the area and transconductance of both output transistors to be the same. The effect of clock feedthrough is also minimized by turning the output switches off via the source terminals instead of gates. Furthermore the crucially important conditions for the simultaneous turning off the two output transistors are analyzed. Finally the simulation results of the proposed circuit using HSPICE and 0.25µm CMOS technology are presented.

Design procedures: The proposed S/H circuit is shown in Fig. 1. Transistors M1-M4 make up the cascoded output of the opamp and M5-M6 are the indirect output transistor switches. M13-M14 are the inverted buffer. The operation of the circuit is as follows, while in tracking mode switches M5 and M6 are off and the output will track the input signal in a unity gain closed loop configuration.

In holding mode, transistors M5 and M6 are switched on as a result, transistors M2 and M3 are turned off. The sampled voltage is available at the output via a high impedance inverted buffer. Application of the current mirror and the cascode configuration are used for increasing the open loop gain

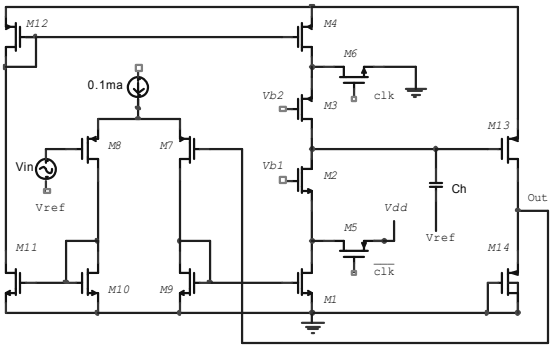

Fig. 1: Proposed S/H circuit

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and it also prepare the symmetrical configuration that is used for minimizing the charge injection effect. The signal path is observed to be low impedance except at the holding capacitor node, hence eliminating the need for an extra compensation capacitor. This technique improves the unity gain frequency of the opamp and as a result the higher clock frequency as compared to the similar work [9]. Transistors M13 and M14 form an inverter buffer output configuration having a precise linear large signal characteristics as reported and explained elaborately by [10].

Charge injection cancellation: The charge injection due to M2 and M3 are given by equation (1) and (2) respectively.

$$Q_{M2} = -W_2L_2C_{ox}(V_{gs2}-V_{tn})=W_2L_2C_{ox}V_{eff2} \quad (1)$$

$$Q_{M3} = W_3L_3C_{ox}|(V_{gs3}-V_{tn})|=W_3L_3C_{ox}V_{eff3} \quad (2)$$

In the holding capacitor node:

$$ID_{M3} = ID_{M2}+I_{Ch} = ID_{M2}+C_h\omega V_{IM}Cos(\omega t) \quad (3)$$

The second term in equation (3) can be ignored in the frequency range of interest, hence the two transistor currents are almost equal. For the practical considerations such as dynamic range, the effective voltage of transistors M2 and M3 are designed equal. From the above considerations, using saturation characteristic equation and equations (1) through (3), results:

$$\frac{W_3}{L_3} = \frac{W_2}{L_2}\left(\frac{\mu_n}{\mu_p}\right) \Rightarrow W_3 = \sqrt{\frac{\mu_n}{\mu_p}}W_2;\ L_2 = \sqrt{\frac{\mu_n}{\mu_p}}L_3 \quad (4)$$

Equation (4) must be held in order to cancel the charge injection effect. As a result of equation (4), both the area and the transconductance of the transistors M_2 and M_3 must be the same. The clock feed-through charges of M2 and M3 are also cancelled by indirect switching via transistors M5 and M6 respectively. This is due to the fact that the switching voltage is applied to the source terminals instead of gates while the gate terminals are stabilized by the constant bias voltages. The circuit dependence on device mismatches is not critical since the total injected charge into the hold capacitor (Q_{total}) is given by equation (5):

$$Q_{total} = (W_3L_3-W_2L_2)\,C_{ox}\,(V_{eff3}-V_{eff2}) \quad (5)$$

Observing that the first term, explicitly and the last term according to equation (6) are dependent on relative accuracy of dimensions.

$$\frac{V_{eff3}}{V_{eff2}} = \sqrt{\frac{W_2L_3\,\mu_n\,ID_{M3}}{W_3L_2\,\mu_p\,ID_{M2}}} \quad (6)$$

Loading effect of indirect switches: It is vitally important that transistors M2 and M3 are turned off simultaneously in order to avoid pedestal error. Consequently the capacitive loading effect and absolute currents of the switched transistors M5 and M6 must be equal. The first problem can be alleviated by equating W_5 to W_6 since the capacitive load of drain and source are proportional to the width of transistors. The latter problem is diminished by satisfying equation (7).

$$\frac{L_5}{L_6} = \frac{m_n}{m_n}\left(\frac{V_{dd}-V_{tn}}{-V_{dd}-V_{tp}}\right)^2 \quad (7)$$

SIMULATION RESULTS

The proposed circuit is simulated using HSPICE and 0.25µm CMOS technology. The simulation is carried out under the sampling frequency of 1MHz and the output load of 1 pF. The open loop frequency response of the designed opamp is shown in Fig. 2. Using a 2.5 pF holding capacitor and a single supply voltage of 2.6 volts an open loop unity gain bandwidth of 31.4 MHz, phase margin of 53º and 79 dB of DC gain are achieved.

Figure 3 shows the output of the S/H circuit for a 1 V (P-P) sinusoidal input signal at 50 KHz. As shown in the captured section of Fig. 3. the pedestal error is less than 0.15 mV and the total error is approximately 0.4 mV. In frequency range below 25 KHz the total error is less than 0.2 mV which is approximately equivalent to a 12 bit resolution.

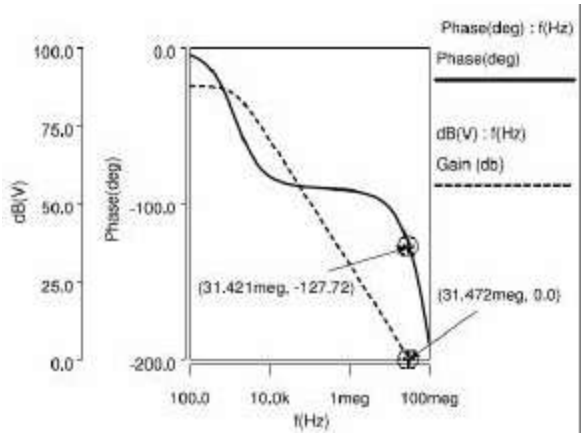

Fig. 2: Frequency response of the main op-amp with $C_h = 2.5pf$

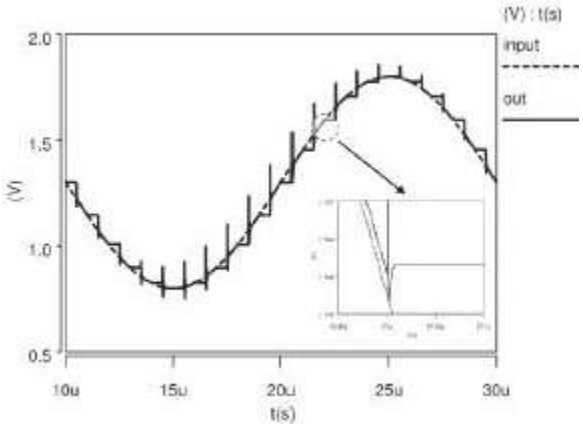

Fig. 3: Comparison of input and output
------- Input voltage at 50KHz and 1v(p-p)
–––––– Output sampled signal

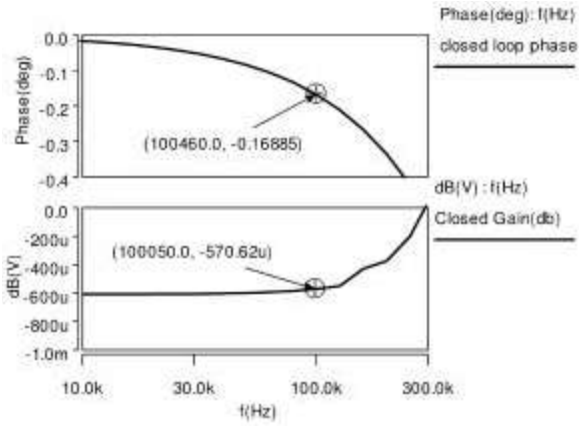

Fig. 4: Frequency response of closed loop op-amp

Increasing the input frequency will result in a higher total error which is mainly due to the phase delay action of input-output closed loop. For instance, at frequency of 100 KHz the total error is comparable to less than 10 bit resolution. Fig.4 shows the frequency response of closed loop S&H with M_5 and M_6 switches removed. The phase delay between input and output is approximately-0.16°. Equation (8) shows the effect of phase delay (f) error while an input signal of 0.5 Sin (ωt) is assumed. Simulation results confirms the validity of equation (8).

$$V_o - V_i = \text{Cos}(\omega t)\ \text{Sin}(f/2) \quad (8)$$

Figure 5 shows the power spectrum density (PSD) which is calculated using 2048 point FFT [11] for frequencies of 20.01953125 KHz and 100.0976563 KHz. Second harmonic distortion is 82 dB and 72.5 dB respectively below the main tone.

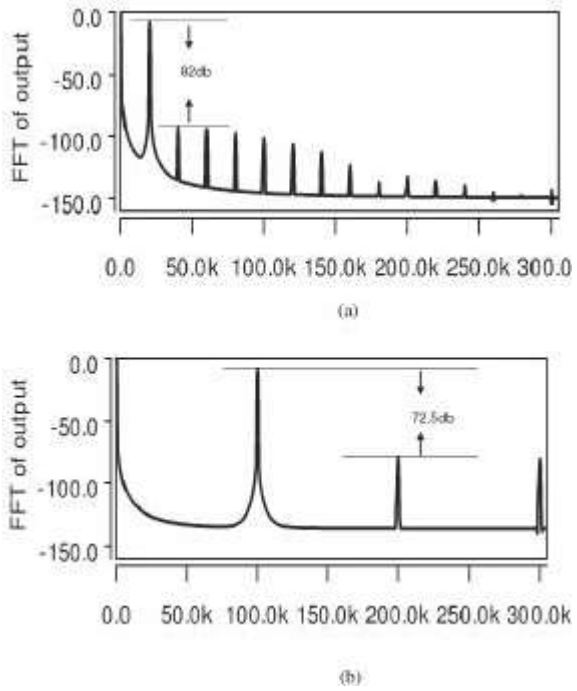

Fig. 5: FFT of output at input amplitude of 1 volt (p-p) at frequencies of
a) 20.01953125 KHz
b) 100.0976563 KHz

Table 1: Overal specification of proposed sample and hold

Input maximum amplitude	1000 mv (p-p)
Power supply	2.6v
Vref	1.3v
Power dissipation	1.35mw
Dynamic range	74db
Acquisition time at 1v step and 0.2mv error	104 ns
Sampling frequency	1MHz
Opamp dc gain	79db
Opamp phase margin	53°
Opamp SR	34.5v/μs

Table 1 shows the overall specification of the proposed S&H as presented

CONCLUSION

In this paper the design and the simulation of a simple single ended voltage mode S/H circuit with less dependence on charge injection and clock feed-through is presented. A novel symmetrical structure in the output switch transistors is used to cancel the charge injection. By indirect switching of the main output transistors via sources instead of gates the clock feedthrough is minimized. The loading effect of indirect

switches is also considered in the design. The simulation results shows the proposed sample and hold circuit has a 12 and 10 bit resolution at 25 KHz and 100KHz input frequency respectively.

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