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A Novel Circuit Design Technique to Minimize Sleep Mode Power Consumption due to Leakage Power in the Sub-100nm Wide Gates in CMOS Technology

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Abstract: With the rapid scaling down of CMOS manufacturing technology, the reduction in leakage power has become an important concern in low voltage, low power and high performance applications. In this paper a novel circuit design technique is presented which minimizes sub-threshold leakage current by zeroing drain-source voltage. This results in a reduction of leakage power consumption in sleep mode especially in wide gates. Since leakage power due to sub-threshold current in sub-100nm technologies increases dramatically the proposed circuit design technique is designed to be less dependent on technology scale and temperature. Since there is no additional circuitry needed for power reduction in this circuit design technique, there is no additional circuitry needed for power reduction. Thus, circuit complexity and dies area cost is much less than existing logic families. Moreover, the switching time between sleep mode and active mode is shorter.

Key words: Dynamic circuits . Leakage . Sleep-mode . Active mode . Low power design . Voltage scaling

INTRODUCTION

In recent years, there has been an increasing trend towards the use of many types of portable electronic equipment. In such portable applications, it is extremely important to minimize current consumption due to the limited availability of battery power. When the whole circuit or segments of it are not in use, they must quickly be switched into a sleep mode in which they almost consume no power. Still leakage current may cause some power consumption even in the sleep mode. If the circuit could be designed such that there is very low leakage current in this mode, then the lifetime of the portable application will increase dramatically. Moreover, the sleeping circuit must be easy to start up. This start up must also be soft, which means that no short circuit current should be allowed to flow through the circuit. In order to manage the active power consumption of high-performance digital circuits, there is a need for active leakage control techniques to gain significant leakage power savings as well as fast time constants for entering and exiting idle mode. Tschanz *et al*. [1] used dynamic sleep transistors and body bias along with clock gating to control active leakage for a 32-bit integer execution core in 130-nm CMOS technology. Their measurements of pMOS sleep transistor showed that there was a substantial reduction in leakage power, while the reactivation of block was achieved in less than two clock cycles. PMOS body bias reduces leakage power with no performance penalty and similar reactivation time. Power measurements at 4 GHz, 1.3V, showed that there was an 8% total power reduction using dynamic body bias and 15% power reduction using a pMOS sleep transistor, for a typical activity profile.

Zhao *et al*. [2] proposed an external dual switch leakage controlled flip-flop which effectively reduces the leakage current by 4 times over the other leakage controlled flip flops.

Gu *et al*. [3] presented the generally unnoticed fact that the sleep transistors for leakage reduction can significantly damp the resonant supply noise due to their series resistance. They presented an optimal sleep transistor sizing method considering the dominant resonant supply noise and showed that a smaller sleep transistor can offer a smaller worst case supply noise due to the increased damping. Gu *et al*. [3] proposed an adaptive sleep transistor technique which automatically dampens the resonant noise only when it is detected with simulations in the 32nm CMOS and showed that the resonant noise was reduced by 32%. Zhao and Cao [4] presented a new generation of Predictive Technology Model (PTM) which may be used for this purpose. They state that in their model which is based

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on physical models and early-stage silicon data, bulk CMOS for 130-to 32-nm technology nodes, with an L_{eff} of as low as 13 nm may be simulated successfully. They state that the error of I_{on} is below 10% for both n-channel MOS and p-channel MOS. The model has been updated recently to cover 22nm technology for metal gate/high-k CMOS.

THE SOURCES OF LEAKAGE CURRENT

There are three main sources of leakage current that the designer must minimize. They are the source/drain junction leakage current, the gate tunneling leakage and the sub-threshold leakage current through the channel of an OFF transistor. The source/drain junction leakage current from the drain and the source to the substrate is due to the fact that the junction acts like a reversed biased diode when the transistor is off. The magnitude of this current depends on the size of the diffusion area of the transistor which depends on the process technology. The gate tunneling current flows through the gate oxide into the substrate and increases exponentially when the gate oxide becomes thinner. It also increases with the increase of supply voltage. It is important to control the high-K gate dielectric leakage current if the low power device is in sleep mode. The sub-threshold leakage current is a leakage current from drain to source. It is a diffusion current that is built up by minority carriers in the channel of the MOS device. The MOS transistor is operating in a weak inversion mode (sub-threshold mode). For example, when the input signal to an inverter is turned off, the NMOS transistor in the inverter will turn off. This will force the output signal to switch into high level. Even in this case when the V_{GS} voltage is equal to 0V, a current will flow due to the fact that V_{DS} has the voltage V_{DD} across it. This sub-threshold current will depend on temperature, supply voltage, process parameters and the size of the device. Of these parameters the most important one is the threshold voltage. Moradi *et al*. [5] presented a new leakage-tolerant circuit design technique for high fan-in domino circuits. The technique presented used the stacking effect to reduce the leakage of the evaluation network of domino gates plus a current mirror in parallel with the evaluation network to reduce the evaluation delay. Depending on the fan-in, their technique exhibited 2.0X to 17.7X leakage and noise tolerance improvement compared to standard domino counterparts designed in a 70-nm technology node.

The sub-threshold current is the dominant leakage current in modern technologies. Results of HSPICE simulations for an inverter in the 70nm technology model are shown in Fig. 1.

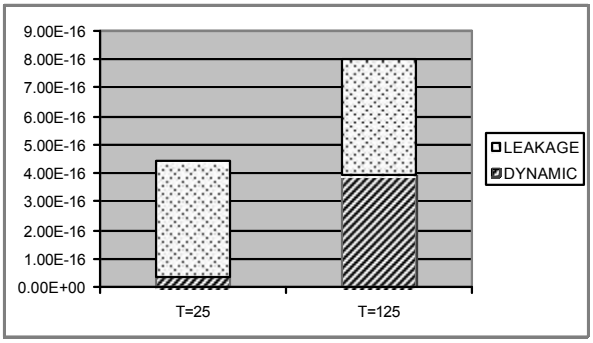

Fig. 1: Simulation results showing a comparison of dynamic power vs. leakage power for an inverter in the 70nm CMOS technology

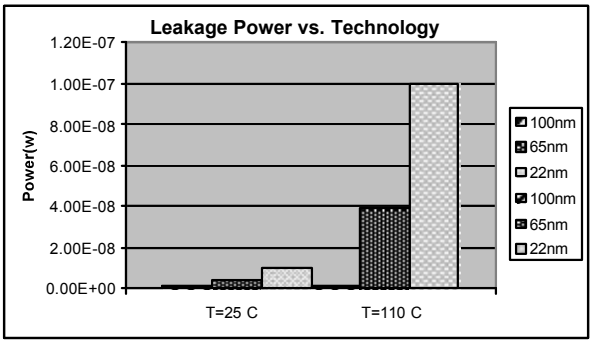

Fig. 2: Simulation results showing a comparison of leakage power vs. technology scaling indicating a worsening of leakage power problem as the technology scales down

A comparison of leakage power vs. technology scale is shown in Fig. 2. As can be seen, leakage power which is very small for 100nm CMOS technology becomes a very major problem in the 22nm technology.

The drain to source current may be calculated with formula (1)

$$I_{DS} = K(1 - e^{\frac{-V_{DS}}{V_T}})e^{(V_{GS} - V_T + \eta\frac{V_{DS}}{nV_T})} \quad (1)$$

where K and n are functions of manufacturing process η is the drain barrier-induced lowering coefficient, V_{DS} is drain-source voltage, V_{GS} is gate-source voltage and V_T is kT/q.

One may see from the formula (1) that the leakage current will increase exponentially with the reduction of the threshold voltage. If the threshold voltage decreases by only 100mV, the sub-threshold leakage current will be increased by a factor of ten. Leakage current also depends on the L and W parameters of the transistor. If the transistor becomes longer it will have a smaller leakage current and if it becomes wider it will have a higher leakage current.

Unlike total dynamic power consumption, total leakage current does not depend on the switching activity. It only depends on the number of transistors which exist on the chip. The input pattern also has a very important effect on leakage current. Because of this input pattern dependence, it is hard to find out exactly how large the leakage current will be. Finding the minimal leakage input pattern is very important in minimizing the leakage current. A significant reduction in leakage current is achievable through using the input pattern with the minimal leakage. Tsai *et al*. [6] evaluated the impact of technology scaling on three run-time leakage reduction techniques being input vector control, body bias control and power supply gating by determining limits and benefits, in terms of the potential leakage reduction, performance penalty and area and power overhead in 0.25, 0.18 and 0.07 μm technologies and presented HSPICE simulation results as estimates with various functional units and memory structures for a comprehensive analysis.

LEAKAGE POWER REDUCTION TECHNIQUES

Various leakage power reduction techniques have been proposed in the past. Won *et al*. [7] 2003 proposed an MTCMOS design methodology for mobile computing. Multi-threshold CMOS (MTCMOS) technology provides low leakage and high performance operation by using high speed, low V_t transistors for logic cells and low leakage, high V_t devices as sleep transistors as shown in Fig. 3. Commonly used processes are double (low and high) or triple (low, normal and high) multi threshold values. The sleep transistors are to disconnect the logic cells from the supply lines in order to reduce the leakage current in sleep mode. This is also referred to as power gating technique wherein circuit blocks that are not in use are temporarily turned off to reduce the overall leakage power. This temporary shutdown time can also called low power mode or inactive mode. When circuit blocks are required for operation, they are activated to active mode. These two modes are switched at the appropriate time in a suitable manner to maximize power performance while minimizing impact on performance. Thus goal of power gating is to minimize leakage power by temporarily cutting power off to selective blocks that are not required in that mode. The main concerns here are wake up latency and power plane integrity. If we suppose that there is a sleep/wake up signal provided from a power management unit, the wake up period of time can affect the overall performance of the circuit. Thus it is very important to minimize the time required to turn on the circuit upon receiving the wake up signal. Moreover, the large current flowing to ground when sleep transistors are turned on may be seen as a major source of noise for the power distribution system on the chip. This might seriously degrade the performance and functionality of the other parts of the circuit. There is always a trade off between the current flowing to ground and the transition time from the sleep mode to the active mode. A low threshold value transistor is very fast but it has quite large sub-threshold leakage currents. This sub-threshold leakage current will be a very important problem when a sleep-mode circuit is constructed. If the sleep-mode is to be effective, this static leakage current must be as small as possible. So if higher threshold value transistors are used to gate ground and also perhaps the power supply (V_{DD}), the lower threshold value transistors are used to perform the circuit function. The higher threshold value transistors will then reduce the sub-threshold leakage current dramatically, but the circuit will then continue to have the same performance as before. These high threshold value transistors are on while the circuit is in active mode and off when the circuit is in sleep mode. The transistors should be wide enough that the current consumption for the active mode will be satisfied. Otherwise the performance of the circuit will be degraded because of the channel resistance of the transistor. Yeo and Roy [8] presented a detailed account of such leakage reduction techniques.

When the physical design of the MTCMOS circuits is done, it is vital to consider the large current flowing through the current stopping transistors in active mode and the electro-migration in the wires should be taken into account. The channel width is also very important due to the large current. There is a trade-off between the local and global sleep devices. The bottleneck with local sleep devices is that there will be a large area overhead due to the fact that there will be a lot of extra transistors. The MTCMOS approach is easy on combinatorial circuits, but it can be tricky on sequential circuits. Should the power supply be turned off, all data stored in the circuit will be irreversibly lost. This is the main problem with MTCMOS circuits. To deal with this problem complex timing scheme must be used or extra circuits have to be added. Because of these added items the performance of the circuit would be degraded. This will also require a larger die area and impose higher power losses.

Variable threshold CMOS (VTCMOS): An efficient method to reduce power consumption is to use low supply voltage and low threshold voltage without losing speed performance. However, this would lead to increased sub-threshold leakage and hence more standby power consumption. Variable Threshold

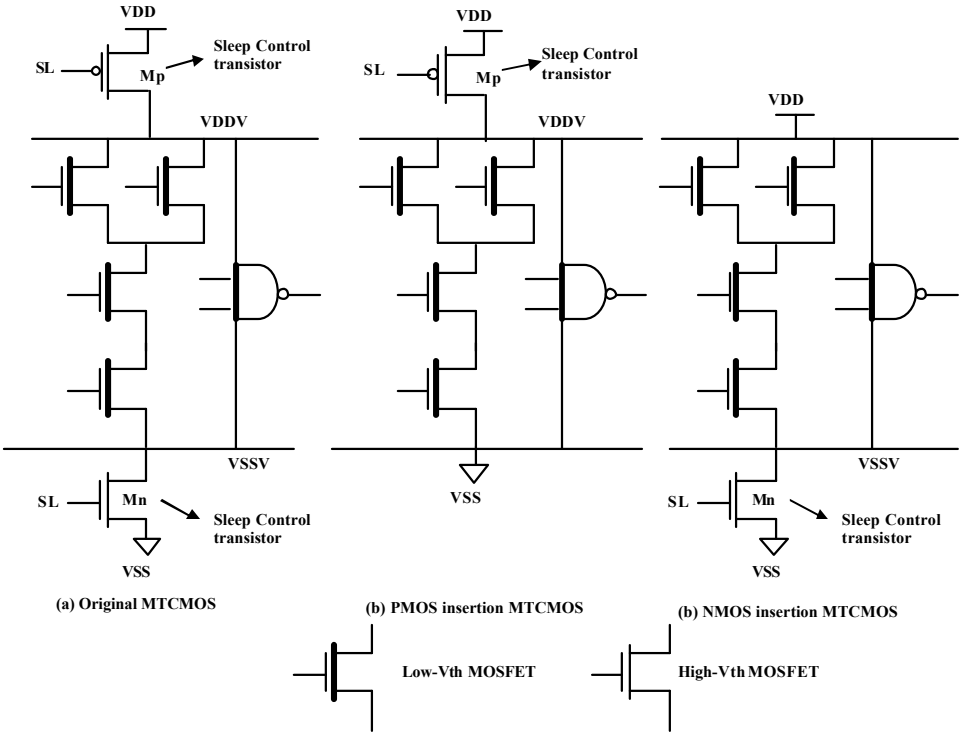

Fig. 3: Schematic of various MTCMOS circuit adapted form Yeo and Roy [7]

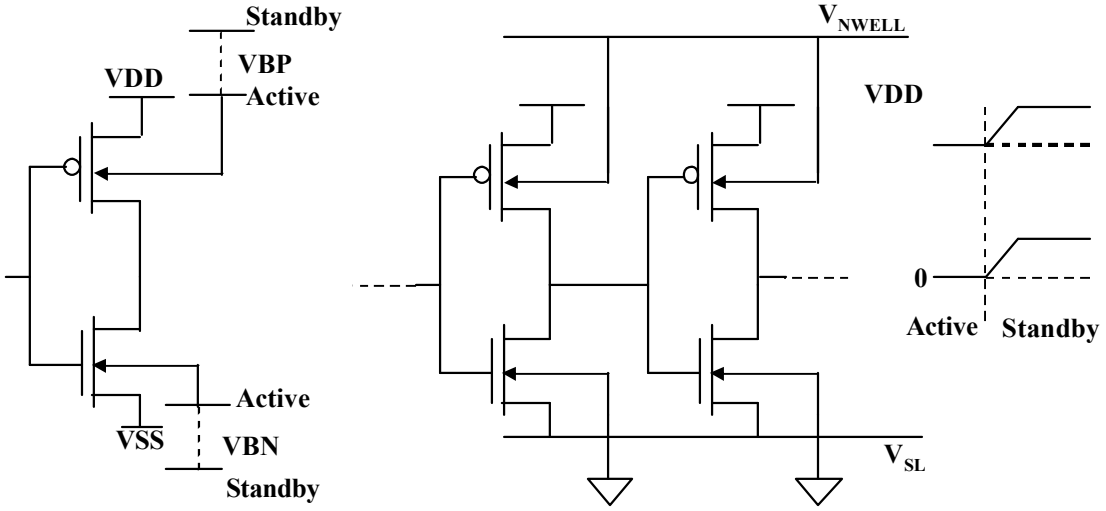

Fig. 4: Forward/Reverse body biasing (VTCMOS) scheme adapted from Yeo and Roy [8]

CMOS (VTCMOS) devices are one solution to this problem. In VTCMOS technique, the threshold voltage of the low threshold devices is varied by applying variable substrate bias voltage from a control circuitry. The only disadvantage of VTCMOS technique is its drawbacks related to manufacturing of these devices which require either twin well or triple well technology to achieve different substrate bias voltage levels at different parts of the integrated circuit. The area overhead of the substrate bias control circuitry is negligible. This approach to reduce leakage current is shown in Fig. 4. VTCMOS circuits do not need any extra circuit to hold the data into latches. Instead of having transistors with different threshold values to minimize leakage currents in sleep mode, such designs control the threshold voltage by changing the back-gate bias. This is controlled by making the substrate voltage lower than ground for NMOS transistors or higher than

VDD for PMOS transistors. VTCMOS circuits impose added complexity of structure, triple well structure and substrate bias voltage generator. The junction leakage current and gate tunneling are larger than normal because of the substrate bias.

Lowering supply voltage: Supply voltage scaling which has originally been developed for the reduction of switching power may be used to reduce leakage power since sub-threshold leakage and the leakage due to DIBL decrease when the supply voltage is lowered. This may be implemented in either a static fashion using multiple power supplies or in a dynamic one using a single power supply but lowering both the voltage and frequency when performance demand is low. This is equivalent to lowering the supply voltage as fast as the circuit goes into the sleep mode and it can be used for reducing the leakage power consumption of VLSI circuits. Of course, in this approach one cannot turn off just small pieces of the circuit since the power supply voltage is common for the whole chip.

Leakage control by adding control pins: This method of reducing the leakage current is similar to vector input control. However, in this method the inner states of the circuit are controlled. These signals can be controlled in two ways, either by multiplexing the signals or by modifying the gates. The multiplexing method is controlled by a sleep signal that is deciding the state of the multiplexer. When the sleep signal is off the circuit operates as normal and when the sleep signal is on a fixed value, it is set as input signal. This input value makes the circuit have the lowest leakage current. Because this value is fixed, it is possible to use either an OR gate or an AND gate. These gates will consume dynamic power when the circuit is in active mode. If the sleep mode periods are long, this extra dynamic power consumption will not be negligible. There will also be extra leakage current in the added gates. A design that takes the extra leakage power into account and finds the optimum solution must be used. By using this method the leakage power can be significantly reduced. Another method is to modify the existing gates. Abdollahi *et al*. [9] showed that it is possible to reduce the leakage current in combinational circuits by an average of 25% with only a 5% delay penalty. They also presented a design technique for applying the minimum leakage input to a sequential circuit where they used the built-in scan-chains in a VLSI circuit to drive it with the minimum leakage vector when it enters the sleep mode, thereby eliminating the area and delay overhead of the additional circuitry that would otherwise be needed to apply the minimum leakage vector to the circuit. The basic idea which they presented was to increase the controllability of the internal signals of the circuit by using multiplexers or modifying the internal gates of the circuit. By using this method, the extra hardware that the multiplexers require can be avoided. The area overhead and leakage current of the extra hardware would be large especially if the number of multiplexers is high. When a high value is wanted in sleep-mode, the existing gate will be replaced by OR and when a low value is wanted the existing gate will be replaced by AND. The transistors will be added in series into the existing gate's N or P network, which is not the same as adding a new circuit. Adding a new transistor to the gate with possibly another threshold value or size can result in serious problems in the circuit due to delay and a large leakage current when the sleep circuit is turned on and off. In the case of sleep circuit, the circuit operates almost as normal when the sleep signal is off.

Power gating has also become an attractive design choice for low-power applications. Singh *et al*. [10] introduced a novel power gating approach to yield an improved power-performance tradeoff in large combinational circuit blocks and latch-to-latch data-paths. They presented a multiple sleep mode power gating technique where each mode represents a different point in the wake-up overhead versus leakage savings design space and showed that the high wake-up latency and wake-up power penalty of traditional power gating limits its application to large stretches of inactivity. The proposed multiple-mode feature allows a processor to enter power saving modes more frequently, hence, resulting in enhanced leakage power savings. Their simulations showed that multiple sleep mode capability provides an extra 17% reduction in overall leakage compared to traditional single mode gating.

Using scan chain for leakage current reduction: Scan chains are used in nearly all electrical circuit to increase the possibility to test inner states of the circuit. These scan chains can also be used to reduce leakage current in sequential circuits. The minimal leakage vector will be applied to control the input values on the sequential circuits. The simplest way to apply this minimal leakage vector is to read it from memory and shift it in by the scan chain. The sleep signal must then be combined with a test-enable signal. After the vector is shifted in, the clock signal can fall in sleep mode to save power.

Source biasing for sub-threshold leakage reduction: Source biasing techniques are a class of circuit techniques that have been proposed by researchers to reduce standby sub-threshold leakage currents. Inserting a switched impedance at the source of a MOS

transistor reduces the standby sub-threshold current by three to four orders of magnitude and suppresses the current variation caused by threshold-voltage and temperature fluctuations. Horiguchi *et al*. [11] proposed a switched-source-impedance (SSI) CMOS circuit as a means of reducing the exponential increase of sub-threshold current with threshold-voltage scaling. The scheme they proposed is applicable to any combinational and sequential CMOS logic circuit as long as their standby node voltages are predictable. Kawahara *et al*. [12] presented analytical expressions for sub-threshold current reduction in a decoded-driver by self-reverse biasing, which is inherently required for low-voltage, low-power, high-speed DRAM's for portable equipment. The scheme proposed involved inserting a switching MOS transistor between the driver circuits and its power supply line. The sub-threshold current of the decoded-driver was thus reduced to the order of 10^{-3} in the practical temperature range (250-350 K) with 254 mV of self-reverse biasing voltage, while the delay time was only 3% more than in conventional schemes. Ye *et al*. [13] presented stack effect and Keshavarzi *et al*. [14] presented optimum reverse body bias as other attempts in source biasing all relying on an underlining source biasing principle to reduce sub-threshold leakage currents.

In source biasing, the main idea is to bias the source of the transistor of an off device in order to reduce the leakage current exponentially. This would be very effective for placing a circuit block in a low leakage state during the standby mode.

Switched source impedance techniques utilize a large switched impedance that can be placed in series with an off low V_t transistor during the standby mode and it is bypassed during the active mode. This will cause the standby leakage currents to decrease, but still maintain high performance during the active mode.

Self reverse biasing technique simply replaces the switched source impedance with another off transistor, so that the equilibrium value is set through the series of off devices. The stacking effect is the reduction in sub-threshold current observed when multiple transistors connected in series or in a stack are turned off.

The disadvantages of source biasing for sub-threshold leakage reduction are smaller voltage swing (IR drop on sleep transistors), lower performance, increased noise coupling and a need for local power grid design.

Input vector control: Abdollahi *et al*. [8] and many others have tried to estimate the minimal and maximal power consumption of a sleep-mode circuit since the leakage current of a circuit can be minimized when the input vector is changed due to stacking effect of transistors. One may get a ten times difference by just looking at different input combinations in a sleep mode NAND gate, for example, as shown in Table 1 adopted from Kleist A. [15]

Table 1: The leakage current in a three-input NAND gate adopted from Kleist [15]

State	Leakage [pA]
000	3.21
001	4.62
010	4.67
011	3.13
100	6.47
101	3.21
110	3.67
111	3.23

Kleist [15] expressed that the best solution will be to find the maximum number of off transistors in all stacks in the circuit for the leakage current to be the smallest. When this vector is found it is possible to apply it to a circuit directly when it switches into sleep mode. One way to find the best vector is to do an exhaustive testing on the circuit to find out which combination is the best combination. Although this seems to be a simple solution, it is not possible for large circuits. Since two main sources of leakage current are the sub-threshold current and the gate tunneling, both must be taken into account to find the optimum solution.

Body biasing techniques: Another technique for controlling sub-threshold leakage currents is to adjust device body biases (in a triple technology for example) to tune device threshold voltages directly. Unlike dual V_t approaches where explicit high V_t and low V_t devices are used for low leakage and high performance, body biasing techniques use the body terminal bias values as another control mechanism to dynamically tune threshold voltages. For every process technology there is an optimum reverse body bias. Optimum reverse bias value reduces by a factor of 2 for each technology generation and maximum achievable leakage power reduction diminishes by a factor of 4. However, band-to-band tunneling limits the technique's effectiveness and bulk capacitance can be large which increases reverse body-bias switching energy.

The proposed circuit design technique: Sleep mode circuits are used to turn off some parts of a circuit. When a section of the design is not used any more it has to be turned off in a fast and simple way. When this part is started, there should be no large leakage current. The part that is in sleep mode must have a very small

leakage current for the sleep mode to be effective. The most critical part of the sleep mode design is to find a solution that transfers the portion of the circuit that must go "sleep" into this mode without affecting any other parts of the design and the sub-threshold currents must be minimized. When the circuit is in active mode, this sub-threshold current will not be especially important, because most of the current consumed in the circuit is dynamic.

These issues are all considered in our design. The main idea in our proposed circuit design technique is using charge sharing between output capacitors to recover charge stored on the capacitance nodes. Thus after pre-charge, all nodes are set to $V_{DD}/2$ and output capacitor is charged or discharged only from $V_{DD}/2$ to V_{DD} or from $V_{DD}/2$ to 0 respectively. This half- V_{DD} swing ideally reduces active power consumption by 50%. But with technology scaling and reduction of channel length and threshold voltage, leakage current and consequently leakage power which is the dominant portion of consumed power in wide gates will increase dramatically. According to formula (1), it is clear that in order to totally eliminate sub-threshold current, the drain and source voltages must be equal. This is not possible to do, since then we will have no circuit operation at all. However, we set all nodes to $V_{DD}/2$ in sleep mode. This circuit design technique is studied in both active and sleep modes.

Active mode: In active mode input and output signals and their complementary vary from $V_{DD}/2$ to 0 and $V_{DD}/2$ to V_{DD} respectively. All the nodes are set at $V_{DD}/2$ in the precharge phase and the signals are applied at the evaluation phase.

For example, in the AND gate shown in Fig. 5, the output voltage changes only from $V_{DD}/2$ to 0, if An (or Bn) changes from $V_{DD}/2$ to V_{DD} and A (or B) changes from $V_{DD}/2$ to 0. This topology provides faster wide AND gates without signal skew and contention between keeper transistor and pull down network cannot occur due to elimination of keeper transistor in Domino logic. Thus, this topology saves power and reduces delay.

For NOR gates shown in Fig. 6 the evaluation phase changes from $V_{DD}/2$ to 0 and the output voltage is pulled down if one input signal remains at $V_{DD}/2$. A 2-input XNOR gate is shown in Fig. 7 which is suitable to eliminate the signal. Output node (V_o) is pulled down, if A is zero and B remains at $V_{DD}/2$ and vice versa. Because of using two voltage levels in XNOR gates, it is clear that we can have n input XNOR gates.

In gates with fan-in of less than 3, the above circuits are not fast enough and PMOS pull up network must be utilized which is similar with NMOS pull down network.

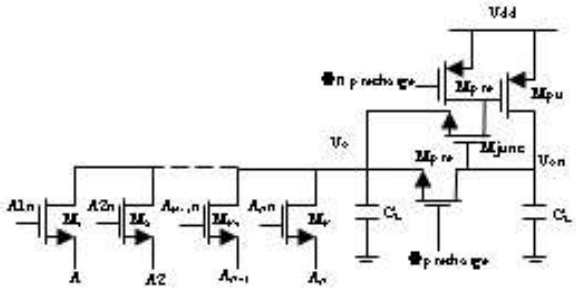

Fig. 5: Fast N-input AND gate

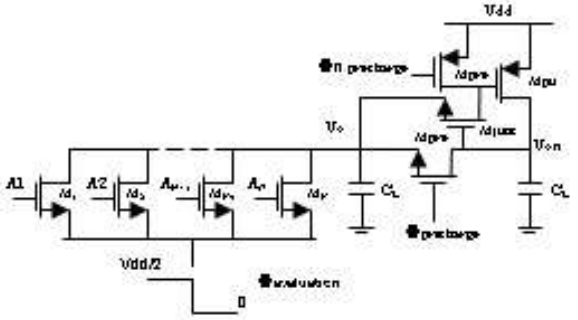

Fig. 6: Fast N-input NOR gate

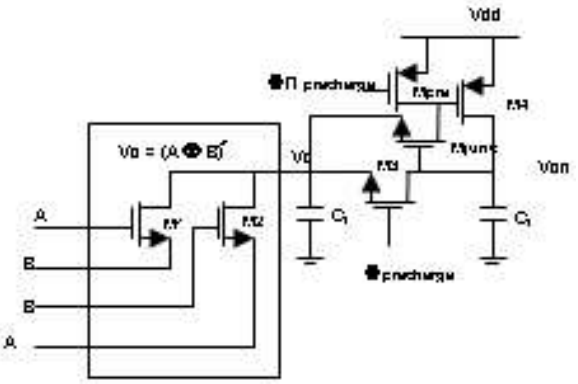

Fig. 7: A 2-input XNOR gate

Sleep mode: In order to switch to sleep mode, after precharge phase, the evaluation phase will be disabled. In this mode all nodes are set to $V_{DD}/2$ and remain at that level until the evaluation phase is enabled. The necessary inputs are kept in high efficient latches and are passed on when the evaluation phase is enabled.

In this mode the sub-threshold current is very small because of equilibrium of drain-source voltages.

COMPUTER SIMULATIONS AND RESULTS

In this section, the leakage power consumption of the proposed circuit technique is compared with other existing circuits such as Multi-Threshold CMOS

Table 2: A comparisons between various wide gate circuits

Logic type	Vdd current (A)	Leakage power (W)	Transistor count	Switching time (s)
Conventional domino	2.9868E-06	4.585E-06	68	0.07E-09
MTCMOS	5.1790E-09	6.739E-08	70	0.5E-09
SSI	2.6973E-08	3.388E-07	69	0.4E-09
CDSM	4.5605E-09	1.367E-07	72	0.2E-09
Proposed circuit technique	4.2757E-09	5.392E-08	68	0.1E-09

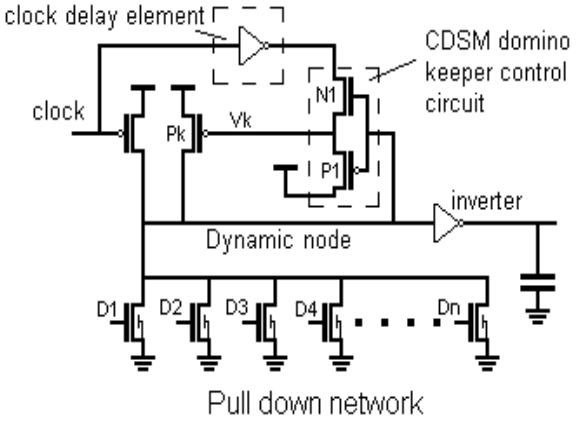

Fig. 8: A wide fan-in CDSM domino OR-gate

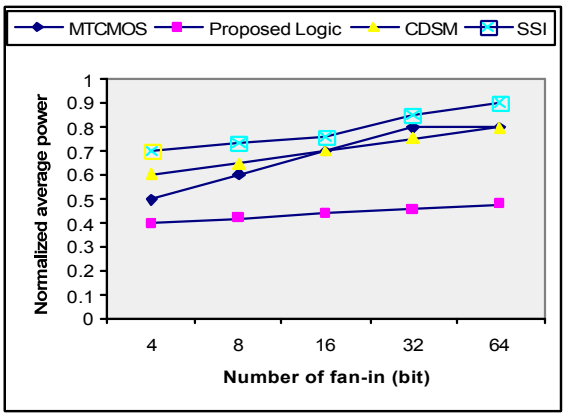

Fig. 9: The normalized power comparison vs. number of fan-in

(MTCMOS), Switched Source Impedance (SSI) and Clock-Delayed sleep mode domino (CDSM) as shown in Fig. 8.

For comparison of performance in the sub 100nm scale, the various circuit techniques were simu lated and studied in the 70nm deep submicron technology using the Zhao and Cao [4] predictive models. The 4, 8, 16, 32 and 64-bit fan-in gates were simulated with 0.9V supply voltage at T=110C°. A comparison between circuits versus V_{DD} current, leakage power, transistor count and switching time, which is needed to switch

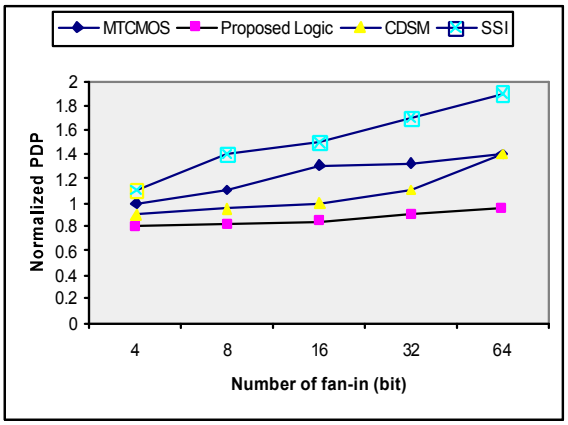

Fig. 10:The normalized Power-Delay Product (PDP) comparison vs. number of fan-in

between active mode and sleep mode is summarized in Table 2. The simulation results show that the proposed circuit takes about the same number of transistors as conventional domino takes, it needs less transistors than other techniques do, it has about the same switching time as conventional domino, but has the least leakage power consumption. Therefore, it has a better performance than existing techniques for wide gates.

Simulation of average power, which is normalized to conventional domino, versus number of fan-in is shown in Fig. 9 which shows that the new circuit technique consumes less average power compared to the other circuits.

The Power-Delay Product (PDP) normalized to conventional domino is shown in Fig. 10. The curves show that the PDP parameter of the new circuit technique is lower than other logic families. Since V_{DS-max} in the proposed circuit technique is $V_{DD}/2$, short channel effects especially hot-electrons are reduced and this results in a better performance. Moreover, leakage power is independent of the input vector and no additional circuits are needed.

These results exhibit the superior performance of our proposed circuit technique in sleep mode. In the novel circuit design technique proposed, the leakage current is very small and the sleep mode power is minimized.

CONCLUSIONS

In this paper, several existing leakage power reduction techniques in sleep mode are discussed and a novel circuit design technique to minimize sleep mode power consumption due to leakage power in the sub-100nm wide gates in CMOS technology is proposed. This circuit technique provides significant energy savings in sleep mode without any speed degradation or die area overhead. Moreover, it is almost independent of technology scaling and has no circuit design complexity. Another advantage of this technique is that it eliminates signal skew problems and switches fast between active and sleep modes without any additional circuits.

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