

A High Step-Up Hybrid DC-DC Converter with Reduced Voltage Stress for Renewable Energy Applications

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Abstract: This paper proposes a high step-up dc-dc converter with voltage-lifted switched inductor cell, switched-capacitor and voltage multiplier cell. The voltage multiplier cell is used to reduce the voltage stress across the switch and to extend the voltage gain. In addition, this converter consists of simple control system, since there is only one active switch. The operating principle, key waveforms and design details are also presented. The proposed topology is simulated in PSIM to verify the performance of the proposed converter.

Key words: Boost converter • Switch voltage stress • Switched capacitor • Switched inductor • Voltage-lift

INTRODUCTION

The International Energy Agency (IEA), forecasts that the global primary energy demand on 2030 increases by 1.5% annually from now. Developing Asian countries are the main contributors to this growth, followed by the Middle East region. Growth in per capita energy consumption in the past two decades has occurred in all parts of the world primarily because of increased participation in the transport sector, followed by manufacturing. Exceptions to this trend are China and India, where growth is mainly taken in the manufacturing sector, followed by the household sector. A large and sustainable economic growth in India is to develop a great demand for energy resources. Demand and the imbalance between the supply of energy sources is a widespread phenomenon that requires serious efforts of the Government of India to increase the energy supply. More than 50% of the population is little or no energy business for life and living. Renewable energy can make a significant contribution in each of the areas mentioned above. In this context, the role of renewable energy must be seen. Alternative energy such as photovoltaic, bio-fuel and chemical energy such as fuel cell become increasingly key part of the solution to the country's energy needs. The renewable energy is an important element in the energy planning process in India for more than two decades.

Power Electronic devices continues to innovate and the importance of switching power converter is increasing, in which boost converter is widely used in renewable energy systems. In order to boost the available low voltage to high voltage of 380 V, which is required by the full-bridge inverter to connect with a 220 V grid. A huge number of dc-dc converter topologies were proposed and implemented in the range of hundred watt to multiples of kW. The dc-dc converters are generally classified in to two: isolated converters and non-isolated converters. The isolated converters use transformer for isolation which may be necessary or not in some countries. In order to reduce the cost of the system without compromising gain and efficiency, the non-isolated dc-dc converters are to be used in renewable energy applications [1, 2]. The non-isolated dc-dc converters are classified into five categories, such as cascaded dc-dc converter, coupled inductor based boost converter, switched capacitor (SC) based boost converter, switched inductor (SL) based boost converter and voltage multiplier (VM) cell based boost converter.

The conventional boost converters are cascaded in series and/or parallel to increase the voltage gain of the converter [3-5]. The cascaded converters consist of large number of components, so it is not suitable for high power applications. Coupled inductors are a different method used to increase the voltage gain, reduce the reverse recovery problem of the output diode and to

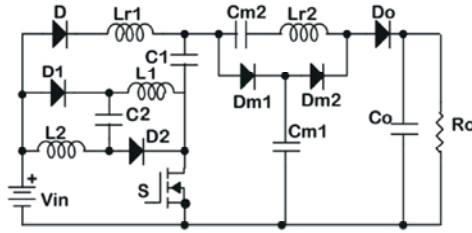


Fig. 1: Proposed Voltage-Lifted Switched-Inductor-Capacitor (VLSIC) converter

reduce the input current ripple [4-8]. The capacitors are switched to charge and discharge in a dc-dc converter to increase the voltage gain. The switched capacitor converter requires a large number of components to achieve high output voltage, which in turn increases the cost, weight and volume of the converter [9-12]. The switched inductor (SL) and voltage-lifted switched-inductor (VLSI) based converters have been explored [13-16]. The voltage multiplier cells are incorporated in the boost converter topologies to increase the voltage gain as well as to reduce the voltage stress across the switch [17-20].

The proposed voltage-lift switched-inductor-capacitor converter is different from existing high step-up dc-dc converters and it is derived from the topology proposed in [21]. The proposed converter has less voltage stress in the power switch and the voltage gain is high when compared to conventional boost converter adopted with any of the techniques like SL, SC, VM and VLSI. This paper is organized as follows. The topology and operation of the proposed converter are presented in section 2. The analysis and expressions for the voltage gain and voltage stress are given in section 3. The simulation results and the performance evaluation are given in section 4. Finally, this paper is concluded in section 5.

Proposed Converter: The topology proposed in [21] is modified by replacing the switched inductor cell with voltage-lift switched inductor (VLSI) cell and it is given in Figure 1. The VLSI cell is formed by D_1 , D_2 , L_1 , L_2 and C_2 . The capacitor C_1 forms the switched-capacitor (SC) cell. The main purpose the inductors, L_r is to reduce the current peak formed by the capacitors in SC and VM cells. The VLSI and SC cell are connected in parallel with the source when they are charging and they are connected in series when discharging. The resonant inductor forms a tank circuit and we have to ensure that the zero crossing of inductor current before the switch is turned off.

Operating Principle: The assumptions made to analyze the circuit are as follows: All the converter components are ideal; The inductors and capacitors are very large, then the voltage across capacitor and current through the inductor will be constant and continuous. The operating modes of the proposed topology are shown in Figure 2.

Mode 1 (t_0 - t_1): In this mode, the power switch, S is in turned off condition. The diodes D_{M1} and D_O are forward biased and diodes D and D_{M2} are reverse biased. The capacitor C_1 , the inductors L_1 and L_2 are connected in series with the input voltage source as shown in Figure 2(a). The energy stored previously in the capacitor, C_1 is discharged to C_{M1} through D_{M1} , to capacitor C_{M2} through L_{r2} and to output capacitor C_O through D_O . The current in the resonant inductor L_{r2} (i_{Lr2}) is increased up to the level of VLSI cell input current and simultaneously the current in the diode D_{M1} is reduced. This change in current occurs in linear manner. Simultaneously, the voltage across the multiplier capacitor, C_{M1} is increased and across multiplier capacitor, C_{M2} is decreased and the voltage across resonant inductor, L_{r2} is constant in this mode.

Mode 2 (t_1 - t_2): At instant t_1 , the diode current i_{DM1} is zero and the current i_{Lr2} and VLSI cell inductor current are equal as shown in Figure 3. The energy stored in the VLSI cell inductors are transmitted to load though the output diode D_O . The inductor current and the capacitor voltage both decreases at the instant t_2 .

Mode 3 (t_2 - t_3): At the time instant t_2 , the switched is turned on. The diodes D_{M1} and D_O are reverse biased; D_{S1} , D_{S2} , D_{M2} and D are forward biased. The VLSI cell inductors and the capacitor C_1 forms the tank circuit. The tank circuit will cause a sinusoidal resonant current in C_1 and the VLSI cell inductor current will increase as shown in Figure 3. Once the amplitude of current oscillation reaches zero, the diode, D is reverse biased. The energy stored in the C_{M1} is transferred to C_{M2} through D_{M2} until the time instant t_3 . Once the energy is fully transferred from C_{M1} to C_{M2} , the diode D_{M2} is reverse biased. The average output voltage will appear across the output capacitor C_O and it will be the sum of the voltage across the capacitor C_{M2} and the voltage at the input of multiplier cell.

Mode 4 (t_3 - t_4): Once the resonance condition stops in the VLSI cell, the power switch, S continues to conduct. So the VLSI cell inductor current increases further. Since the capacitor is fully charged, there will be no current flowing through it. Similarly, at t_3 , the current in

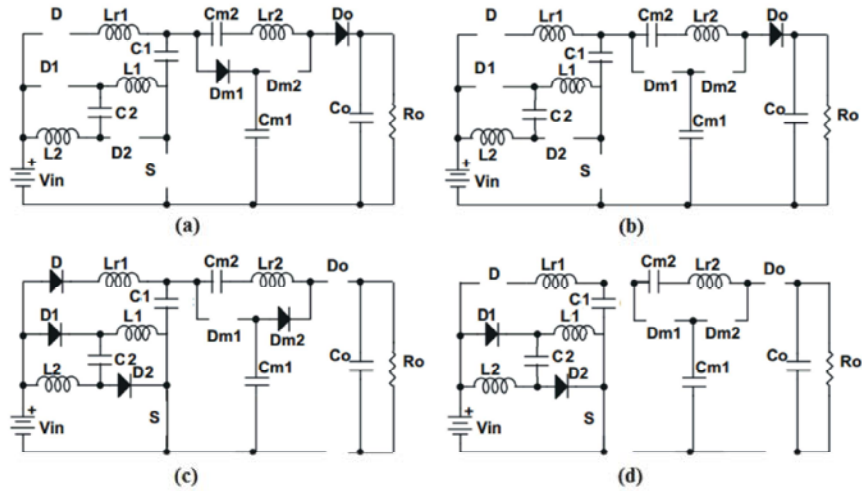


Fig. 2: Operating modes of the proposed converter. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4

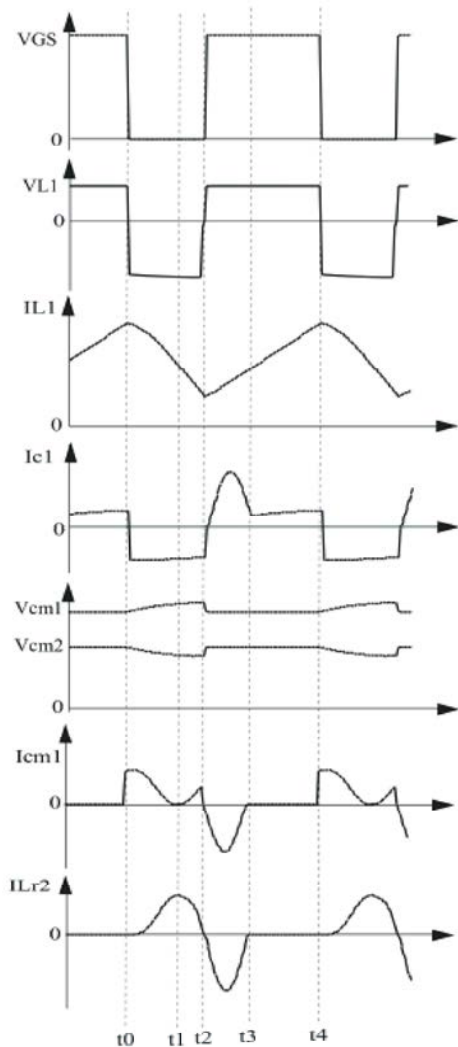


Fig. 3: Theoretical waveforms of the proposed converter

the resonant inductor L_{r2} is zero and in turn it reverse biases the VM cell diode, D_{M2} . Therefore, the output circuit is completely isolated from the source, the VLSI cell inductors will charge from the input voltage source. The VLSI cell and switched capacitor cell will remain in this state until the switch is turned off as shown in Figure 3. Once the switch is turned off, the above four modes will be repeated. Since the diodes in the VLSI and VM cells are turned off naturally, the reverse recovery problems are alleviated.

Analysis and Design Specifications: During switching-on period, the capacitors C_1 and C_2 are charged from the input voltage V_{in} as shown in Figure 2(c), since the capacitors are sufficiently large, both voltages are equal.

$$VC_1 = V_{in} \quad (1)$$

$$VC_2 = V_{in} \quad (2)$$

$$V_{CM2} = V_{CM1} V_{in} \quad (3)$$

The inductor current increases during the on period and decreases during the off period of the power switch, S. The voltage appears across the inductors L_1 and L_2 during on period is V_{in} .

$$V_{L1} = V_{L2} = V_{in} \quad (4)$$

From Figure 2(a), the voltage across the inductor L_1 or L_2 during off state is given by.

$$V_{L1} = V_{L2} = \frac{V_{CM1} - V_{in} - VC_1 - VC_2}{2} \quad (5)$$

Table 1: Comparison of proposed converter and other converters

Converter	Conventional boost converter	Converter proposed in [22]	Converter proposed in [23]	Converter proposed in [24]	Converter proposed in [21]	Proposed converter
Voltage gain	2.5	7	6	7.5 for n=2	9	11
Output voltage	30 V	84 V	72 V	90 V	108 V	132 V
Voltage stress of active switch	7.2 V	48 V	30 V	30 V	48 V	42 V
Voltage stress of output diode	7.2 V	96 V	-	-	48 V	60 V
Voltage stress of intermediate diodes	-	12 V	30 V	30 V	12 V	
				48 V	18 V	30V
				60 V	48 V	60 V

And the output voltage is equal to the sum of multiplier capacitor voltages.

$$V_O = V_{CM1} + V_{CM2} \quad (6)$$

From (1) and (2), the inductor voltage can be rewritten as;

$$V_{L1} = V_{L2} = \frac{V_{CM1} - 3V_{in}}{2} \quad (7)$$

By applying the volt-second balance principle, the voltage across the inductor is given by;

$$DV_{in} = (1-D) \frac{V_{CM1} - 3V_{in}}{2} \quad (8)$$

Hence, the voltage across the multiplier capacitor, C_{M1} is;

$$V_{CM1} = \frac{(3-D)V_{in}}{1-D} \quad (9)$$

Substituting (9) in (3) gives the voltage across the multiplier capacitor C_{M2}

$$V_{CM2} = \frac{2}{1-D} \quad (10)$$

Substituting (9) and (10) in (6), the output voltage is;

$$V_O = \frac{5-D}{1-D} V_{in} \quad (11)$$

Therefore, the voltage gain of the proposed converter is;

$$G = \frac{5-D}{1-D} \quad (12)$$

From Figure 2(a), the voltage stress on switch, S is given by;

$$V_S = V_{CM1} - V_{C1} = \frac{2-D}{1-D} V_{in} \quad (13)$$

Also from Figure 2(a) the voltage stress across the diode D_{M2} is;

$$V_{DM2} = V_O - V_{CM1} = V_{CM2} = \frac{2}{1-D} V_{in} \quad (14)$$

From Figure 2(c) the voltage stress across the multiplier diode D_{M1} and output diode D_O is calculated.

$$V_{DM2} = V_{CM1} - V_{C1} = V_{CM2} = \frac{2}{1-D} V_{in} \quad (15)$$

$$V_{DO} = V_O - V_{CM1} = V_{CM2} = \frac{2}{1-D} V_{in} \quad (16)$$

The voltage stress on the diodes D_1 and D_2 are

$$V_{D1} = V_{L2(Mode\ 1)} + V_{C2} \quad (17)$$

$$V_{D2} = V_{L1(Mode\ 1)} + V_{C2} \quad (18)$$

$$V_{D1} = V_{D2} = \frac{V_{in}}{1-D} \quad (19)$$

From (13) to (19), it is clear that the voltage stress across all the semiconductor devices are lesser than the half of the output voltage. Table 1 gives the comparison of voltage gain and voltage stress across the semiconductor devices of the proposed converter with conventional boost converter and various converter topologies proposed in [21-25], when operating at duty cycle of 0.6 with 12 V input.

Simulation Results: In order to verify the theoretical analysis and the performance of the converter, the proposed converter is simulated in PSIM v9.0. The circuit parameters are calculated from the design equations and they are: $V_{in} = 12$ V, $L_1 = L_2 = 44$ μ H, $C_1 = C_2 = 47$ μ F, $C_{M1} = C_{M2} = 1$ μ F, $C_O = 220$ μ F, $L_{r1} = L_{r2} = 1$ μ H, $R = 60$ Ω . The switching frequency and the duty ratio are selected as 100 kHz and 0.6. Figure 4 shows the gate drive voltage of the power switch, output voltage and current and the voltage stress across the output diode. The output voltage is 132 V and it is equal to the theoretical value calculated by using the voltage gain formula. The ripple in the output voltage is very low and it is in acceptable limit.

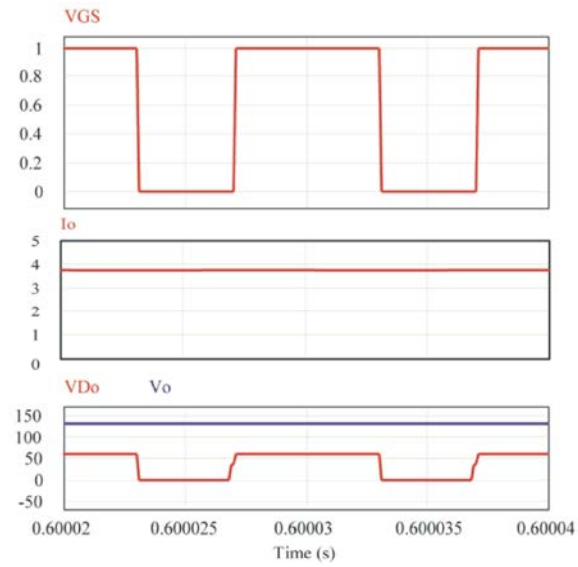


Fig. 4: Gate voltage, output current, output diode voltage stress and output voltage of the proposed converter

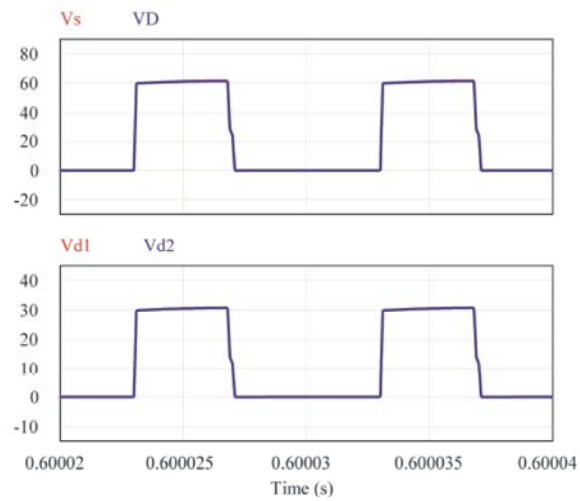


Fig. 5: Voltage stress across the semiconductor devices of the proposed converter

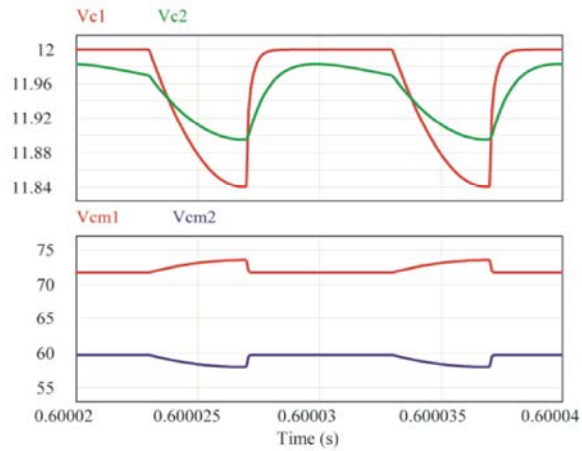


Fig. 6: Voltage across the various capacitors of the proposed converter

The voltage stress across the output diode is 60 V that is lower than the output voltage. Figure 5 shows the voltage stress across the switch and diodes and they are also lesser than the output voltage. Therefore, the switch and diodes with low R_{DS-on} can be used to reduce the cost and conduction losses of the converter. The voltage across the capacitors are shown in Figure 6 and its values validate the theoretical analysis. The voltage across all the elements and devices in the simulation results are same as theoretical results.

CONCLUSION

In this paper, a new high step-up converter that can be used in renewable energy applications is proposed. The proposed converter topology has the capability to obtain high voltage gain in low duty cycle. This converter has low voltage stress on the switch and diodes and hence the semiconductor devices with low turning-on resistance can be used to reduce the conduction losses. The converter consists of only one power switch which makes its control easy. The operation of the converter is presented and it is simulated in both PSIM and Multisim. The simulation results confirm the theoretical analysis and performance of the proposed converter and it is evident that the proposed converter can be used in wide areas where large dc-dc gain is required.

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