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Low Power Circuit Design Using TSG and Fredkin Gate

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Abstract: Reversible logic has a greater ability to reduce the power dissipation which is the main requirement in low power VLSI design. By implementing this reversible logic in carry bypass and carry select adder, the area of the circuit and delay produced in the circuit and the power dissipation can be significantly reduced. It is shown that the adder architecture designed using reversible gates are much better and optimized as compared to existing four bit Carry bypass and select Adder in terms of low power dissipation, area and delay. In this paper reversible gates such as Fredkin, Toffoli and TSG gates are used to design carry bypass and carry select adder blocks. Tools required for designing reversible gate is Tanner EDA

Key words: Reversible Logic · TSG · Fredkin · Reversible adders

INTRODUCTION

Reversible logic gates are very much in demand for the future computing technologies as they are known to produce zero power dissipation under ideal conditions. This paper proposes an improved design of adders using reversible logic gates. Adders are very essential for the construction of various computational units of a quantum computer. The quantum cost of a reversible logic circuit can be minimized by reducing the number of reversible logic gates.

Reversible logic is considered as the emerging technologies in the field of optical computing, low power design and Nano electronics. In processing systems, adder plays an important role.

Reversible computation in a system can be performed only when the system comprises of reversible logic gates. These circuits can generate unique output vector from each input vector and vice versa, that is, there is a one-to-one mapping between input and output vectors. Landauer [1] has shown that for irreversible logic computations, each bit of information lost generates kTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [1]. Bennett showed that $kTln_2$ energy dissipation would not occur, if a computation is carried out in a reversible way [2], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. It has been shown that reversible logic helps in saving this energy using charge recovery process [5]. Recently, transistor realizations of online testable reversible logic gates are shown in [11, 12]. Hence in this work, we are going to propose an efficient adder design using carry skip adder and carry select adder and implemented it in reversible logic. The most significant aspect of the proposed gate is that it can work singly as a reversible full adder, that is reversible full adder can be implemented with a single gate. The design to be proposed gives minimum number of gates, garbage outputs and quantum cost there by reducing the power consumption, area, delay.

The paper is organized as follows. Section II, presents the reversible gates. The carry skip adder is presented in Section III. Section IV presents the carry select adder. In Section V, simulation results for carry select and carry skip adder are presented. Section VI provides our conclusions.

Reversible Fredkin,toffoli Andtsg Gates: A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely

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recovered from the outputs. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits, the number of Reversible gates (N), the number of constant inputs (CI), the number of garbage outputs (GO), quantum cost (QC).

The reversible TSG, Fredkin and Toffoli gates are used for implementation of carry select and carry skip adders. In this paper first the TSG, Fredkin and Toffoli gates are simulated using Tanner tool and then these blocks are used for designing adders.

A.toffoli Gate: Figure 1 shows a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O (P,Q,R). The outputs are defined by P=A, Q=B, R=AB C. Quantum cost of a Toffoli gate is 5.

B.fredkin Gate: Figure 2 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A'B AC and R=A'C AB. Quantum cost of a Fredkin gate is 5.

C.Tsg: Figure 3 shows a ' 4*4' one through reversible gate called TS gate(TSG). The TSG gate can implement all Boolean functions. One of the prominent functionality of the TSG gate is that it can work singly as a reversible Full adder unit. It can be verified that input pattern corresponding to a particular output pattern can be uniquely determined.

The proposed full adder using TSG, which requires only one reversible gate (one TSG gate) and produces only two garbage outputs(garbage output is the gate output that is not used as input to another gate or as a primary output). It has been shown in [6, 7, 8] that the reversible full-adder design using TSG gate is better than the previous full-adder designs.

Carry Skip Adder: The block diagram of carry skip adder is as shown in Figure 4. In 4 bit carry skip adder four full adders and one multiplexer is used. The selection line for multiplexer is obtained from product of propagation constants of the inputs. Propagation constant is nothing but the ex-or operation of the inputs. If the product of all propagation constants is 1 then the carry output is directly selected from input carry. If the product of all propagation constants is 0 then the carry output selected by multiplexer is from the output of last full adder. So here is multiplexer is used for bypass the carry. The hardware cost of bypass adder is less.

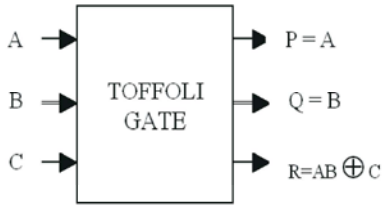

Fig. 1: Toffoli gate

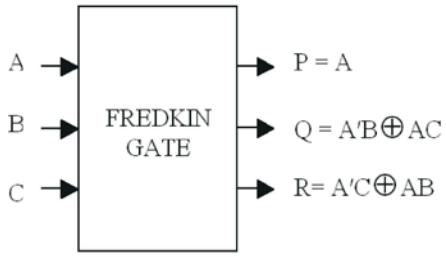

Fig. 2: Fredkin gate

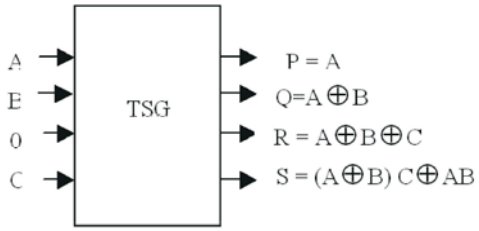

Fig. 3: Proposed TSG Gate

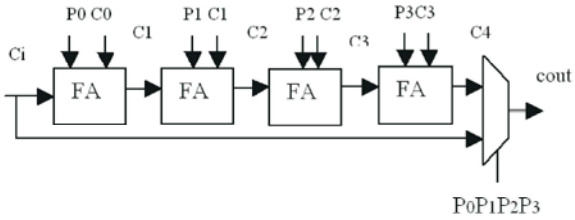

Fig. 4: Carry skip adder structure

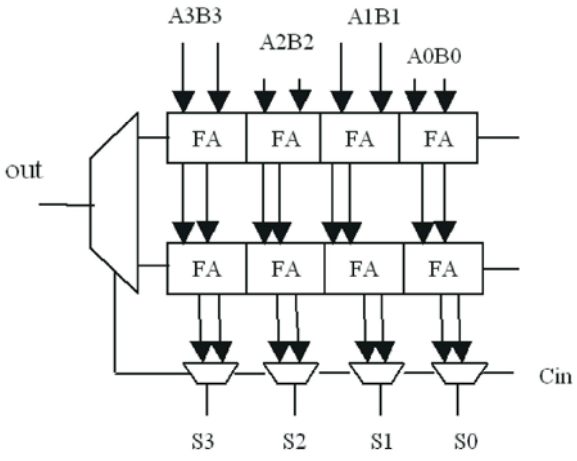

Fig. 5: Carry select adder structure

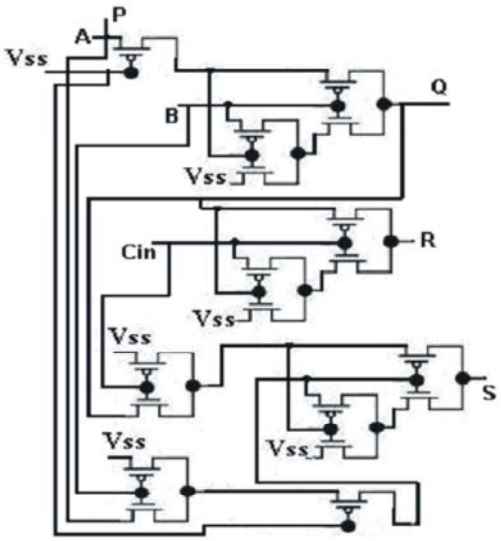

Fig. 6: Transistor Implementation of TSG as a Full Adder

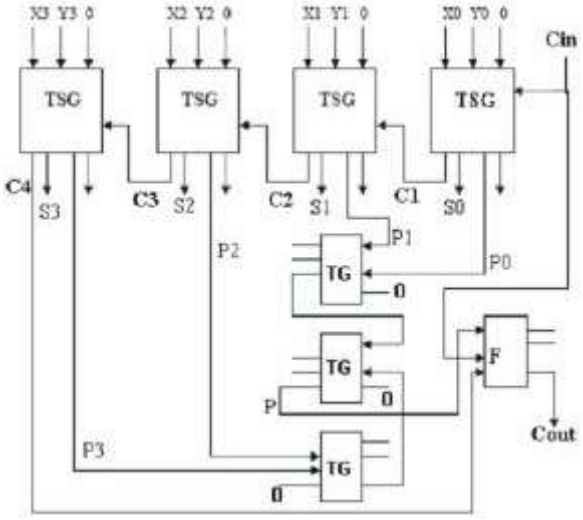

Fig. 7: Proposed Four Bit Carry Skip Adder Block TSG, Toffoli(TG) and Fredkin (F) gates.

Carry Select Adder: The block diagram of carry select adder is as shown in Figure.5.In 4 bit carry select adder four full adders and five multiplexers are used. The reason for going to carry select adder is to reduce delay. The input carry is given as common selection line for all multiplexers. In this two ripple carry adders are used. For first RCA input carry taken as 0 and for second RCA input carry taken as 1. The area of carry select adder is more because of two RCAs are used. The sum output selected by the multiplexer is depending on carry of input data. If Cin is 0 the sum output selected by multiplexer is from first RCA and if Cin is 1 the sum output selected by multiplexer is from second RCA.

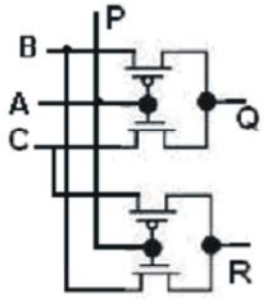

Fig. 7(a): Transistor Implementation of Fredkin Gate

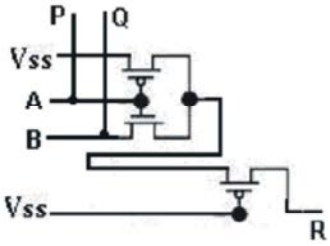

Fig. 7(b): Transistor implementation of Toffoli Gate as a reversible AND gate

Simulation Results Using Reversible Logic

A. Tsg Gate: TSG gate work as a reversible full adder with two garbage outputs. When implementing TSG as a reversible full adder, zero is passed to its third input which reduces the computation complexity at the output of TSG, to make it work as a full adder. Thus, directly implementing TSG as a reversible full adder will lead to transistor overhead. This overhead can be reduced by carefully examining the transistor implementation of TSG gate and removing those transistors which are not involved in the computation, when TSG is working as reversible full adder. The optimized structure of TSG gate working singly as a reversible full adder is shown in Figure 6 which is implemented with only 18 transistors thus avoiding the transistor overhead. This technique will also significantly reduce the transistor overhead when realizing the reversible circuits.

B. Carry Skip Adder: The carry skip adder using reversible gates is obtained with four TSG gates, three TOFFOLI gates one FRDKIN gate. Here Four TSG gates is used as full adder generate different propagate signal and three TOFFOLI gates are used for generating the AND4 operation, which was required to generate block propagate (P) signal. Fredkin gate is used to generate AND and OR operation to generate Cout. Simulation result of Four Bit Carry Skip Adder Block is shown in Figure7.

Table 1: Comparative Result of full adder circuit

Designs	Transistor Count	Power(uw)	Delay(ns)	PDP
Proposed design	18	0.1789	0.1922	3.438
Existing design	28	1.0205	2.2618	2.308

Table 2: Comparative Result of Carry Skip Adder circuit

Designs	Transistor Count	Power(mw)	Delay(ns)	PDP
Proposed design	85	0.278	1.554	4.324
Existing design	174	20.77	7.656	1.590

CONCLUSION

Thus the reversible full adder and carry skip adder circuit was optimized using the properties of Toffoli gate (TG), Fredkin gate (FG), TSG gates. Reversible logic circuits seeking to minimize information loss and hence offer a promising design approach for low-power computing. Optimization criteria are to minimize power, delay, area, Gate counts and Garbage outputs. The TSG Gate is used as a full-adder. The output was simulated using TANNER version 15 and the delay, power was also found to be reduced when compared to existing circuits.

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