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Soft Error Analysis of Multi-Gate MOSFETs

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Abstract: The continuous scaling of classical CMOS features has led to a large reduction in the node capacitances of VLSI circuits. As a result, a small amount of charge deposited by a radiation strike is sufficient to cause an single event upset at the node. Moreover, the increased clock frequency and the reduced supply voltage requirement also aggravate the tolerance of the circuits to SEUs. After we have reached the end of the technology road-map for the conventional CMOS, multiple gate MOSFETs (MuGFETs), will almost certainly take up the baton. This promising solution manifests a superior control of short-channel effects, resulting from an improved electrostatic coupling between the conduction channel and the surrounding gate electrode. In this paper, the influence of the key design parameters of a multiple gate MOSFET on soft error robustness of an inverter circuit has been investigated. It was found that the sensitivity of a node to a single event upset can be reduced by increasing the rate of removal of the charge collected at a node by a particle strike. For instance, this can be done by increasing the effective width of the devices and the operating voltage.

Key words: MuGFETs · Soft Error · Single Event Upset · Reliability

INTRODUCTION

The constant scaling of device features has led to a substantial reduction in the node capacitances of integrated circuits (ICs) and hence the charge stored. Subsequently, the robustness of circuits is decreased in terms of the energetic particle strikes that produce soft errors [1-3]. In previous technologies, this drawback was limited to hostile environmental surroundings' applications, for instance, space electronics. Unfortunately, the effects are increasingly being confirmed at earth level [4, 5].

Moreover, the higher clock frequency and the lowered supply of voltage demands have even exacerbated the sensitivity of electronic circuits to radiation-induced soft errors [2, 6-8]. Additionally, it is worth mentioning that the likelihood of low energy particles is much greater than that of high energy particles [9, 10]. Soft errors are certainly a major threat to vital applications where reliability is the central concern, instead of performance and cost, such as in biomedical or avionics applications.

Generally speaking, single event upsets in microelectronic circuits are, in fact, triggered when radiation particles such as protons, neutrons, alpha particles or heavy ions, strike susceptible regions (typically reverse-biased p-n junctions) in digital circuits. The particle strikes have the ability to deposit a charge at the impacted node, which results in a voltage pulse or glitch, which in turn can lead to a soft or transient error [11].

There are numerous techniques suggested by circuit designers to effectively eliminate the challenge associated with soft errors in conjunction with the obstacles of future circuit design [12]. Critical features such as low power, which is correspondingly viewed as one of the most critical parameters for future circuit applications [13], may mean a different path might turn out to be incorporated and to avoid such issues; to utilize totally different materials and device structures, for instance, MuGFET devices.

For the past tens of years, the continuous progression of planar bulk CMOS technology has already fuelled the expansion of the microelectronics market place.

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After we have reached the end of the technology road-map for the conventional CMOS, multiple gate MOSFETs (MuGFETs), will almost certainly take up the baton. A number of different MuGFET structures and two different modes of operation are increasingly being pursued in the industry these days. In the case of a horizontal double gate (DG), the two gates will likely be asymmetric, having different work functions and existing dielectric thicknesses. Moreover, the two gates could possibly be biased at two different voltages, often known as independent gates. In the other double, triple or potentially all-around gate cases, the gates are biased at the identical voltage, referred to as common gate. Some designs will make use of a lightly doped body to maximize mobility, whilst others can use very high doping concentrations in a thin body to obtain an adequate threshold voltage adjustment [14].

In this paper, the influence of the key parameters of a multiple gate MOSFET on soft error robustness of an inverter circuit has been investigated.

Soft Error Analysis: In studying the robustness of an inverter based on different structures of multiple gate MOSFETs (MuGFETs) to an SEU, circuit simulations have been undertaken using BSIM-CMG models [14] with a single event strike modeled as a double exponential current source [15], as illustrated in Figure 1, with a fast rise and slow fall times using equation (1).

$$i_{soft\_error}(t) = \frac{Q}{\tau_a - \tau_b}(e^{\frac{-t}{\tau_a}} - e^{\frac{-t}{\tau_b}}) \quad (1)$$

Where Q is the charge deposited by a single event strike, τ_a is the collection time constant and τ_b is the ion-track establishment time constant.

The current source is directly connected to the Out node of the inverter circuit as shown in Figure 1. This node was selected as it consists of a reversed biased pn junction (where the N-MOSFET transistor is off) among the other nodes in the inverter circuit. In other words, this node is significantly more vulnerable to the effects of a particle strike on the circuit. The time constant parameters τ_a and τ_b are taken as 250ps and 10ps respectively. The peak of the current source is varied iteratively to determine the minimum amount of charge that leads the output node to flip its logic value and is termed as a critical charge Q_{crit}.

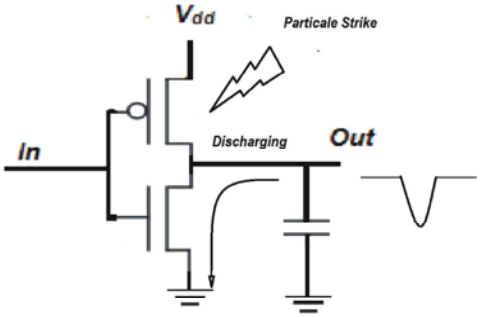

Fig. 1: Schematic view of how SEU-induced current pulse translates into a voltage pulse in a CMOS inverter.

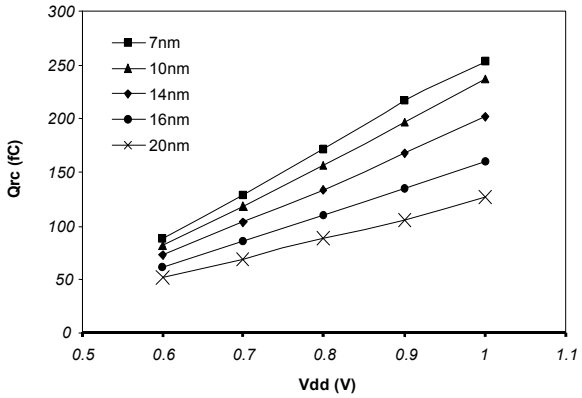

Fig. 2: The impact of power supply variations on the circuit robustness to SEU for different technology nodes.

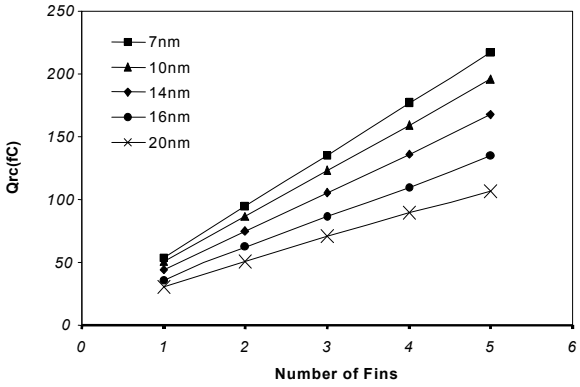

Fig. 3: The impact of the number of fins on the circuit robustness to SEU for different technology nodes.

Figures 1,2,3,4 and 5 show the influence of key circuit and device parameters, such as supply voltage V_{dd}, the number device of fins, the number of device figures and fin pitch of both PMOS and NMOS devices on the critical charge in the inverter circuit, which is realized in MuGFET technology.

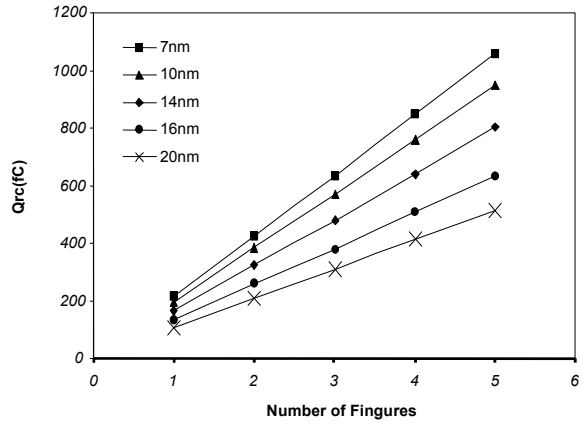

Fig. 4: The impact of a number of device fingers on the circuit robustness to SEU for different technology nodes.

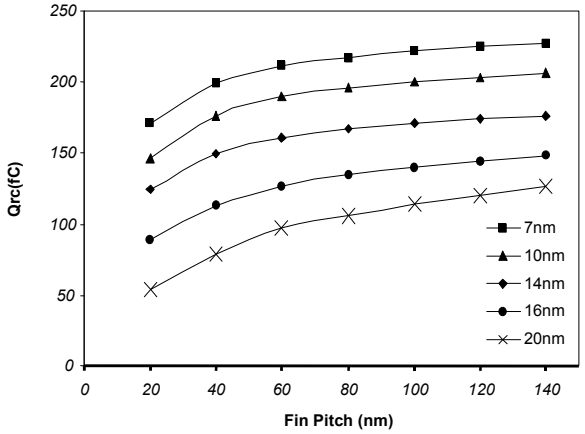

Fig. 5: The influence of fin pitch on the critical charge needed to create an SEU for different technology nodes.

Figure 2 shows that as the supply voltage V_{dd} of the circuit increases the robustness of the inverter, in terms of the critical charge increases, leading to a substantial improvement in the circuit's robustness to a particle strike. Figure 3 shows that as the number of fins of the transistor increases, the critical charges that were required to cause a single event upset in the circuit increases, leading to a positive improvement in the circuit's robustness to a particle strike. This might be explained by the fact that increasing the fins of the device will significantly increase the effectiveness of the restoring devices (PMOS). Similar effects can possibly be noticed from Figure 3 when the number of figures of the PMOS and NMOS devices is increased. Additionally, it can be concluded from the Figures 2, 3 and 4, that using smaller device geometries can promote significant changes in the resilience of the circuit to SEU. This might be explained by the fact that the current strength of the restoring device, here a PMOS transistor, is clearly increased as the device size is reduced; this is often despite the reduction incurred in node capacitances as a consequence of device scaling, together with the increased probability of SEU as the source/drain areas are decreased as a result of scaling.

From the above results, it can also be seen that using a higher power supply voltage increases the robustness of the circuit to soft errors. Moreover, increasing the number of fins, fin pitch and the number of fingers of the MG devices will increase the size of the pull–up transistors, subsequently increasing the PMOS/NMOS width ratio, which greatly improves the robustness of the inverter to soft errors, as shown in the Figures 1-5.

This can be explained by expressing the current at the output node when a particle strike hits this node as in Equation (2):

$$C_{out}\frac{dv_{out}}{dt} = i_{PMOS} - i_{soft\_error} \quad (2)$$

Where C_{out} is the capacitance at output node and v_{out} is the voltage at output node, while i_{PMOS} represents the current needed to charge up the output node and $i_{soft\text{-}error}$ that is given in equation (1).

From equation (2), by increasing the strength of the restoring devices i_{PMOS}, it is possible to increase the rate of the removal of the charge collected at a node and thus decrease the sensitivity of the node to a single event upset. In particular, it is possible to improve the robustness of a circuit to soft errors by firstly increasing the total node capacitance. This can be done by connecting a capacitor to the selected node. However, this will degrade the circuit's performance in terms of delay and dynamic power consumption; secondly, increasing the driving strength, that is i_{PMOS} of the restoring devices that supply charges to the node exposed to a single event strike.

From equation (2), the robustness can possibly be improved by increasing the fin width of the devices as shown in Figure 6.

Figure 7 shows the impact of device gate length on SEU robustness of the inverter circuit; it is possible to realize that the critical charge can be increased by reducing the gate length of the devices.

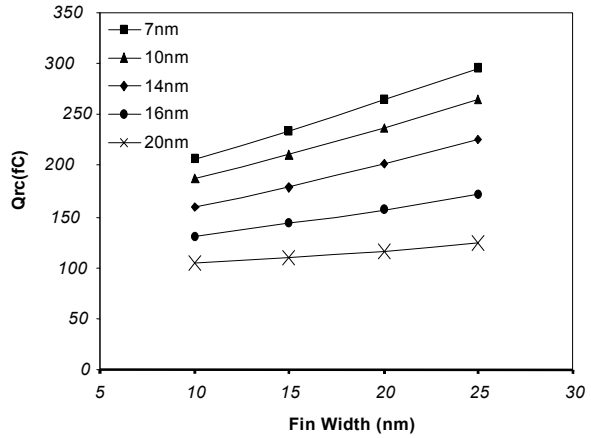

Fig. 6: The impact of fin width on the circuit robustness to SEU for different technology nodes.

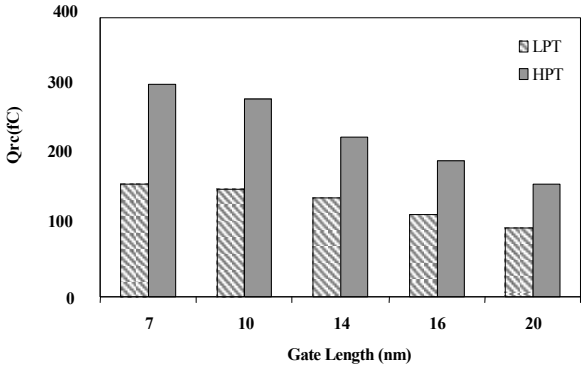

Fig. 7: The impact of technology scaling on the circuit robustness to SEU for high power and low power devices.

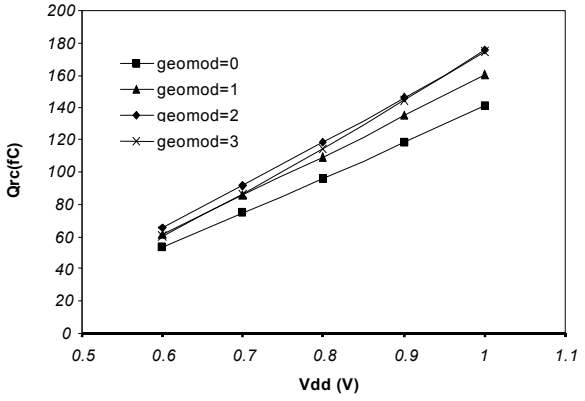

Fig. 8: The effect of power supply variation on the circuit robustness to SEU for different MuGFETs structures.

Besides the fact that device scaling can also be improved by using smaller technology nodes, it is equally worth mentioning that the variation of

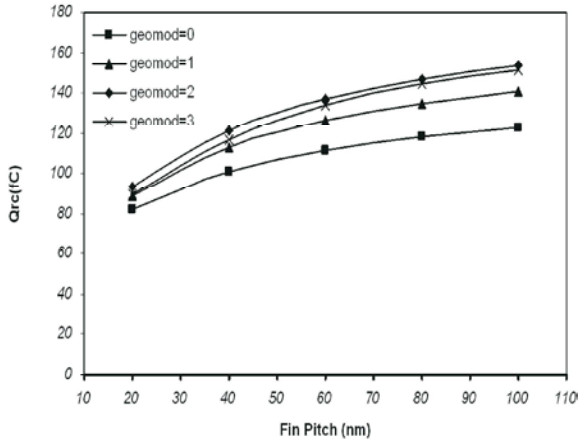

Fig. 9: The effect of fin pitch on the circuit robustness to SEU for different MuGFETs structures.

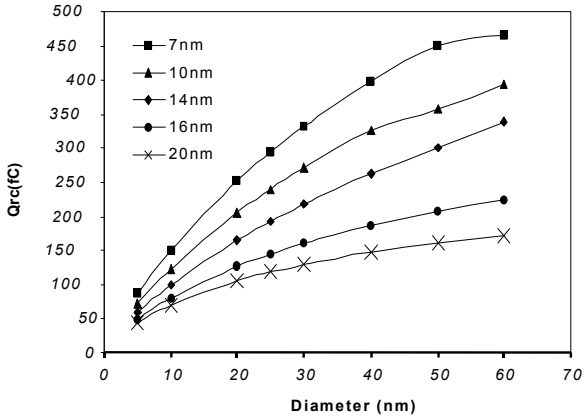

Fig. 10: The effect of the diameter of all-around gate transistors on the circuit robustness to SEU for different gate lengths.

gate length is significantly more noticeable when utilizing high power devices, with reference to their low power counterparts.

Figures 8, 9 and 10 compare the impact of parameters investigated previously, such as V_{dd} variation and fin pitch for different MuGFET devices utilizing different geometrical structures, namely (GEOMOD, Dual Gate = 0, Tri-Gate = 1, Quadruple Gate = 2, Cylindrical /all around Gate = 3).

It can be seen from Figures 8, 9 and 10 that the quadruple gate and all gate around devices offer higher Q_{crit} values with regard to the variations of V_{dd} and fin pitch, whilst these values are reduced when using a normal dual gate. This might be explained through the expected rise in current strength, due to the fact that the electrostatic control of the device gate increases, as

demonstrated for quadruple and cylindrical gate structures, where the gate electrode is wrapped around the entire channel.

Furthermore, as shown in Figure 10, the robustness to SEU of an inverter can easily be strengthened by increasing the cylinder diameter of the all-around gate transistors (Geomod = 3). This might be explained by the increase in the cylinder diameter which will effectively increase the effective device width, which in turn improves the device strength of the PMOS device, helping it to recover from a single upset event. It can also be noticed that the slope of the curves obtained increases for smaller gate lengths; consequently, it can be figured out that a higher improvement in circuit resilience to SEU can possibly be gained for devices when using larger core diameter and smaller gate length devices.

CONCLUSION

Soft error analysis using various MuGFET structures of an inverter has been carried out. The analysis involved the simulation for studying the impact of each of the key parameters of MuGFET devices, power supply voltage (V_{dd}) and on the critical charge (Q_{crit}) necessary to create a single event upset (SEU). It was found that the sensitivity of a node to a single event upset can be reduced by increasing the drive strength of the restoring devices which, in turn, increases the rate of removal of the charge collected at a node by a particle strike. This can be done by increasing the effective width of the devices and increasing the power supply voltage.

The analysis of different MuGFET technology nodes subsequently permits a relative comparison of Q_{crit} to be undertaken. The quadruple and all-around gate structures are found to be the most robust in terms of soft errors, compared to the dual and tri-gates of the inverter.

The potential of high and low power technology devices in enhancing the resilience of a circuit to soft errors has been explored. It has been observed that circuits based on HPT devices show a higher tolerance when compared to an LPT structure.

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