

A Low-Power Reversible Full-Adder Using Novel 3X3 Reversible Gate

¹R. Uma, ²P. Vigneshwarababu and ¹P. Dhavachelvan

¹Department of Computer Science, School of Engineering,
Pondicherry University, Pondicherry, India

²Department of Electronics, School of Engineering,
Pondicherry University, Pondicherry, India

Abstract: Reversible computation has become an alluring concept in low power circuit design. The conventional computations generate more heat due to the effect of logic gates which are irreversible in nature. For low power consumption circuit must be designed with reversible logic gates that have both forward and backward deterministic. The main focus of this study involves two primary design implementations. The earlier presents the design of Modified Toffoli Reversible gate (MTGDI) gate. The proposed MTGDI gate is fully reversible and designed with Gate diffusion input (GDI) logic design technique which consumes less power and less area. The last presents the realization of full adder by incorporating the proposed MTGDI gate. The performance of the proposed study have been compared with its counterpart in terms of transistor count, quantum cost, PDP and garbage output. From this study it is tacit that the proposed model produces maximum of 47.3% of PDP improvement with 7% of delay and 28.5% of quantum cost improvement.

Key words: Reversible logic gate • Quantum Computing • Bijective mapping • Logical reversibility • Gate diffusion input

INTRODUCTION

According to the Moore's law it is understood that, for every 18 months the number of the transistor fabricated in an IC doubles. Therefore heat generation due to increasing chip density also inevitably increases. Reversible logic design is extensively motivated in recent years due to its energy and information lossless design. Conventional irreversible logic gates dissipate heat for every single bit loss during their operation. In 1973 Physicist C.H Bennett [3] demonstrated that no energy dissipation occurs when the circuit is designed with reversible logic gates. If the circuit or logic gate permits to recover input data from the output data and vice versa which makes the circuit information lossless then the circuit is said to be reversible circuit or reversible logic gate. The general consideration imposed in the design of reversible logic should satisfy bijective property that is the circuit design should consist of equal number of input and output with one to one mapping. This bijective mapping averts the loss of information which is

primary reason for power dissipation in irreversible logic. The reversible gate output which is not used is called Garbage output. Extra Inputs which are used in reversible gate to accomplish reversibility is called Constant or Garbage input. Performance and Complexity of reversible gate/circuits are depends on various parameters. Such as

- Less no. of reversible logic gates are used to design reversible circuit
- Less number of constant or garbage input should be used to make the gate reversible
- Garbage output should be minimum
- Fan out is restricted in reversible logic gate. The fan out each gate is equal to one. A copying gate is used if more fan out are required.

The main aim of this study is to introduce new reversible gate using Gate Diffusion Input (GDI) technique. The primary objective of this proposed gate is to produce optimum no. of garbage output and quantum cost with respect to its counterpart. The paper is

Corresponding Author: R. Uma, Department of Computer Science, School of Engineering,
Pondicherry University, Pondicherry, India.

Table 1: Existing Reversible Logic Gates

Existing Reversible Gate	Gate Size	Input/output Definition	Functionality	Description	Quantum cost
Feynman 1985[6] Figure 1a	2x2	I(A,B)/ O(P=A,Q=A⊕B)	XOR, Buffer	When the control input A is high the output is complementary function of A, otherwise it acts as a buffer	1
Toffoli 1980[19] Figure 1b	3x3	I(A,B,C)/ O(P=A,Q=B,R=AB⊗C)	Controlled Controlled gate and buffer	When two input A and B are high then output of third terminal is negation of its input, for remaining output terminals act as buffer	5
Fredkin 1982[7] Figure 1c	3x3	I(A,B,C)/O(P=A,Q=A' B⊗AC, R=A'C'⊗AB)	Controlled Swap gate	Output of Q and R will be the swapped value of input B and C when the input A is high	5
Peres 1985[15] Figure 1e	3x3	I(A,B,C)/O(P=A,Q=A⊕B, R=A⊕BC)	Controlled NOT, Controlled Controlled NOT, Copying gate	When input A is high, output Q will be negation of B and when both A and B are high then the third output R will be the negation of its input C	4
New 2002[2] Figure 1f	3x3	I(A,B,C)/O(P=A,Q=AB⊗C, R=A'C'⊗B')	The gate acts as buffer, XOR and AND	When C input is low the output is XOR by inverting A and B else it acts as AND gate	7
TR 2011[8] Figure 1d	3x3	I(A,B,C)/O(P=A,Q=A⊕B, R=AB'⊗C)	Buffer, NAND	When the input B is inverted by using NOT gate it produces NAND output functions	6
PRT-I 2011[17] Figure 1g	3X3	I(A,B,C)/O(P=AB⊗B' C, Q=A⊕B⊗C, R=AB' ⊗BC)	XOR,XNOR,OR AND	When input A is high it acts as XNOR/OR and when input C is low it acts as XOR/AND	6
PRT-II 2011[17] Figure 1h	3X3	I(A,B,C)/O(P=BC⊗AC', Q=A'(B⊗C)+AB, R=C)	OR,XNOR	It acts as OR when input A is high and when C is 1 it acts as XNOR	5
TSG 2005[9] Figure 1i	4x4	I(A,B,C,D)/ O(P = A, Q = A' C'⊗ B', R = (A' C' ⊗ B')⊗ A, S=(A' C'⊗ B')D⊗(AB⊗ C)	AND	When input C and D applied with 0 it acts as AND gate	14
MKG 2007[12] Figure 1j	4X4	I(A,B,C,D)/ O(P = A, Q = C, R = (A'D'⊗ B')⊗ C, S = (A'D'⊗ B')C⊗(AB ⊗ D))	Buffer, XOR, XNOR and	MKG acts as XOR/AND when A and D is 0 and acts as XNOR when A is high and D is low	9
DKG 2011[10] Figure 1k	4X4	I(A,B,C,D)/ O(P = B, Q = A'C + AD', R=(A⊗ B)(C ⊗ D)⊗ CD, S = B⊗ C⊗ D)	Buffer, XOR and	It acts as XOR when A input is low	11

organized as: Section II outlines the related work in terms of input and output logic with quantum cost. Section III describes the proposed logic structure Modified Toffoli Gate with GDI. The proposed MTGDI gate has been developed to operate in the voltage range of 3V to 5V. The process technology used to define the transistor is TSMC 250 nm process. The designed structure is compared with other technologies like CMOS, TG, PT, CPL and DPL. Section IV presents the construction of proposed full adder using MTGDI and NOT gate. Section V presents the performance issues with respect to its counterpart. Discussion about proposed adder design carried out in section VI and the conclusion is presented in section VII.

Related Work: Various implementation of logic gates addressed in [2-15], the classification defined in terms of its size and functionality. The 2x2 reversible gate is

Feynman. The 3x3 reversible gates are Toffoli, Fredkin, Peres, New gate, TR gate, PRT-1 and PRT-2 and the 4x4 gate includes TSG, MKG and DKG. The design specifications and the functional descriptions are presented in Table 1.

Proposed Primitive Reversible Cells: The implementation and characteristics of the proposed MTGDI cell are explained in the following sections. The transistor level implementation using GDI along with the simulated results and quantum cost calculations are also discussed.

Proposed Primitive Reversible Primitive Cell: The proposed MTGDI gate is a 3x3 reversible logic gate where no. of input and output ports are equal to 3. Input and output vectors are defined as A, B, C and $P = A$, $Q = A \oplus B$, $R = AB \oplus C$ respectively. MTGDI can be configured as Buffer, 2-Input XNOR and 2-Input AND or 2-Input NAND

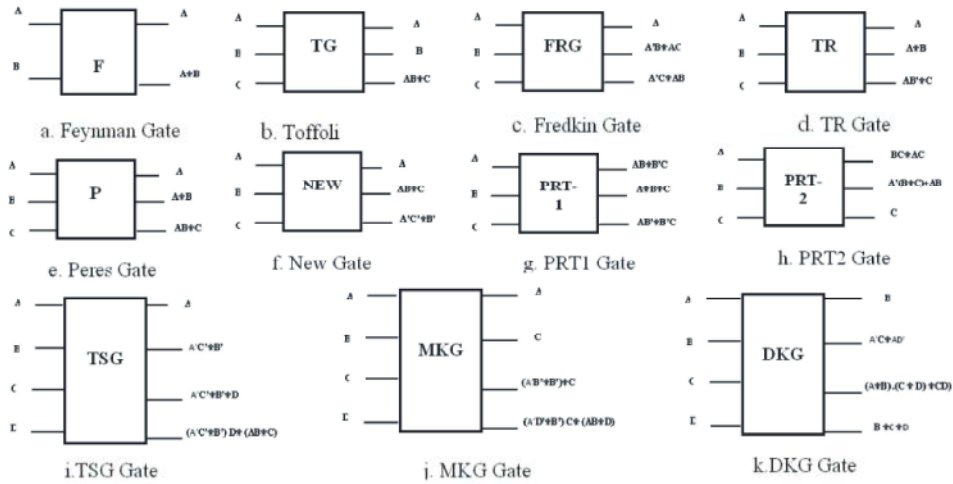


Fig. 1: Existing Reversible Logic Gates

Table 2: Logic function implemented with GDI technique

N	P	G	OUT	Function
'0'	B	A	\overline{AB}	F1
B	'1'	A	$\overline{A} + B$	F2
'1'	B	A	A+B	OR (F3)
B	'0'	A	AB	AND (F4)
B	C	A	$\overline{AC} + AB$	MUX(F5)
'0'	'1'	A	A	NOT(F6)
\overline{B}	B	A	$A \oplus B$	XOR(F7)
B	\overline{B}	A	$\overline{A \oplus B}$	XNOR(F8)

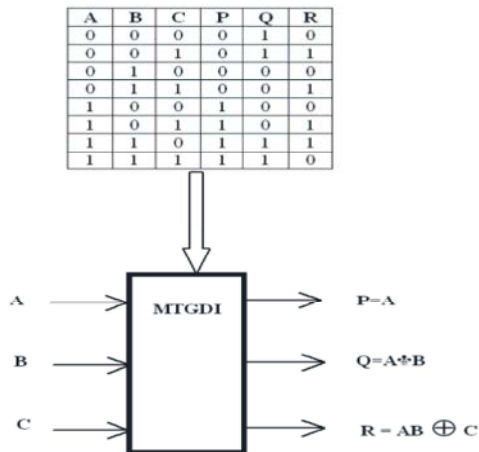


Fig. 2: Proposed Reversible MTGDI Gate

depending on C input. The computation functions based on A, B, C are depicted in the Figure 2. When 0 is forced at the input terminal A or B, the MTGDI acts as XNOR gate and XOR gate can be realized by applying 1 at the input terminal A. Depends on the input at the C it can acts

as AND or NAND gate. So by configuring the input terminals suitably we can realize various logic functions.

Transistor Level Representation of Proposed Reversible Gate in GDI Technique: Basic GDI cell shown in Figure. 4 consist of two transistors with the inputs G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), N input to the source/drain of NMOS. Even though GDI cell is comparable to CMOS style inverter, but it offers more functions then just inverting the signal. NMOS and PMOS bulks are connected to N or P respectively so it can be arbitrarily biased at contrast with a CMOS inverter. By configuring these three terminals of GDI cell various Boolean functions can be achieved which are shown in Table 2. The proposed MTGDI gate can be implemented using the functional table of GDI logic which is depicted in Table 2. The proposed MTGDI gate is implemented using F8, F7 and F4 function from the above table. Transistor level implementation of proposed gate depicted in Figure. 5, it contains 22 transistors

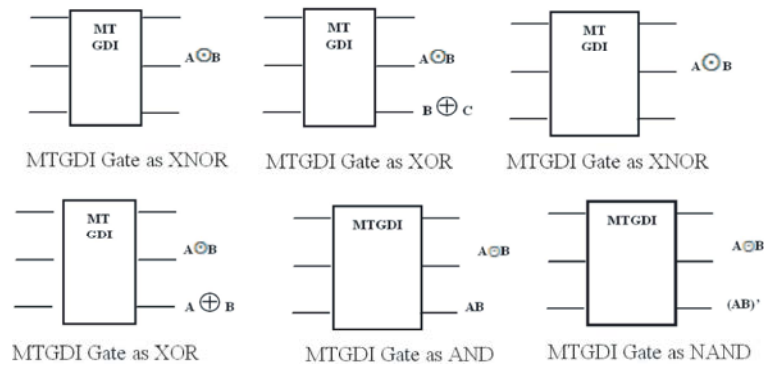


Fig. 3: Various Configuration of Reversible MTGDI Gate

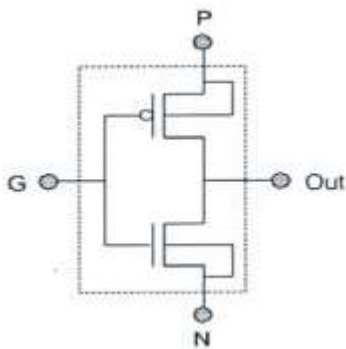


Fig. 4: GDI cell

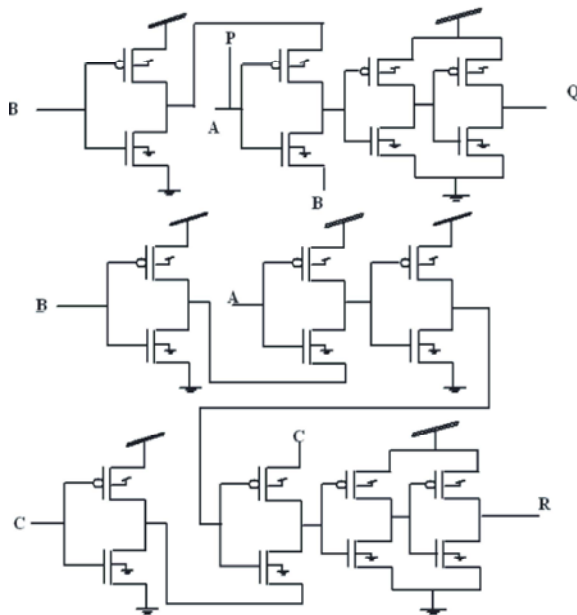


Fig. 5: Transistor level implementation of proposed MTGDI gate

Simulation Results of the Proposed MTGDI Reversible Gate: Tanner EDA tool has been used to simulate the proposed reversible gate in 250nm standard CMOS

technology with supply voltage ranges from 1.2v to 5v in steps of 0.5v. Bit patterns “01010101”, “00110011”, “00001111” are forced to input terminals A, B and C respectively to provide an impartial testing environment. To check the proper working of MTGDI gate due to variation in device characteristics and environment it has been operated with multiple design corners Typical-Typical (T-T), Fast-Fast (F-F), Fast-Slow (F-S) and Slow-Slow (S-S). Designed gate based on 2.5/025 μ m W/L ratio transistor [NMOS and PMOS] and simulated at the clock frequency of 100MHz. Obtained output parameters are tabulated in the Table 3 and 4. To perform the complete analogy, proposed gate is constructed with different logic design techniques such as CMOS, TG, PT, CPL, DPL and compared with GDI based design for the performance.

Propagation delay has been estimated for the input reaches 50% of voltage level with respect to 50% of rise in output voltage. The propagation delay is observed for A to P, A to Q, A to R, B to P, B to Q, B to R, C to P, C to Q and C to R. The average of propagation delay of the inputs A, B and C has been reported as the total delay of the circuit in Table 3.

The rise time has been calculated for the output signal to have risen from 0% to 90% of its steady state value. Similarly time taken by output waveform to fall from high value (90%) to low value (10%) of its full swing output value is calculated as fall time. The rise time and fall time for the outputs P, Q and R are reported in Table 4. The power consumption has been measured for all the bit combinations and its average power has been reported in Table 4. In comparison of different logic, the superiority of the design not only depends on power, delay and transistor count but also on PDP (Product of power and delay) and AT (Product of transistor count (area) and delay) values. The comparisons of PWR (Power), PDP and AT are presented in Table 4.

Table 3: Delay of MTGDI gate for different logic design techniques

Logic	Delay1 (ns)				Delay2 (ns)				Delay3 (ns)				TotalDelay(ns)
	A to P	A to Q	A to R	Avg	B to P	B to Q	B to R	Avg	C to P	C to Q	C to R	Avg	
GDI	0.042	19.88	44.80	21.57	30.04	10.11	14.80	18.31	45.04	25.11	0.194	23.44	21.11
CMOS	0.153	19.84	44.78	21.59	30.15	10.15	14.78	18.36	45.15	25.15	0.214	23.50	21.15
TG	0.161	30.03	44.86	25.01	30.16	0.037	14.86	15.01	45.16	14.96	0.133	20.08	20.04
PT	0.159	19.93	44.74	21.60	30.16	10.06	14.74	18.32	45.16	25.06	0.254	23.49	21.14
CPL	44.89	29.85	0.160	24.96	30.16	0.146	14.89	15.06	45.16	15.14	0.107	20.13	20.05
DPL	0.160	20.04	44.94	21.71	30.16	9.957	14.94	18.35	45.16	24.95	0.053	23.38	21.15

Remarks: **GDI**-Gate Diffusion Input, **CMOS**-Complementary Metal Oxide Semiconductor, **TG**-Transmission Gate, **PT**-Pass Transistor Logic, **CPL**-Complementary Pass Transistor Logic, **DPL**- Double Pass Transistor Logic. **Delay1**-Propagation delay from input A line to outputs (P, Q, R). **Delay2**-Propagation delay from input line B to outputs (P, Q, R). **Delay3**-Propagation delay from input line C to outputs (P, Q, R). Total Delay: Average of delay1, delay2 and delay3.

Table 4: Power dissipation of MTGDI gate for different logic design techniques

Reversible MTGDI	logic	PWR (W)A(V1)	PDP ($\mu\text{W} \times \text{ns}$ in fW _{ns})	Rise Time (ns)			Fall Time (ns)			# Tr	AT(#Trns)
				P	Q	R	P	Q	R		
	GDI	830.79 μ	17540.93	0.248	0.085	0.074	0.217	0.082	0.103	26	548.95
	CMOS	1.19m	25170.75	0.235	0.244	0.179	0.104	0.527	0.174	34	719.16
	TG	14.91m	298798	0.105	20.47	0.291	0.118	0.324	0.400	28	561.12
	PT	1.23m	26002.61	0.107	0.088	0.084	0.119	0.045	0.037	32	676.49
	CPL	4.39m	88045.36	0.102	19.86	0.123	0.119	0.181	0.080	31	621.73
	DPL	6.90m	145942.7	0.103	20.81	0.621	0.118	0.344	0.602	28	592.23

Remarks: Power reported is an average power which is measured for positive peak, **Rise Time (RT)** - Time for a waveform to rise from 10% to 90% of its steady state value, **Fall Time (FT)** - Time for a waveform to fall from 90% to 10% of its steady state value, **#TR**- Transistor Count, **AT**- Parameter which define the product of Area (A) and Delay (T)

Table 5: Performance Comparison of MTGDI Gate for Different Logic Design

	PWR					PDP					AT				
	CMOS	TG	PT	CPL	DPL	CMOS	TG	PT	CPL	DPL	CMOS	TG	PT	CPL	DPL
MTGDI	30.1	94.4	32.4	81.0	87.9	30.3	94.1	32.5	80.0	87.9	23.6	2.1	18.8	11.7	7.3

Remarks: PWR: Average power consumption PDP: Product of power and delay term. - Parameter which define the product of Area (A) and Delay (T)

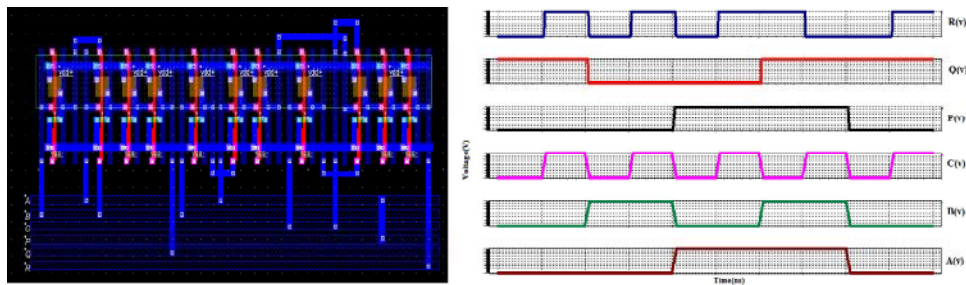


Fig. 6: Layout and post layout simulation of proposed MTGDI gate

The silicon implementation of MTGDI gate is depicted in Figure 6. The proposed structure is a GDI Inverter based structure. So the primitive construction involves the design of inverter. The basic CMOS inverter has its P-channel device in an N-type well and its N-channel device in the P-type substrate. The inverter is designed with minimum-size transistors. The layout of MTGDI contains two controlled V+, one controlled NOT and one controlled-V gates. So the total number of

transistor required to layout this circuit is 22 transistors (F4, F7 and F8 functions in GDI which is presented in Table 1).

Quantum Cost Calculation: To compute the cost of a reversible circuit, diverse metrics are applied. More specifically to obtain the cost the number of circuit lines incorporated in the reversible gate is an important criterion. The total number of basic quantum gates

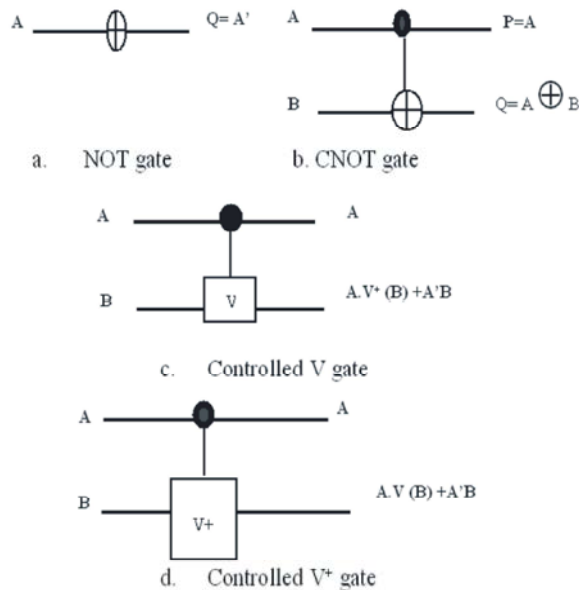


Fig. 6: Basic quantum gates

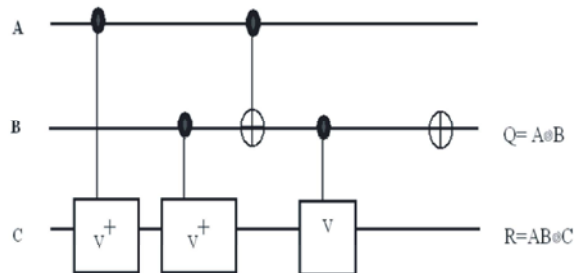


Fig. 7: Quantum cost computation of MTGDI gate

required to construct the reversible logic gates is known as quantum cost. The quantum gate library was introduced by Toffoli in 1980. All reversible functions can be realized using smallest complete set of gate library which includes NOT, CNOT, Controlled-V gate, Controlled-V⁺ gate. 1x1 and 2x2 gates are used to realize all reversible logic gates. Since all reversible gates are built from 1x1 and 2x2 quantum primitives and its quantum cost is calculated as a total sum of 2x2 gates which has quantum cost of 1 and quantum cost of 1x1 assumed to be zero.

NOT gate is one input one output gate which inverts the input bit value. The quantum cost of NOT primitive is zero. The property of CNOT library primitive is, if the value of A=1 then it inverts the value of B. CNOT gate operates as a buffer if A=0 then the value B is transfer at the output of the reversible gate. The quantum cost for CNOT gate is 1. CNOT, Controlled-V gate and Controlled-V⁺ gate have 2 terminal lines. One is control line which control/changes the value at the other output line.

Depending on the value of control line Controlled-V gate changes the value on the output line using the transformation matrix $V = \begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix}$. The V gate is also called

as square root of NOT primitive. Controlled-V⁺ gate depending on the value of control line, it changes the value on the output line using the transformation $V^+ = V^{-1}$. Some other Properties of V and V⁺ are

$$V * V = \text{NOT}$$

$$V * V^+ = V^+ * V = I$$

$$V^+ * V^+ = \text{NOT}$$

The above equations show that two V and V⁺ gates in series are equal to NOT gate. V and V⁺ gates in series are equivalent to a buffer gate or identity gate. The quantum cost of, Controlled-V gate and Controlled-V⁺ gate are 1. For the proposed MTGDI gate the quantum cost are computed based on the primitive quantum library of 1x1 and 2x2 (NOT, CNOT, Controlled-V and Controlled-V⁺). For MTGDI gate uses 1 CNOT, 2 Controlled-V⁺ and 1 Controlled-V. The total cost of gate5 is 4 (1 CNOT+ 2 Controlled-V⁺ + 1 Controlled-V).

Proposed Full Adder Cell Using Mtgdi: Adder is a fundamental component used in applications like filters, ALU, DSP core, etc. The key aspects in the design of adder cells include many factors such as area, delay and power dissipation. Different adder topologies were analyzed to design the proposed adder which is reported in [2, 9-10, 16]. The proposed adder circuit realization is shown in Figure 8. The proposed adder is implemented with MTGDI gate and NOT gate. Detailed analogy has been drawn to verify the performance of proposed and existing reversible adders. Tanner EDA software used to simulate the designed circuits at 0.250μm technology and tested with different step input voltages ranges from 1.2V to 5V. All the full adders verified for proper operation to ascertain its function across variation in device characteristics and environment, so it has been operated with multiple design corners Typical-Typical (T-T), Fast-Fast (F-F), Fast-Slow (F-S) and Slow-Slow (S-S). Designed gates based on 2.5/0.25μm W/L ratio transistor [NMOS and PMOS] and simulated at the clock frequency of 100MHz. The waveform in Figure. 9 indicates the complete transition characteristics of proposed full adder with the three inputs A, B, C having the bit patterns (000, 001, 010, 011, 100, 101, 110 and 111).

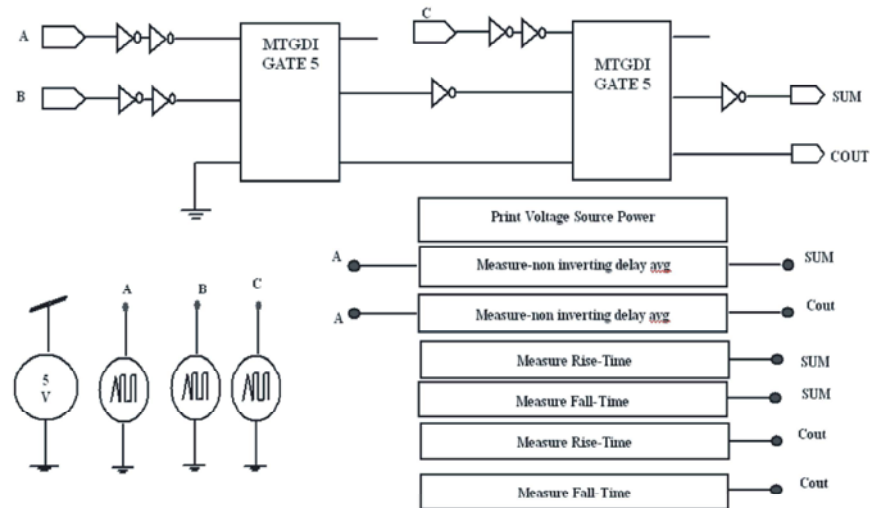


Fig. 8: Simulation setup of proposed full adder

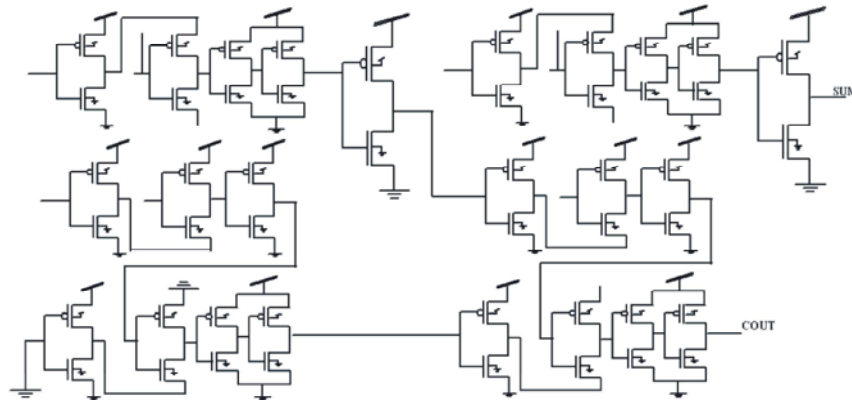


Fig. 9: Transistor level implementation of proposed full adder

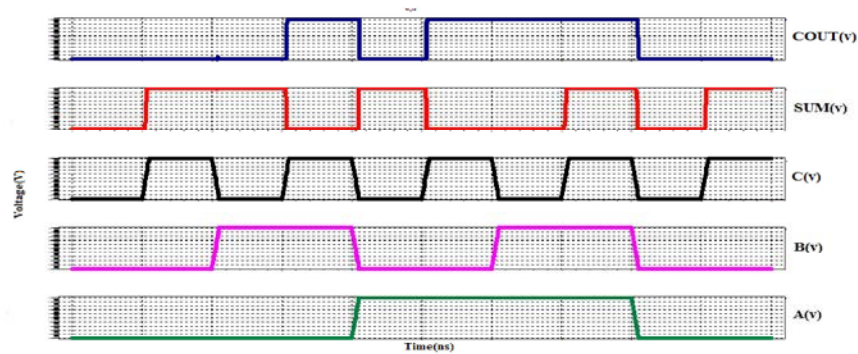


Fig. 10: Input and output waveform of proposed full adder

Performance Analysis of Proposed Full Adder Cell:

Table6 shows the output parameters of the proposed and existing full adder. A detailed analogy has drawn with circuit output parameters such as delay, power, rise time, fall time, PDP, garbage output, critical path and quantum cost. Analysis reveals that proposed adder has better performance over existing adders. Full adder using TSG

gate consumes the maximum power of 5.54mW with the highest quantum cost and PDP value of 14 and 381506.5fW-s respectively. Full adder design in [16] produces maximum delay of 69.572ns and critical path of 4 with quantum cost of 11. In adder [2] is designed with 1 New gate, 1 Toffoli gate and Feynman gate which has critical path of 3 with the high quantum cost of 11 and

Table 6: Performance analysis of proposed full adder with existing reversible full adders

Reversible Adder	Reversible Gate Used	Delay Sum(ns)	Delay Cout(ns)	Total delay(ns)	SUM		COUT		Power (μ W)	PDP μ W \times ns in fW-s	Garbage output	Critical path	Quantum cost
					RT(ns)	FT(ns)	RT(ns)	FT(ns)					
Existing[10]	DKG	39.917	24.72	64.64	0.0758	0.0759	0.0487	0.0806	1590	102782.3	2	1	11
Existing [9]	1 TSG	44.505	24.359	68.864	0.172	9.6339	0.4107	0.0958	5540	381506.5	2	1	14
Existing [16]	2 TOFFOLI + 2 FEYNMAN	44.838	24.734	69.572	0.2856	0.2606	0.1032	0.1228	865.62	60222.91	2	4	11
Existing [2]	1 NEW GATE +1 TOFFOLI + 1 FEYNMAN	44.818	24.734	69.552	0.2856	0.1513	0.0103	0.1168	836.20	58159.3	3	3	11
Proposed	2 MTGDI gate5 + 2 Not gate	39.915	24.762	64.677	0.0421	0.7119	0.7272	0.0812	836.11	54077.9	2	2	10

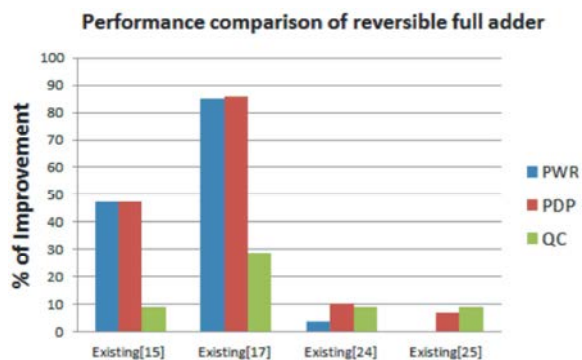


Fig. 11: Performance comparison of reversible full adder in terms of power, PDP and quantum cost

Table 7: Performance improvement of proposed full adder with existing reversible full adders

Reversible Adder	% improved in Power	% improved in PDP	% improved in QC
Existing[15]	47.41	47.38	9.09
Existing[17]	84.90	85.82	28.57
Existing [20]	3.409	10.20	9.09
Existing[12]	0.010	7.017	9.09

delay of 69.552ns. Full adder using single DKG gate has the power consumption of 1.59mW with quantum cost of 11. In overall comparison, proposed design has been proved to be better than all existing adder design.

DISCUSSION

Gate diffusion input (GDI) based reversible logic gate has been described in section 2 and full adder has been designed using proposed MTGDI gate and complete performance of the full adder tested and simulated output parameters have been reported in section 4. Percentage of performance improvement between proposed and existing full adder is tabulated in Table 7. Full adder designed with MTGDI reversible gate offers improved power consumption with the maximum of 84.90% and minimum of 3.40%, nearly 85.82% and 28.57% of improvement obtained in power delay product (PDP) and quantum cost (QC).

CONCLUSION

This study presents completely new reversible logic gates based on Gate Diffusion Input technique. The characteristics and performance has been presented in section 3 and performance has been evaluated with respect to existing logic design techniques. The proposed logic gate provides superiority in terms of PDP when compared to the existing logic families. A new full adder has been designed using proposed gate and its performance analyzed in terms of delay, power, area, PDP, garbage output and quantum cost. Two MTGDI gates and two Not gates are used to construct the full adder with the total transistor count of 48 with 2 critical path and 10 quantum cost. The designed full adder has better performance over existing designs with maximum improvement of 47.3% in PDP and 7% and 28.5% improvement in delay and quantum cost value respectively.

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