

Recovery Boosting Technic Using Efficiency Increasing in SRAM

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Abstract: High variability in nano-scaled technologies can easily disturb the stability of a carefully designed standard 6T- SRAM cell, causing access failures during a read/write operation. We propose a 7T-SRAM cell to increase the read/write stability under large variations. The proposed design uses a low overhead read/write assist circuitry to increase the noise immunity. Use of an additional transistor and a floating ground allows read disturb free operation. While the write assist circuitry provides a floating ground during a write operation that weakens cell storage by turning off the supply voltage to ground path of the cross-coupled inverter pair. This allows a high speed/low power write operation. Monte Carlo simulations indicate a 200% increase in the read stability and a boost of 124% in write stability compared to a conventional 6T-SRAM design, when subjected to random dopant fluctuations, line edge roughness and poly-granularity variations. HSPICE simulations of a 45nm 64x32 bit SRAM array designed using standard 6T and proposed 7T SRAM cells indicate a 31% improvement in write speed/write power, read power decreases by 60% and a 44% reduction in the total average power consumption is achieved with the proposed design.

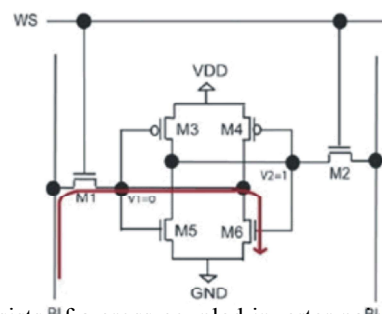
Key words: Variability • SRAM • SNM • Stability • Power • Speed

INTRODUCTION

SRAM is an important part of modern microprocessor design, taking a large portion of the total chip area and power. Increasing the density of SRAM caches provides an effective method to enhance system performance [1]. That has resulted in over 70% of the chip area being occupied by SRAM [1]. Scaling device size doubled the transistor count every two years according to Moore's law and hence the density of SRAM caches kept mounting every next generation [2]. However device dimensions become too small in nano-scale technologies and are more prone to variations due to manufacturing process [3]. These variations can disturb the read/write stability of a SRAM design causing reliability problems. A conventional 6T-SRAM has a poor read stability due to constraint design requirements and can suffer functional failures due to high threshold voltage variations. Statistical variability arising from the discreteness of charge and matter is a major source of threshold variation that degrades the reliability of conventional SRAM design [2]. Conventionally device sizing is used to enhance the read

stability of SRAM cell design. However conventional sizing can be ineffective in nano-scaled technologies due to large threshold variations [3, 4]. Different SRAM designs have previously been presented that use from 6 to 10 transistors to provide reliable and/or low power operation [5-9].

Proposed 7T-SRAM design:



It consists of a cross-coupled inverter pair (M3-M6) that does data storage and two access transistors (M1-M2) to load/retrieve data on bit lines, BL and BLB. During a write operation, the data is loaded on the bit lines and the word select signal WS is turned high. A successful write

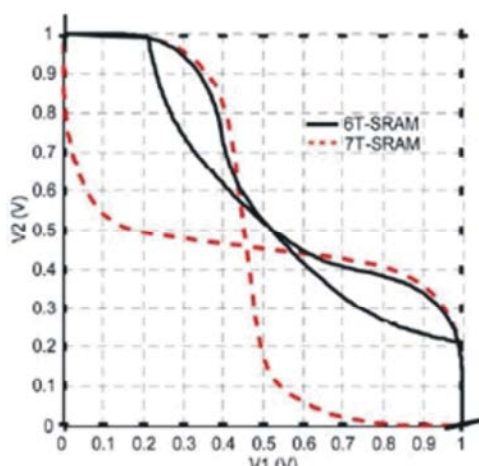


Fig. 4: Shows the read/write stability comparison using

operation occurs if the data is correctly latched in the cell [10]. The bit lines are pre-charged to the supply voltage and the word select line is turned high to retrieve data during a read operation [11]. The bit line (BL) connected to the storage node (V1) storing a '0' gets discharged. The storage node (V1) rises above '0' during a read operation due to voltage division between the access transistor (M1) and the driver transistor (M6) [12]. A read failure can occur if the voltage drop rises higher than the threshold voltage of the inverter (M3, M5).

Simulation Results and Analysis: 35nm gate-length MOS-models with no variability [10]. Conventional 6T-SRAM provides a SNM of 112 mV for a 1 V supply voltage with CR=1.5 (CR = $WM5/WM1 = WM6/WM2$). Whereas the proposed 7T-SRAM design increases the read margin to 299 mV with CR=1, indicating a 167 % improvement as shown in Fig. 4a. This indicates a high tolerance against read failures for the proposed design because the storage nodes are not disturbed during a read operation [13]. This enhancement in the SNM comes at the expense of an additional transistor. However, increasing device variability will result in further degradation of the SNM of conventional 6T-SRAM in future technologies, therefore a move to 7T or higher SRAM cell designs will be necessary to provide high stability and performance under large variations. The use of write assist transistor results in a significant increase of the WNM due to weakened cell storage and the WNM improves by 112 % (406mV vs. 861mV) at a supply voltage of 1 V.

CONCLUSION

Variability in nano-scaled technologies is a major challenge for reliable SRAM design. A conventional 6T-SRAM cell can't achieve high read/write stability due to constrained design. A 7T-SRAM cell is proposed that uses separate read/write assist circuitry to provide high stability under large variations. Monte Carlo simulations indicate a 200% increase in the SNM and a 124% boost in the WNM for the proposed design [14-17]. This increase comes at the cost of an additional transistor that has a 16% area overhead. However the use of 7T or higher SRAM designs may be necessary in future generations due to poor stability of conventional 6T-SRAM design. A comparative analysis of a 45nm 64x32 bit SRAM array designed using conventional 6T and proposed 7T SRAM cells indicates a 31% increase in write speed and a 31% decrease in write power for the proposed design. Use of a single ended read operation results in a 60% decrease in read power, while a 44% reduction in total average power is observed for the proposed design.

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