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Test Data Compression Architecture for Lowpower VLSI Testing

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Abstract: With the ever increasing integration capability of semiconductor technology, today's large integrated circuits requires an increasing amount of data for testing which increases test time and elevated requirements of tester memory. Larger test data sizes not only demand high memory requirements, but also a huge increase in the testing time. These remain the bottleneck for testing the whole system. The above disputes are addressed by the method called test data compression, which is reducing the test data volume without affecting the whole performance of the system. ISCAS'89 benchmark circuits are used to compress the test sets and the test vectors are generated by MINTEST vector generation. The main highlight of the paper is to reduce the test data volume and the test data memory by using coding schemes such as variable length coding, fixed length coding and so on.

Key words: MINTEST vector · ISCAS'89 · Tester memory · Compress

INTRODUCTION

According to Moore's law, the number of transistors integrated per square inch on a die has doubled every year and a half since the integrated circuit(IC) was invented. As per the usage of digital IC's are increasing in everyday life, the emphasis on placing larger and more complex design in smaller areas using advanced process technologies is becoming more prominent. Also for every few years the size of the transistors employed is shrunken and the frequency of circuits increased. If the trend continues, several new challenges become relevant in the testing of very large scale integrated circuits (VLSI) circuits [1]. To suggest whether a system is good or bad in VLSI circuit design testing is needed. The everlasting improvements in semiconductor fabrication technology have led to ICs with billions of transistors. Such large ICs can contain all necessary electronic circuitry for a complete system and are referred to as SOCs. Such system chips typically are very large Integrated Circuits (ICs), consisting of millions of transistors, containing a variety of hardware modules. These modules called cores are reusable, predesigned silicon circuit blocks. Embedded cores incorporated into system chips cover a very wide range of functions like processor, mpeg coding/decoding, memory etc.Fabrication process of IC is a very long way from the flaws and imperfections such as shorts due to power or ground, additional materials etc.. and also gives rise to a action of failures and defects. So each and every IC manufactured should be entering in to a testing phase. The intention of testing is to make sure that the fabricated IC is free from manufacturing defects. As because of the complexity in test process a design approach called DFT is analyzed which aims at making the testing phase simpler and faster [2]. It is very mandatory in the minimization of test time and power. In this paper, a lossless data compression scheme is presented, which reduces the amount of test data that is to be stored on the tester and then transferred to the chip. In this, a smaller amount of compressed data is transferred from the tester to the core in each test vector, instead of transferring the entire data.

Lesser Time Will Be Taken to Transfer the Entire Data: For achieving Test vector compression, many different coding schemes are presented such as variable length

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coding and fixed length coding. Examples of Variable length coding are Golomb Coding, Huffman Coding, Arithmetic coding and so on [3].

Related Work: Several Complications are quite arising under test data compression until now. Many test data compression techniques based on variable length coding schemes are going to be discussed so further. Some of them are statistical coding, run length coding, Golomb coding, selective Huffman coding, Tunstallcoding, LZWcoding, heterogeneous compression technique, FDR coding, run length Huffman coding, multilevel Huffman coding, Bitmask and Dictionary Selection Methods and variable to variable Huffman coding [4].

Run Length Coding: Some important quality factors should be considered for any kind of compression technique like the amount of compression, area overhead, reduction in test time, scalability of compression and so on [5]. The data compression code for compressing scan vectors were encoded by runs of repeated values. New method of coding based on the frequency of runs of 0s with run length less than 20 is high and also within the range of 0 to 20, the frequency of runs of length 1 decreases with increasing length. And also the shorter run lengths are mapped to shorter code words. The FDR code is similar to Golomb code but the difference in the variable group size. There are different type of codes which comes under the run length codes such as simple run length code, Golomb code, frequency directed run length codes, Extended FDR, Shifted alternating FDR code and so on. The following example shows coding for run length encoding of binary streams:

Original Test Data: 00 11111 0000
Run Length: 2 5 4

To get the maximum compression, the don't care bits are also used to filled to get the longer runs. The run based reordering and other techniques are used to enhance the run length and further increases compression, overall test time and power [6].

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Rectangular Encoding: Several techniques were proposed to improve the encoding efficiency of the basic scheme. A number of BIST schemes exploit the characteristic of test data including weighted pattern testing. The first step in rectangular encoding is to partition the test cubes in to clusters such that the pattern wise correlation within a cluster is maximized. Clustering algorithm is used here. Scan slices for a test cube are partitioned in to a sequence of variable -length rectangles. All the test cubes within each test cube cluster are partitioned identically. Within each rectangle, the largest set of scan chains that has compatible values is identified.

The above figures which clearly demonstrates how rectangular encoding is done between the test cubes. While employing this method, test compression would be significantly improved if scan chain reordering was employed with the technique to improve correlation.

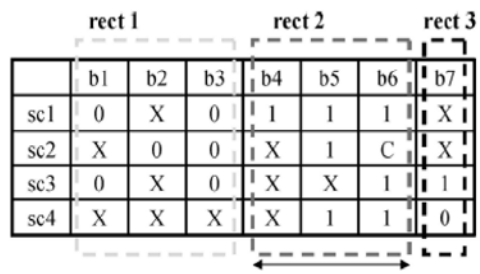


Fig. 1: Example of Test Cubes

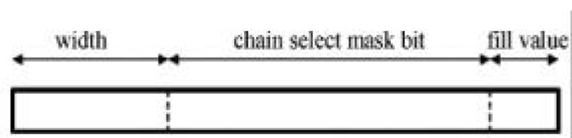


Fig. 2: Example of Rectangles

T1	B1	B2	B3	B4	B5	B6	B7
Sc1	0	X	X	1	1	1	X
Sc2	X	0	0	X	1	1	X
Sc3	0	X	X	X	X	1	1
Sc4	X	X	X	X	1	1	0

Fig. 3: Format of Rectangles

Compression Method: In this paper, Test Compression is achieved using the variable length codes [8]. Example of variable length Huffman Coding is considered for achieving compression.

Regarding compression and decompression scheme, Huffman codes are used for generating any set of deterministic scan vectors. For testing the cores with internal scan, Huffman coding is used [9]. A Huffman code is an optimal statistical code which is used to

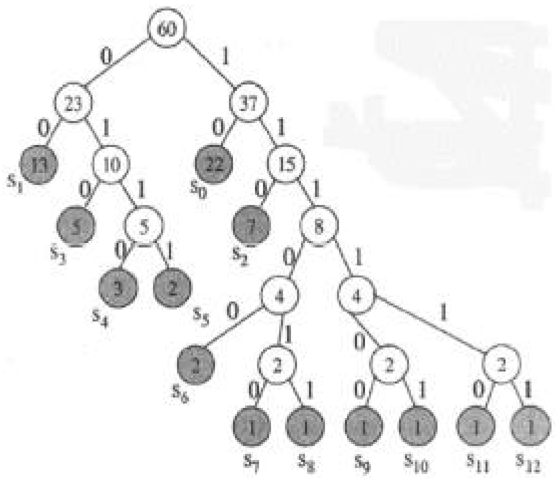


Fig. 4: Huffman Tree Construction

provide the shortest average code word length among all uniquely decodable variable length codes. Huffman tree is constructed using Huffman coding [10]. The path from the root to each leaf gives the code word for the binary string corresponding to the leaf.

The amount of compression that can be achieved with statistical coding depends on how skewed the frequency of occurrence is for the different code words [11]. The don't care bits provide flexibility to allow a block to be encoded with more than one possible code word. Using a Huffman code would provide the maximum compression, but it requires a complex decoder and may not satisfy the constraint on the minimum size of a codeword.

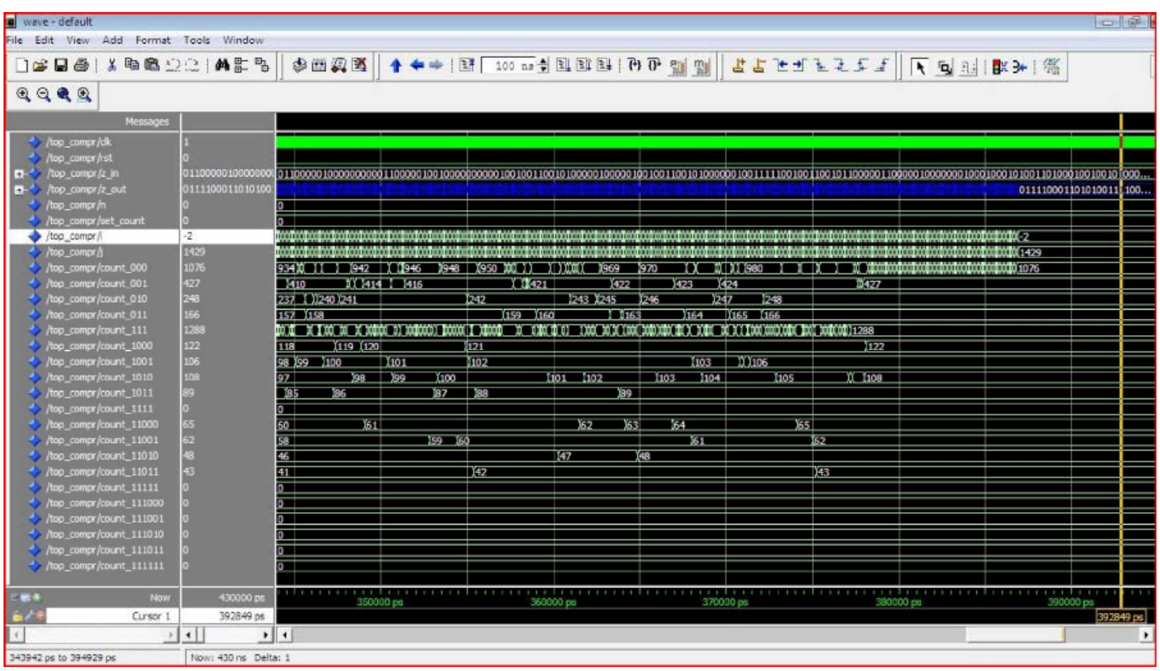
The proposed compression and decompression scheme is achieved using Huffman code.

RESULTS

The experimental results for the various ISCAS89 benchmark circuits test vectors are compressed and presented in the following table. We have used the Mintest test datas.We achieved the highest compression percentage for the different benchmark circuits.Results are implemented using the HDL Languages either in MODELSIM or XILINX. The comparison is also given in the table below.

Table 1: Comparision of different Compression Schemes using MINTEST Test data

	Existing methods				Proposed Work
Cicuits	Golomb	Rice algorithm	Tunstall	FDR	Selective Huffman
s9234	45	54	59	61	67.1
s13207	80	30	34	58	60.3
s38417	28	45	68	55	62,.5



CONCLUSION

Huffman coding is a great way to compress test data. The Coding scheme will definitely reduces the test time and memory. In this paper, we have discussed of how we have applied our algorithm on different benchmark circuits and have made comparison of our reults with existing test compression techniques. By applying our technique, we have achieved a significantly higher compression ratio [1-15].

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