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Comment on "Design of a Novel Reversible Multiplier Circuit Using HNG Gate in Nanotechnology"

Rigui Zhou, Yang Shi, Jian Cao and Hui'an Wang

College of Information Engineering,
East China Jiao Tong University, Nanchang, Jiangxi, 330013, China

Abstract: This paper is an exploratory research of errors in "*Design of a Novel Reversible Multiplier Circuit Using HNG Gate in Nanotechnology*" which was published in the Volume 3, Issue 6 of World Applied Sciences Journal in the year of 2008. There are a few flaws in some figures of that paper and affected by these wrong figures, some conclusions of that paper may be wrong. The authors give our own views on these errors and strongly suggest that they should be discussed through peer review.

Key words: Exploratory Research · World Applied Sciences Journal · Flaws · Peer Review

INTRODUCTION

In the article "*Design of a Novel Reversible Multiplier Circuit Using HNG Gate in Nanotechnology*" [1], M. Haghparast *et al*. designed a reversible multiplier circuit using HNG gate which was shown in Figure 12 *on the page of 977 in the Volume 3, Issue 6 of World Applied Science Journal in the year of 2008.* The reversible 4x4 multiplier circuit is made up of two parts. First, the partial products are generated in parallel using Peres gates as shown in Fig. 11 which quoted the *Reference 19* of that paper *(Reference 19* [2] *appears on the page of 806-810 in the Volume 3, Issue 5 of World Applied Science Journal in the year of 2008)*. Then, the addition is performed as shown in the Fig. 12 of [1]. But we think there is something wrong with these two figures and a series of conclusions in the remaining parts of that paper can be wrong because of those errors.

We firstly analyze the Fig. 11 in [1]. To facilitate the presentation, we copy the Figure 11 of [1] in Fig. 1.

It is well known that FANIN and FANOUT are not allowed in a reversible circuit. The operation FANIN allows wires to be joined together, whereby single wire contains the bitwise OR of the inputs. It is quite clear that this operation is irreversible. In addition, the FANOUT operation is also impossible in quantum circuits because it had turned out that quantum mechanics forbad the copying of a qubit [3]. But in Fig. 1, that is, the Figure 11 of [1], it is apparent that FANIN has been used so many times, so we strongly believe that the Figure 11 in [1] and also in *Reference 19* [2] of [1] are wrong, Here we rebuild the reversible partial products generation circuit using Peres gates which is shown in Fig. 2.?

Actually, the components in the dotted-line are just the "copying circuit" using Feynman gate (FG). FG is a quantum gate with two input bits and two output bits. It is drawn as shown in Fig. 3.

What is worth mentioning, if B is set to 0, then the FG changes into a "copying circuit", where input signal of one gate is grown to multi-outputs and those outputs can be used for inputs of other gates, as illustrated in Fig. 4.

So if it is necessary to FANIN in a reversible circuit, just like from x_0 to x_3 in the Figure 11 in [1], we have no option but to use "copying circuit", but in the meantime it will increase the number of reversible logic circuit.

In addition, we strongly suggest that the circuit of reversible multiplier circuit using HNG gate which was shown in Figure 12 in [1] cannot get the correct results as M.Haghparast et al mentioned. The operation of the 4×4 multiplier is depicted in Fig.5, it is observed that the results consist of 16 partial product bits of the form $x_i y_i$ (i=0….4).

Corresponding Author: Yang Shi, College of Information Engineering,
East China Jiao Tong University, Nanchang, Jiangxi, 330013, China.
Tel: +86-791-13970803095, E-mail: shy2400@gmail.com.

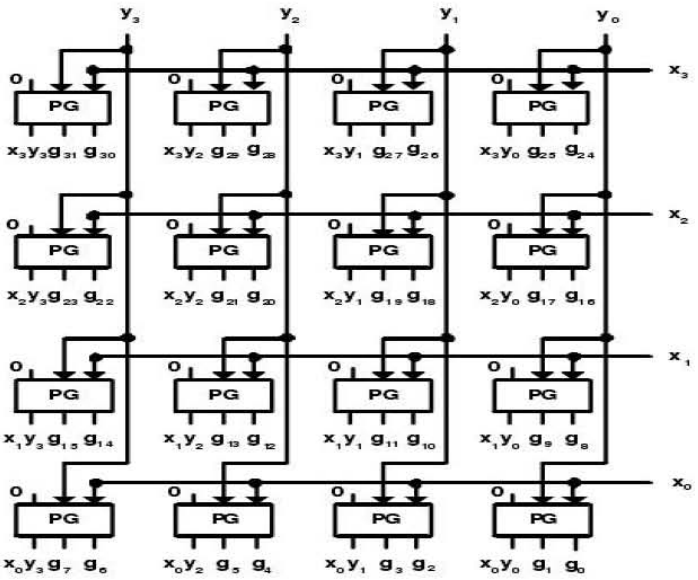

Fig. 1: Reversible partial products generation circuit in [1]

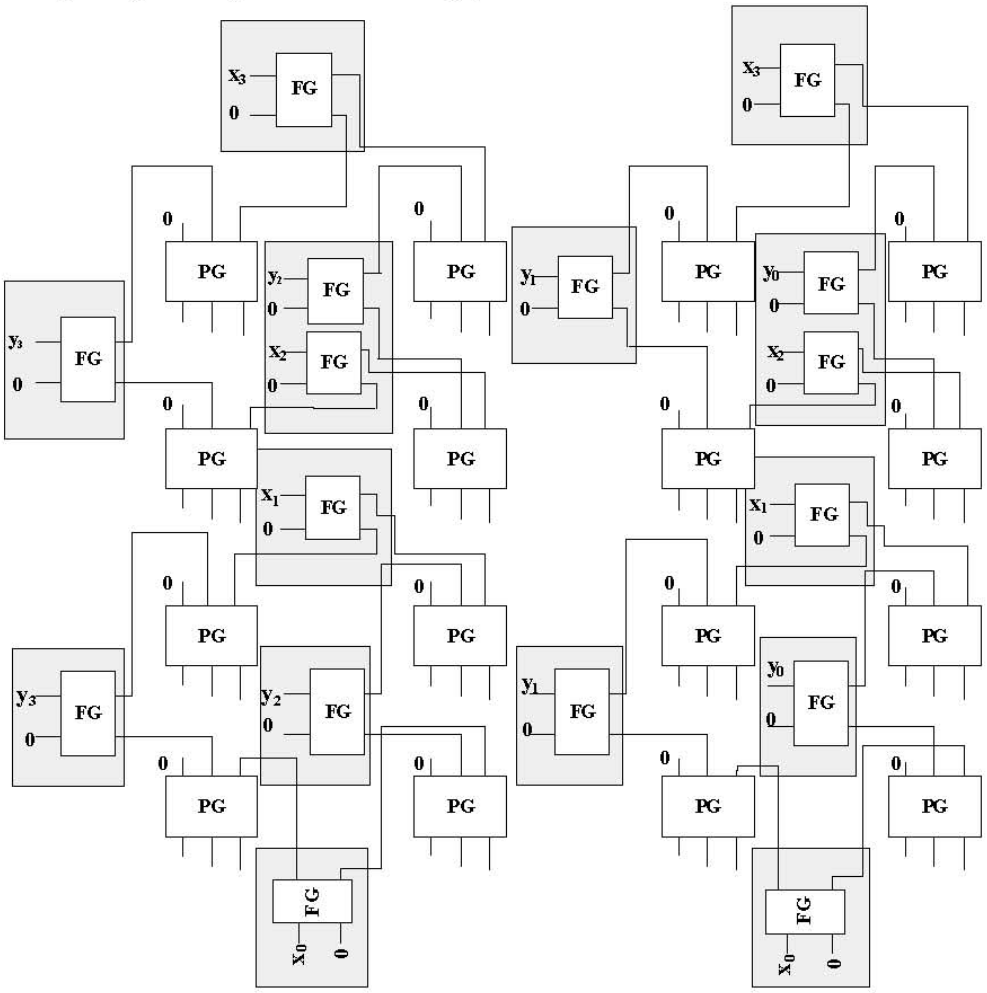

Fig. 2: Proposed Reversible partial products generation circuit using Peres gates and FG

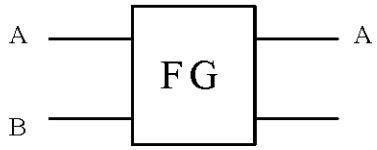

Fig. 3: Feynman Gate

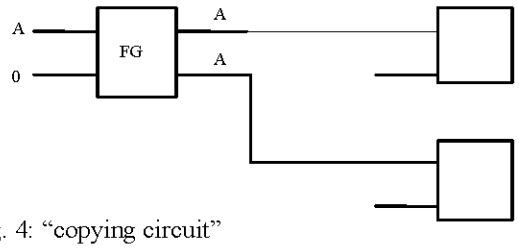

Fig. 4: "copying circuit"

$$
\begin{array}{cccccccc}
 & & & x_3 & x_2 & x_1 & x_0 & \\
 & & X & y_3 & y_2 & y_1 & y_0 & \\
\hline
 & & & x_3y_0 & x_2y_0 & x_1y_0 & x_0y_0 & \\
 & & x_3y_1 & x_2y_1 & x_1y_1 & x_0y_1 & & \\
 & x_3y_2 & x_2y_2 & x_1y_2 & x_0y_2 & & & \\
+ & x_3y_3 & x_2y_3 & x_1y_3 & x_0y_3 & & & \\
\hline
P_7 & P_6 & P_5 & P_4 & P_3 & P_2 & P_1 & P_0
\end{array}
$$

Fig. 5: Partial products in a 4×4 multiplication

From the Fig. 5, for computing the results, some equations can be obtained as followed:

$$
\begin{aligned}
P_0 &= x_0y_0 \\
P_1 &= x_1y_0 + x_0y_1 \\
P_2 &= x_2y_0 + x_1y_1 + x_0y_2 \\
P_3 &= x_0y_3 + x_1y_2 + x_2y_1 + x_3y_0 \\
P_4 &= x_1y_3 + x_2y_2 + x_3y_3 \\
P_5 &= x_2y_3 + x_3y_2 \\
P_6 &= x_3y_3
\end{aligned}
$$

P_7 is the carry bit comes from the most significant bit

Let notation"⊕" be the Exclusive-OR operation, then we can computed the results by the following relation:

$$
\begin{aligned}
P_0 &= x_0y_0 && (1) \\
P_1 &= x_1y_0 \oplus x_0y_1 && (2) \\
P_2 &= x_2y_0 \oplus x_1y_1 \oplus x_0y_2 && (3) \\
P_3 &= x_0y_3 \oplus x_1y_2 \oplus x_2y_1 \oplus x_3y_0 && (4) \\
P_4 &= x_1y_3 \oplus x_2y_2 \oplus x_3y_3 && (5) \\
P_5 &= x_2y_3 \oplus x_3y_2 && (6) \\
P_6 &= x_3y_3 && (7)
\end{aligned}
$$

P_7 is the carry bit comes from the most significant bit According to the output expressions in (1) to (7), it is easy to see that the products of multiplication could be calculated by additive accumulation respectively by using the x_i y_i (i=0….4), just as described by M. Haghparast *et al.* in the Fig. 12 of [1] and we redraw this figure in Fig. 6.

But this design approach does not pay enough consideration to the carry bits between different Full Adders which derives from the HNG and PG. For example, according to the result expression of P_2, we must divide the P_2 into two parts: the first part is the sum of x_2 y_0 x_0 y_2 and the low position to carry; the second part is the sum of the result of the first part the carry bit from the f irst part and x_1 y_1. However, in the circuit of getting the P_2 in Fig. 6, the second part is just composed of the result of the first part and x_1 y_1. So are other result expressions. Here we rebuild the 4×4 reversible multiplier circuit audaciously according to our current understanding to reversible logic design, which is shown in Fig. 7.

Just because of the effect of these errors, Table 2 of that paper also has defects. So we update this table according to the correct circuit of 4x4 reversible multiplier circuit, as shown in Table 1:

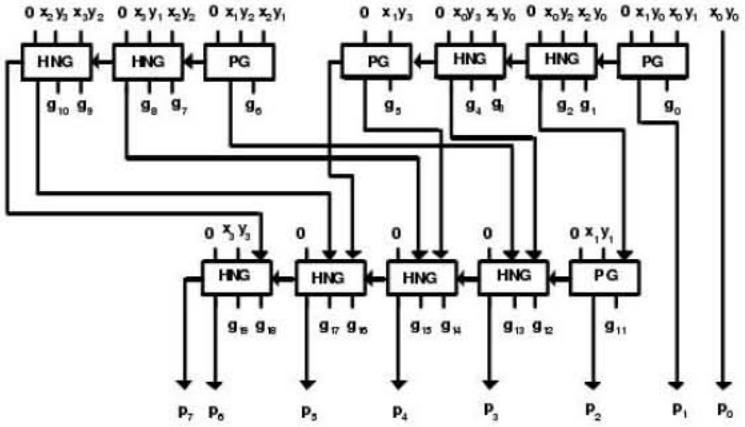

Fig. 6: 4x4 reversible multiplier circuit in [1]

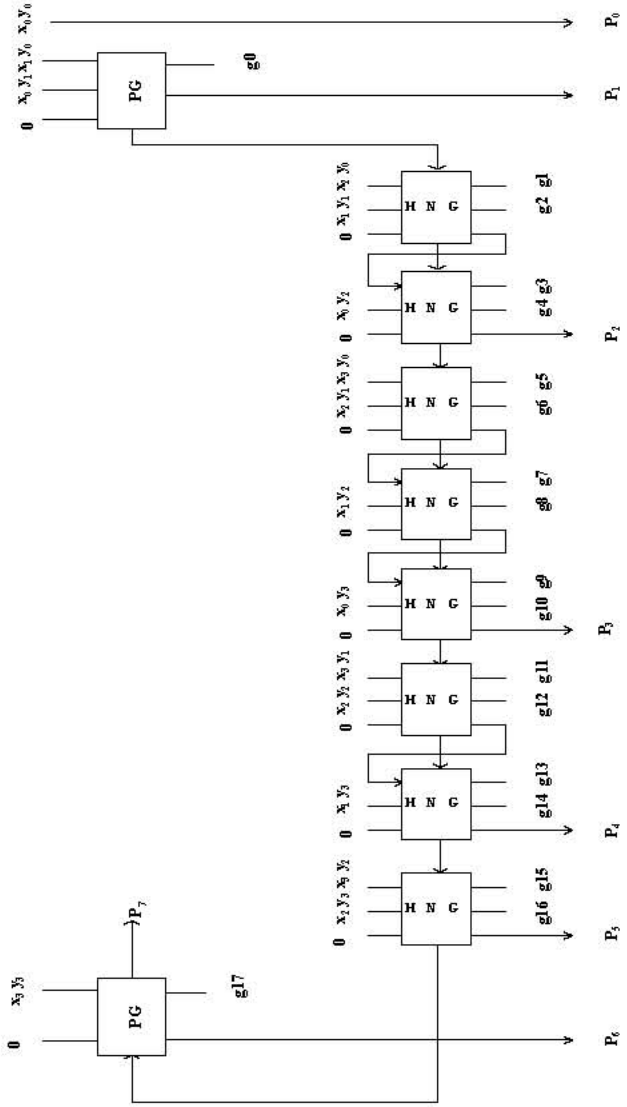

Fig.7: The proposed 4×4 reversible multiplier circuit

Table 1: Comparative experimental results of different reversible multiplier circuits

	Circuit in [1]	Circuit in [4]	Circuit in [5]	Circuit in [2]
No. of gates	(44)[a]	40	29	28
No. of garbage outputs	(49)[b]	56	58	56
No. of constant inputs	28	31	34	32
Total logical calculation	(92a+34b)[c]	80a+100b+68d	(110a+103b+55d)[d]	92a+52b+36d

[a] In the original table, the number of gates is 28. However, if in consideration of the "copying circuit" in Fig. 2, we strongly think that the number of gates of the circuit in [1] is 44 because there are extra 16 FG gates.

[b] In the original table, the number of garbage outputs is 52. But if using the correct 4×4 reversible multiplier circuit in Fig. 7 whose garbage outputs is 17, the number of garbage outputs should be 49.

[c] In the original table, the total logical calculation of circuit in [1] is 80a+36b. According to the rules in [1]:

a = A two input EX-OR gate calculation,
b = A two input AND gate calculation
d = A NOT calculation
T = Total logical calculation

It can be known that the total logical calculation of PG is (2a+b), the total logical calculation of HNG is (5a+2b) and the total logical calculation of FG is (a). There are 18 PG gates, 16 FG gates and 8 HNG gates in total in the correct 4×4 reversible multiplier circuit in Fig. 2 and Fig. 7. So:

Total logical calculation

$$= 18\times(2a+b)+8\times(5a+2b)+16\times a$$
$$= 92a+34b$$

[d] in the original table, the total logical calculation is the total logical calculation of circuit in [5] is (110a+103b+71d). But according to our observations, the total logical calculation of circuit in [5] should be 110a+103b+55d in strict accordance with the rules all above.

Finally, It is worth mentioning that *Reference 13* [6] and *Reference 15* [7] of [1] are all about the same reversible full adder called HNG gate, but in section 2: MATERIALS AND METHODS of [1], M. Haghparast *et al* put forward various results in calculating the total logical calculation of HNG, It is (5a+3b+3d) and (5a+2b), respectively. The authors are afraid that there has been a mistake about these two results and insist that the latter is right according to our current understanding.

Thus, for the above problems, the authors strongly suggest that these parts of [1] should be discussed through peer review.

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