World Applied Sciences Journal 10(12): 1463-1469, 2010
ISSN 1818-4952


# A New Full Swing Full Adder Based on New Logic Approach

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**Abstract:** As full adders are duplicated many times in arithmetic circuits, power consumption of them plays important role in total power consumption of the system. This paper presents a new low power full adder based on a new logic approach. The main aim is implementing full adder with only one XOR module to reduce power consumption. Simulation has been conducted by using HSPICE in 0.18$\mu$m bulk technology with 1.8V supply voltage. The results show that the proposed circuit has less power and higher delay than recently proposed full adders in the literature. However, PDP has been improved.

Index Terms-Full adder · Low power · Very Large Scale Integrated Circuit

## INTRODUCTION

With the continuously increasing chips' complexity and number of transistors in a chip, circuits' power consumption is growing as well. Technology trends show that circuit delay is scale down by 30%, performance and transistor density are doubled approximately every two years and the transistor's threshold voltage is reduce by almost 15% every generation. All of these technology trends lead to higher and higher power consumption in circuits. Higher power consumption, raises chips' temperature and directly affect battery life in portable devices as it causes more current to be withdrawn from the power supply. A higher temperature directly affects circuit operation and reliability and requires more complicated cooling and packaging techniques. In addition, higher current density shortens battery packs, which is not demanded by users [1].

Full adder is the fundamental unit in circuits used for performing arithmetic operations such as multipliers, compressors, large adders, comparators and parity checkers [2]. In other words, reducing power consumption in full adders, will reduce the overall power consumption of the whole system.

There are several issues related to the full adders. Some of them are power consumption, performance, area, noise immunity, regularity and good driving ability [3]. Several works have been done in order to decrease transistor count and consequently decrease power consumption and area [2, 3, 5, 6, 7, 13]. In some designs, reducing transistor count has been resulted in threshold loss problem that cause non-full swing outputs, low speed and low noise immunity especially when they are used in cascaded fashion[5, 17]. However

The aim of this study is to design 1-bit low power full adder cell, based on new logic approaches without losing driving capability.

This paper is organized as follows: Section II is the literature review for five full adders. Section III presents a logic approach and new full adder. Simulation environment and setup will be presented in Section IV. The proposed circuits will be simulated and compared to six existed full adders in Section V. Finally, the paper concludes in Section VI with the summary of the study.

**Previous Works Review:** There is variety of full adders in the literature. There are 41 full adders only in [2]. Most of them use XOR-XNOR as intermediate signal [2,3,5,9,10,13, 16,18]. There are full adders based on only multiplexers [13] or inverters [6]. In term of transistor count, it varies from 6 in [7] up to 32 in TFA [6][8]. There are also full adders in dynamic style [11] and current mode [21]. Including all full adders in this study is not possible. In continue six well-known full adders with various numbers of transistors will be selected in order to study and compare with the proposed full adder cell.

Conventional CMOS [6][12] full adder in Fig.1 (a) with 28 transistors is a robust, high power and area full adder, which has been designed, based on standard CMOS topology. It has full-swing outputs that increase noise margin and reliability. Due to high number of transistors, its power consumption is high. Large PMOS transistor in pull up network results in high input capacitances, which cause to high delay and high dynamic power. However, Using inverters on the output nodes decreases the rise time and fall time and increases the driving ability in high output loads. It can function well with low power supply voltage because it does not have threshold loss problem.

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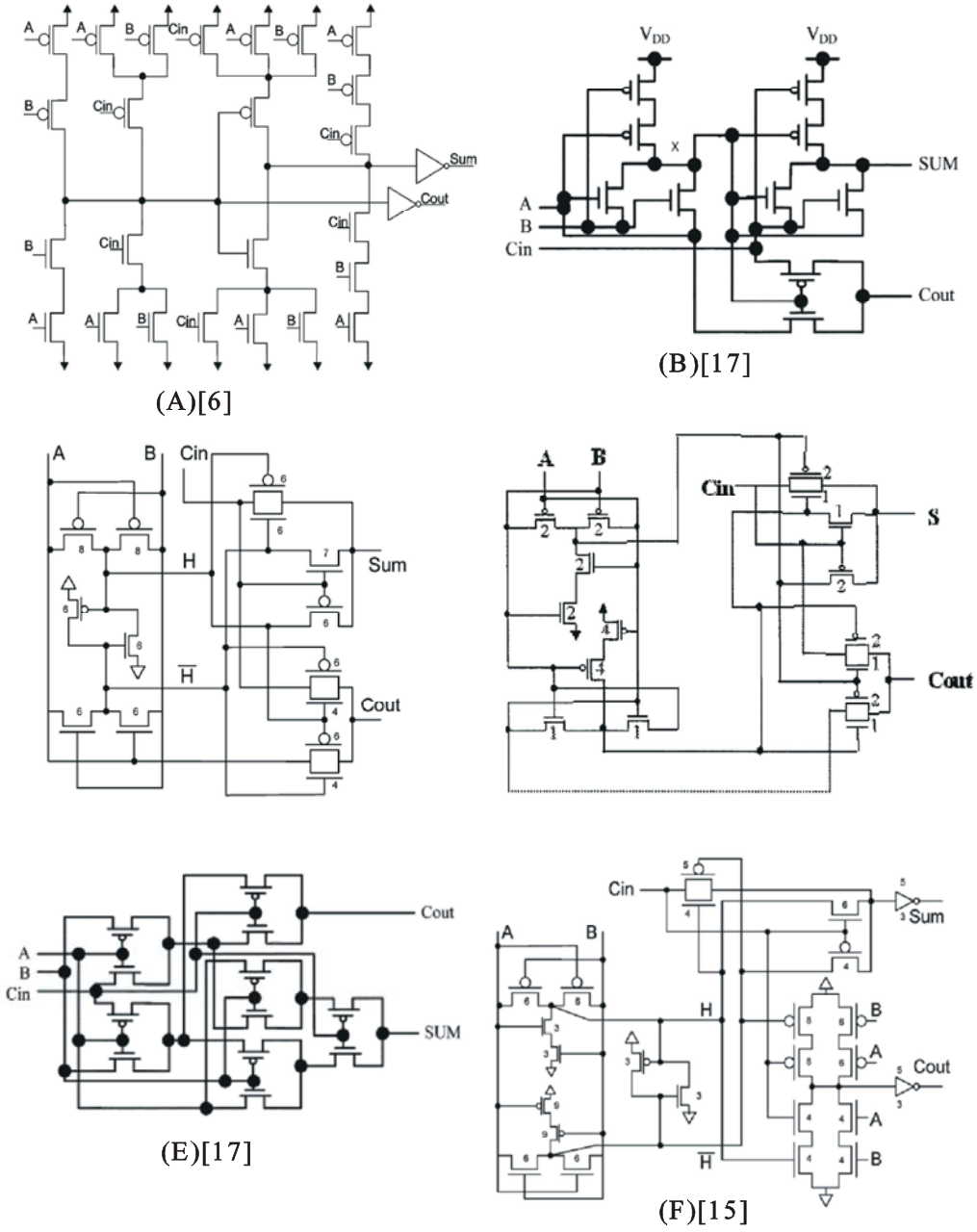


Fig. 1: Several fulladder in order to comparison. (a) CCMOS [12]. (b) Energy recovery full adder (SERF) [5]. (c) New version of 14T (New14T) [14]. (d) 16T [13]. (e) Multiplexer based full adder (MB12T) [17]. (f)New version of hybrid pass logic with static output drive full adder (16T) [15].

SERF full adder, as shown in Fig. 1 (b), uses energy recovery technique to decrease the power consumption. Energy recovery logics reuse stored charges. Ten transistors are used to implement this circuit. Thus, it is low cost and low area cell. Outputs are not full swing. Thus, it cannot work correctly with low voltages and it has high delay when the cells are cascaded to make large full adders. In the worst case, when $A=B=$'1' there is $2V_{tn}$ threshold loss in output voltage. Therefore, the value of logic 1 approaches to equal $VDD-2V_{tn}$. The suitable operating supply voltage is limited to $VDD>2V_{tn}+|V_{tp}|$. There are five gate capacitances on node X. It causes long delay in generating of the intermediate signal and finally the delay in generating SUM and COUT. Threshold loss problem also increases the power consumption as mentioned earlier.

New-14T full adder is based on 14T full adder [13] with a little modificaiotn (Fig.1 (c)). The problem with 14T is using inverter to generate XNOR signal from XOR which, results in high delay and un simultaneous XOR-XNOR output transistion. In the new-14T the inverter has been omitted to overcome the above problem. therefore, XOR and XNOR signals are generated simultaneously. There are improvments in terms of power and delay compare to 14T, however feedback transistors still cuase high delay and power consumption during transistions. The XOR and XNOR signals are named *H* and in Fig.1 (c). Non-simaltinous H and Hb will cuase glitches and unnecessary power dissipation. Outputs are full-swing, thus there is no critical limitation for supply voltage. Outputs are driven by pass gates. Therefore, it lack of driving in high loads.

Fig. 1 (d) shows another improvemed version of 14T which is called 16T[13]. It is the same as new-14T in output modules. XOR-XNOR module has been modified to reduce delay and power consumption. lower power and delay has been obtained at the expense of 2 additional transistors. XOR-XNOR modules does not have full-swing outputs thus the transistors which have been connected to this module will be turned on or off slowly.

MBA12T [17] uses 12 transistors. This full adder cell has been implemented using six multiplexers. Each multiplexer is implemented in pass-transistor logic with two transistors. As shown in Fig. 1 (e) there is no VDD or GND in this circuit. Therefore, short circuit power can be decreased significantly. However, pass gates lack of driving in cascaded mode and high fan-out that leads to high delay. As mentioned above this circuit also is not suitable for long chains and high loads due to non-full-swing outputs. As mentioned above this circuit also is not suitable for long chains and high loads.

26T full adder [15] in Fig. 1 (f), has used the output module of CCMOS for generating cout signal and also modified version of sum generator circuit of 16T with additional inverter in order to increase driving ability and speed. The XOR-XNOR module is the same modoule as 16T, with two additional feedback transistors in order to make outputs full swing. It is a high speed and low power XOR-XNOR module with full swing outputs. This design trades power and performance with area. All the intermediate signals are rail to rail and the outputs have good driving capability. Therefore, it shows high speed in cascaded fashion and large loads. Using both VDD and GND for generating cout causes to speed up in carry propagation. Pass gate design accompanied with full swing signals reduce the leakage and short-circuit current and make it a low power circuit.

Table 1: Truth Table for the Proposed Structures

| C | B | A | $B \oplus C$ | $\overline{cout}$ | $\overline{sum}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $\overline{C}$ | $\overline{A}$ |
| 0 | 0 | 1 | 0 | $\overline{C}$ | $\overline{A}$ |
| 0 | 1 | 0 | 1 | $\overline{A}$ | $A$ |
| 0 | 1 | 1 | 1 | $\overline{A}$ | $A$ |
| 1 | 0 | 0 | 1 | $\overline{A}$ | $A$ |
| 1 | 0 | 1 | 1 | $\overline{A}$ | $A$ |
| 1 | 1 | 0 | 0 | $\overline{C}$ | $\overline{A}$ |
| 1 | 1 | 1 | 0 | $\overline{C}$ | $\overline{A}$ |

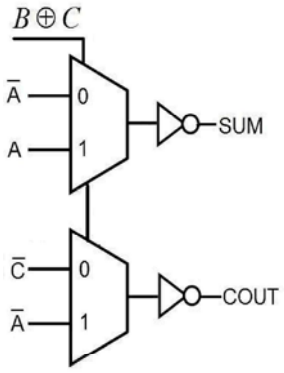


Fig. 2: The proposed logic to implement 1-bit full adder cell with one XOR gate

**Proposed Full Adder:** In this section, a new logic approach to design low power full adder is proposed. Afterward the proposed full adder will be illustrated.

**An Alternative Logic Approach:** As can be seen in Table 1, COUT and SUM can be produced using intermediate signal $B \oplus C$. The new logic approach will reduce the power consumption by eliminating power consuming XNOR gate compared to those use XOR-XNOR module. In order to increase the driving ability for high fan-out applications, the approach provides invert output signals, which will generate positive signals using common inverters.

**Proposed Full Adder Cell Circuit (Ss16t):** Logic block diagram of the proposed full adder has been showed in the Fig. 2. The proposed full-swing XOR gate in [19] has been used in this full adder. It uses 6 transistor and it has full swing output, low delay and power consumption. Two inverters between Cin and Cout act as a buffer that decreases the delay in propagating carry out. However using carry-in as input in XOR module increases the delay. Multiplexers are implemented using two transistors. Full swing XOR module avoids double $V_T$ threshold loss problem at the input of the output inverters and high leakage power consumption in the output inverters.

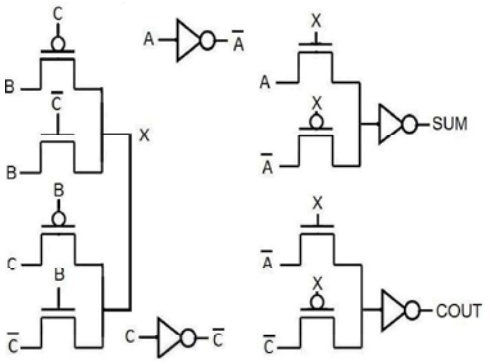


Fig. 3: The proposed full adder cell (SS16T

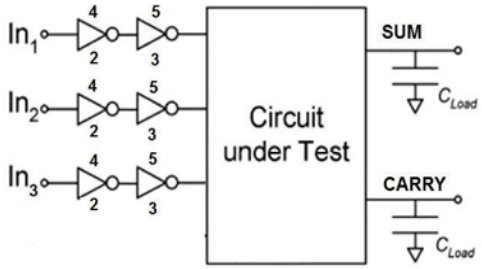


Fig. 4: Input buffers and output loads in the test environment.

**Simulation Setup:** All the netlists have been simulated using HSPICE in 0.18$\mu$m bulk technology. Output loads and input buffers have been added to the under the test circuits according to Fig. 4. Power and delay of the inverters are included in the power and delay calculation of the whole circuit. To study the properties of the compared circuits in cascaded fashion, 4-bit adder have been implemented from 1-bit cells. The transistor sizes in each cell are same as the other cells in an adder.

The performance of the under test circuits were evaluated in term of worst-case propagation delay. Propagation delay has been calculated from 50% of voltage level of input to 50% of voltage level of output. Rise time and fall time of the input signals in the all simulations are 5% of the pulse width. In this study, power means the total average power consumption. Power delay product has been calculated from production of worst-case delay and average power consumption.

Transistor sizing follows below rules. First, $L=L_{min}=0.18\mu$m. Second, $W$ for all NMOS transistors is equal to $2\times L_{min}$ and for PMOS Transistors is equal to $4\times L_{min}$. Third, if there are n serried transistors in a path, the size of them become n times larger. Forth, the transistor sizes should be changed in order to optimize

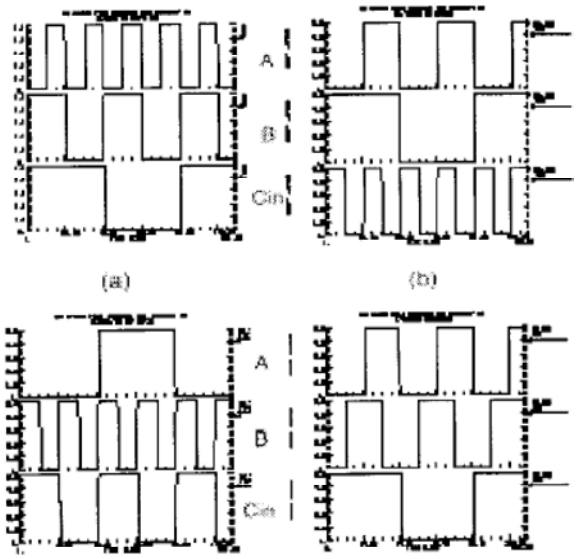


Fig. 5: Samples of input patterns to be applied to the compared circuits [20].

PDP in the circuit. In order to optimization, worst-case delay and power should be studied. All the circuits have been optimized in 1.8V supply voltage, 10fF output load and 100MHz input frequency conditions.

To compare the cells, several input patterns have to be applied to cover all the input cases. An input pattern, which maximize the power consumption for a given cell, could exhibit less power consumption for another cell [20]. Different patterns also show different delays for a given circuit [20]. With three inputs and three frequencies, there are 27 different input patterns. All the 27 input patterns have been applied to the under test circuits to fairly compare them. Fig. 5 shows four samples of them.

## RESULTS AND DISCUSSION

Fig. 6 (a) and (b) show the power consumption vs. supply voltage and output load respectively. CMOS power consumption, is more than the other compared circuits due to high number of transistors and internal nodes. Input capacitance is high because of large PMOS pull up network which causes high dynamic power dissipation. SERF consumes less power than CCMOS and higher than 16T. 16T has full swing outputs, thus it has better delay in comparison to SERF. Weak pull-up and pull-down network in generating signals and $H$ in New-14T, has been resulted in higher delay and power consumption than 16T, although the output stages are same in them (Fig. 6 (c) and (d)).

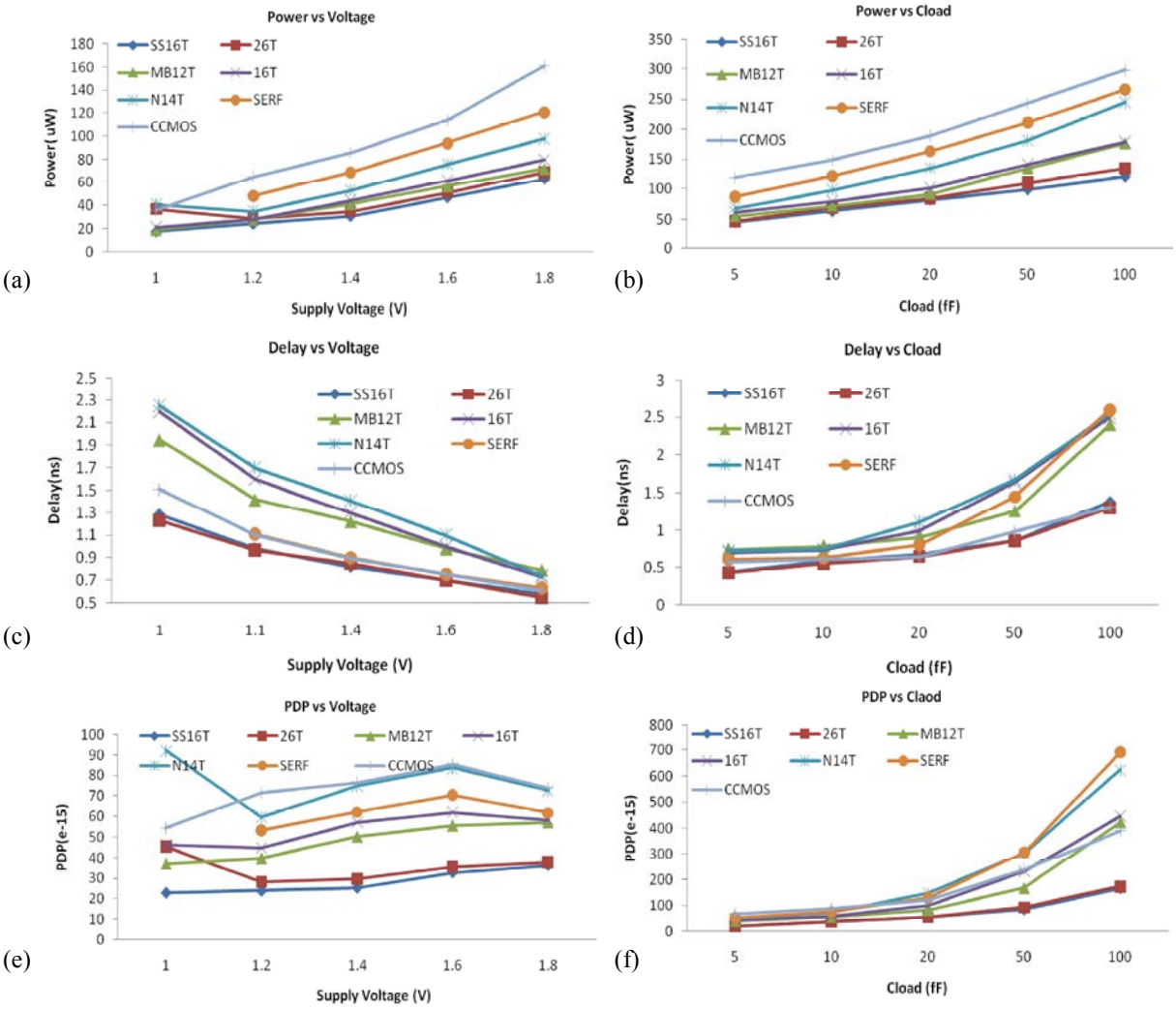


Fig. 6: Power and delay comparison vs. supply voltage, output load and frequency. (a) Power consumption vs. supply voltage. (b) Power consumption vs. output load (c) Delay vs. supply voltage (d) Delay vs. output load (e) PDP vs. supply voltage (f) PDP vs. output load.

Low number of transistors and low power pass gate design of 16T leads to less power consumption than CCMOS. However, pass gates lack of driving in high output loads. As Fig. 6 (d) shows, 16T has high delay in 100fF load, while 26T, CCMOS and SS16T have lower delay than the other compared circuits. Output inverters help mentioned circuits to improve driving ability, while it increases dynamic and static power consumption. SERF has highest delay in 100fF load, due to pass gate output and high threshold loss in output voltage. It can be seen in Fig. 6 (d) that 26T lagged SS16T in term of delay. Using carry in XOR module leads to higher delay than 26T, however Fig. 6 (a) and (b) are telling that the power consumption of SS16T is lower than 26T due to lower transistor count and using one XOR as intermediate signal.

Fig. 6 (c) and (f) show the PDP of the compared circuits vs. supply voltage and output load respectively. As can be seen N14T is not performing good in low voltages. It has high PDP in 1V supply voltage. SS16T has the lowest PDP in all supply voltages and 26T is in the second rank in term of PDP for supply voltages above 1.2V. SERF cannot function correctly in 1V supply voltage, thus there is no point for that in Fig. 6 (a), (c) and (e) in 1V supply voltage. In the Fig. 6 (f) the circuits are compared in various output loads in term of PDP. In high fan-out, the SS16T, 26T and CCMOS are the three top circuits in ranking. SERF shows the highest PDP in high loads.

Table 2: Simulation Results for 1.8V, 10fF and 100MHz.

| | PWR (uW) | DLY (ns) | PDP (e-15) | Max.Freq. (GhZ) |
|---|---|---|---|---|
| SS16T | 63 | 0.56 | 36.5 | 1.72 |
| 26T [15] | 69 | 0.55 | 37.9 | 1.82 |
| MB12T [17] | 72 | 0.79 | 56.8 | 1.27 |
| 16T [13] | 80 | 0.73 | 58.4 | 1.37 |
| NEW14T [14] | 98 | 0.74 | 72.5 | 1.35 |
| SERF [5] | 121 | 0.63 | 76.2 | 1.59 |
| CCMOS [12] | 161 | 0.61 | 98.2 | 1.64 |

The value of the simulation results for 1.8V with 10fF output load are in Table 2. The values are sorted in term of power consumption. As can be seen the proposed circuit, is low power full adder, however it is not good circuit for high-speed applications. On the other hand, 26T has higher power consumption and higher speed than SS16T. In term of number of transistors, SERF with 10 transistors is the best circuit of this study. For normal applications which PDP is more important than delay, SS16T is better than the other compared circuits.

## CONCLUSION

One full-swing full adder cell based on a new logic approach was proposed in this paper. The new full adder employed one XOR gate as intermediate signal in order to reduce power consumption. The proposed circuit was simulated using HSPICE and compared to several full adders in the literature. The results show that there is improvement in term of PDP. In addition, simulation for high output loads show that full-swing full adders with output inverters have higher speed than the other with no output inverters or non-full swing outputs for the compared circuits in this study. Study of the compared circuit with different transistor count shows that, lowering the number of transistors does not always mean power reduction.

## REFERENCES


1. Walid M. Elgharbawy and Magdy A. Bayoumi, 2005. Leakge sources and possible solutions in nanometer CMOS technology, Ieee Circuit and System Magazine, pp: 6-16.
2. Bui, H.T., Y. Wang and Y. Jiang, 2002.. Design and analysis of 10-transistor full adders using XOR-XNOR gates, IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., 49(1): 25-30.
3. Kumar, A. and M.A. Bayoumi, 2006. Design of robust Energy Efficient Full Adders for Deep-Submicrometer Design Using Hybrid-CMOS logic Style, IEEE Trans. VLSI, Vol. 14, No. 12.
4. Lynch, T. and E. Swartzlander, 1992. A spanning tree carry lookahead adder, IEEE Trans. Comput., 41: 931-939.
5. Shalem, R., E. John and L. K. John, 1999. A novel low-power energy recovery full adder cell, in proc. of GLSVLSI, pp: 380-383.
6. Navi, K., M. Maeen, V. Foroutan, S. Timarchi and O. Kavei, 2009. A Novel low power full-adder cell for low voltage, Integration the VLSI J.,
7. Navi, K., V. Foroutan, B. Mazloomnejad, S.H. Bahrololoumi, O. Hashempour and M. Haghparast, 2008. A six transistor full adder, World Applied Science J.,
8. Zhuang, N. and H. Wu, 1992. A new design of the CMOS full adder, IEEE J. Solid-State Circuit 27, May 1992. 840-844.
9. Elgamel, M.A., S. Goel and M.A. Bayoumi, 2003. Noise Tolerant Low Voltage XOR-XNOR for Fast Arithmetic, GLSVLSI,
10. Zhuang, N. and H. Wu, 1992. A new design of CMOS full adder, IEEE J. Solid-State Circuits, 27(5): 840-844.
11. Navarro-Botello, V., J.A. Montiel-Nelson and S. Nooshabadi, 2007. High performance low power CMOS dynamic logic for arithmetic Circuits Microelectronics J., pp: 482-488.
12. West, N. and K. Eshraghian, 1993. Principles of CMOS VLSI design, system prespective reading, MA: Addison-Westly, 1993.
13. Shams, A.M. and M.A. Bayoumi, A Novel high performance CMOS 1-bit full adder cell, IEEE Trans. Circuits and Systems II: Analog digital Signal Process. 47 (2000), Vol. 47, No. 5, MAY 2000.
14. Radhakrishnan, D., 2001. "Low-voltage low-power CMOS full adder," *IEE* Proc. Circuits Devices Syst., 148(1): 19-24.
15. Chang, C.H., J. Gu and M. Zhang, 2005. A review of 0.18-_m full adder performances for tree structured arithmetic circuits, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 13(6): 686-695.
16. Goel, S., A. Kumar, M.A. Bayoumi, 2006. Design of Robust, Energy-Efficient Full Adders for Deep-Submicrometer Design Usong Hybrid-CMOS Logic Style, IEEE Trans. on VLSI Systems, Vol. 14, No. 12, Dec. 2006.
17. Jiang, Y., A. Alsheridah, Y. Wang, E. Shah and J. Chung, 2004. A Novel Multiplexer-Based Low Power Full adder, IEEE Trans. On Circuits and Systems, Vol. 51, No. 7, July 2004.

18. Veeramachaneni, S. and M.B. Sirinivas, 2008. New improved 1-bit full adder cells, CCECE/CGEI, Canada,
19. Tung, C., S. Shieh, Y. Hung and M. Tsai, 2006. High-Performance low-power full swing adder cores with output driving capability, IEEE Asia Pacific Conference on. Publication,
20. Shams, A.M., T.K. Darwish and M.A. Bayoumi, 2002. Performance analysis of low-power 1-bit CMOS full adder cells, IEEE Transaction on large scale integration (VLSI), Vol. 10, No. 1, Feb. 2002.
21. Navi, K., S. Daraeizadeh, B. Mazloomnejad and M. Haghparast, Novel Current Mode Full Adder Based on Majority Function, WASJ, 2008.