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A Novel Low Power Adiabatic Based Sram Design Using Latest Nano-Devices for Memory Array

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Abstract: In this paper, we change the topological structure of SRAM cell Since in a Memory design, SRAM is the main source of leakage current and consumes more power during its operation. Due to more power consumptions, speed of the circuit will be reduced finally the performance will be degraded. By changing its structure it has reduced power and enhances its performance. This paper deals with a new method of incorporating adiabatic logic like use of adiabatic switch and ECRL in conventional designs. These proposed designs have reduced power and noise compared to conventional design and thus the proposed designs are further implemented in latest nano-devices. Simulations are carried out using Tanner EDA Tool and HSPICE Synopsis.

Key words: SRAM · Efficient Charge Recovery Logic (ECRL) · Adiabatic logic · Switch · Tanner EDA · Power and noise analysis

INTRODUCTION

In a given process technology, the process constraints such as gate-oxide reliability limits and reduced gate-oxide thickness determines the maximum supply voltage of the transistor [4]. For a given performance requirement, the minimum SRAM supply voltage is limited by the increased process variations which includes both random and die-to-die and the increased sensitivity of circuit parameters at lower supply voltage.

Hence, the SRAM cell operation is enabled by lowering the wide range of supply voltage. Such that Read-Write operation and bit cell configurations are explored. Basic operation of access transistor is controlling the magnitude and the duration of different node biases such as word-lines, bit lines, bit cell VSS node and bit cell VCC node. This project mainly aims in incorporating adiabatic logic in SRAM cell. SRAM cell design can be carried out using new approaches like Single Bit line adiabatic logic based SRAM cell and Efficient Charge Recovery Logic (ECRL) based SRAM cell [1, 8]. These designs therefore reduce power and hence reduce heat dissipation. Further these designs are carried out using various Nano-devices.

Conventional Sram Design: The key component of Static Random Access Memory for storing binary information is SRAM cell [12]. A conventional SRAM cell has two cross-coupled inverters forming a latch and access transistors. The purposes of Access transistors are to enable access the cell during read and write operations and provide isolation during the not-accessed state. An SRAM cell is designed to provide non-destructive read access, write capability and data retention for as long as the cell is powered.

For instance, low-power can compromise the cell area also speed of operation. The Conventional CMOS SRAM normally has 6 transistors in which four transistors (Q1-Q4) comprises of cross-coupled CMOS inverters and remaining two NMOS transistors Q5 and Q6 perform read and write access to the cell. A 6T CMOS SRAM cell is the most popular SRAM cell because of its superior robustness, low power and low-voltage operation [7].

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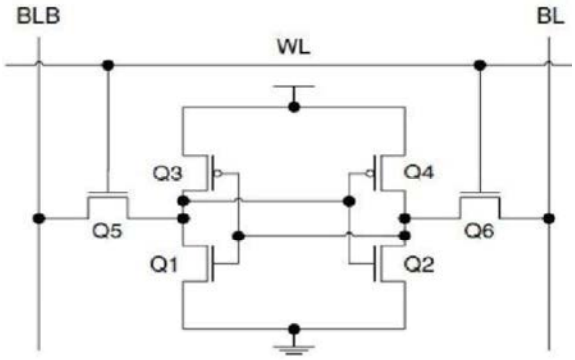


Fig. 1: Conventional 6T SRAM Cell

Proposed Designs: The main purpose of this paper is to reduce the Read-Write delay and power consumptions. For doing so we are incorporating adiabatic logic in the conventional SRAM design [1]. This logic performs by ENERGY RECOVERY PROCESS. In order to reduce the dissipation, circuit designer must minimize the switching activities, decrease the node capacitances, reduce the voltage swing or by applying the combination of these methods. All these cases results in energy drawn from the power supply and used only once before being dissipated. Such that the energy efficiency can be increased by introducing recycle of energy drawn from the power supply. This can be done by adiabatic logic which offers the possibility of further reducing the energy dissipation during switching and also reuse some of the energy drawn from the supply. To achieve this goal, we have to modify the circuit topology and the operation principles [3]. The amount of energy recycled using the adiabatic techniques can also determined by the fabrication technology, switching speed and the voltage swing.

Firstly, we design an adiabatic switch by removing one of bit lines [10]. Thus switch reduces the relay in SRAM operation. Single bit line SRAM design enhance the performance of the design and it is far better than the Memory system consist of pre-charge circuit and sense amplifier flip-flops [5].

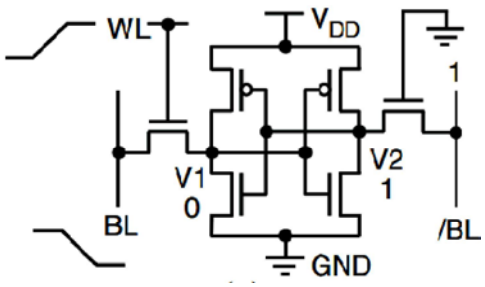


Fig. 2: Single bit line SRAM design

Secondly, we design the cross coupled inverters of conventional one using ECRL logic. This logic is proposed as low-energy adiabatic logic circuit. Power comparison with other logic circuits is performed on an inverter chain [11]. It supports a new method of performing pre-charge and evaluation simultaneously. ECRL then wipe outs the pre-charge diode and less energy is dissipated compared to other adiabatic circuits [2].

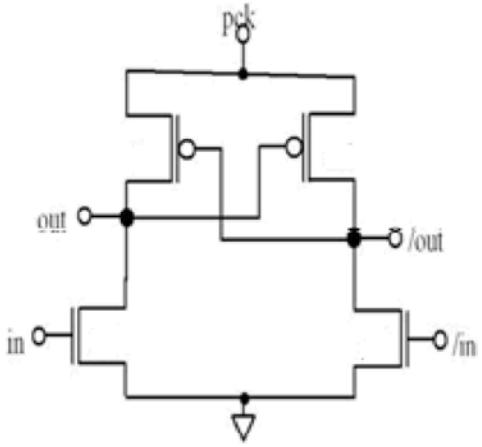


Fig. 3: ECRL Inverter

Further these proposed designs are finally implemented using FinFET and CNTFET for efficient use in Memory Arrays [6]. The main drawback of using CMOS transistors are high power consumption and high leakage current. Fin-type field-effect transistors (FinFETs) are promisingly substitutes the bulk CMOS in nano- scale circuits. FinFETs have two gates, such that the source and drain terminals are shorted. This double-gate (DG) FinFETs has better short channel effects performance compared to the conventional CMOS and stimulates technology scaling. It is more versatile than the single-gate FETs since the two gates can be controlled independently. Usually, the second gate of FinFET transistors controls the threshold voltage of the first gate and thereby improves the performance as well as reduces leakage power [9]. As one of the promising new devices, CNFET avoid most of the fundamental limitations for traditional silicon devices.

Simulation and Waveform: The below waveforms are obtained by simulating the designs in Tanner EDA under 18nm technology for computing various parameters like power, delay and noise.

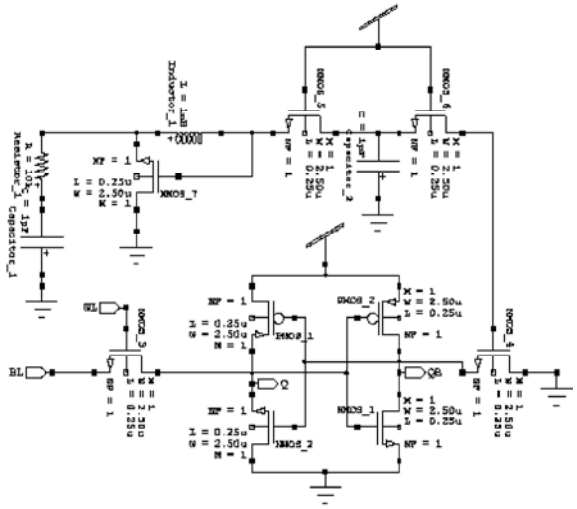


Fig. 4: Schematic of Single bit line Adiabatic SRAM design

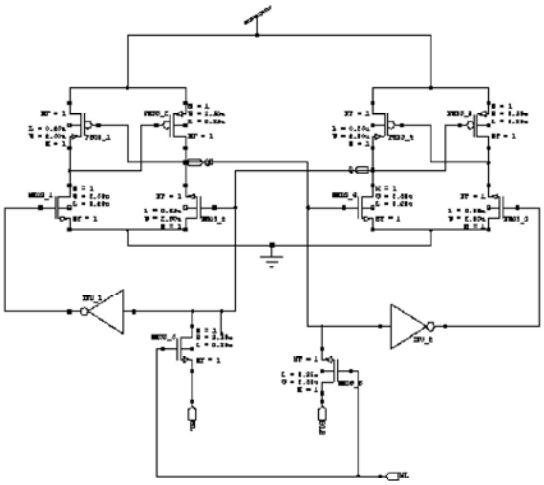


Fig. 5: Schematic of ECRL based SRAM design

SRAM waveforms are similar irrespective of the techniques used. But the leakage power is greatly varies in proposed designs. Waveforms of CMOS proposed designs are as follows in Fig No. 5 and these waveforms are obtained for Voltage vs Time.

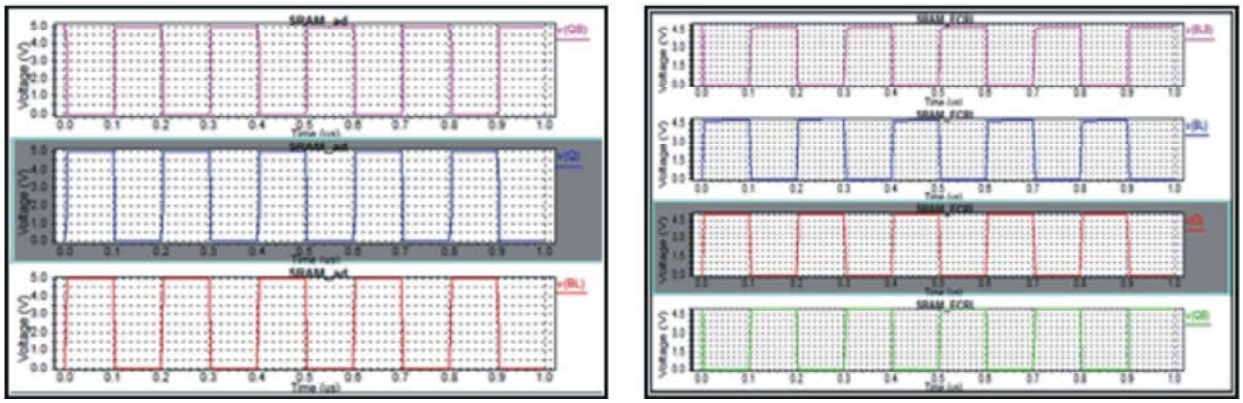


Fig. 6: Waveforms of CMOS based proposed Designs

The simulation results of FinFET and CNTFET based proposed designs are as follows in Fig. 7 and 8. These simulations are carried out in HSPICE Synopsis.

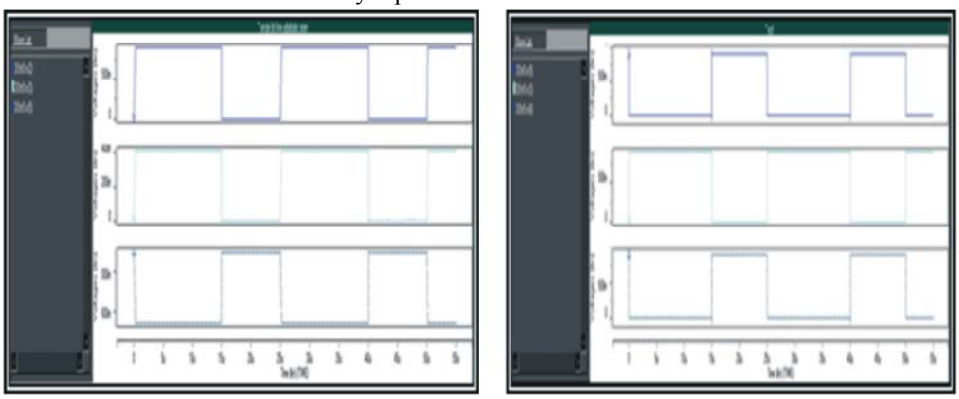
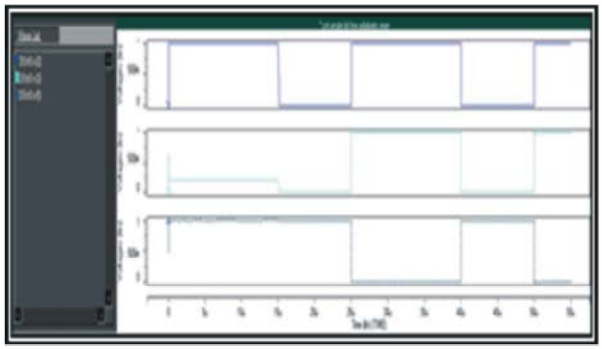


Fig. 7: Waveforms of FinFET based SRAM designs



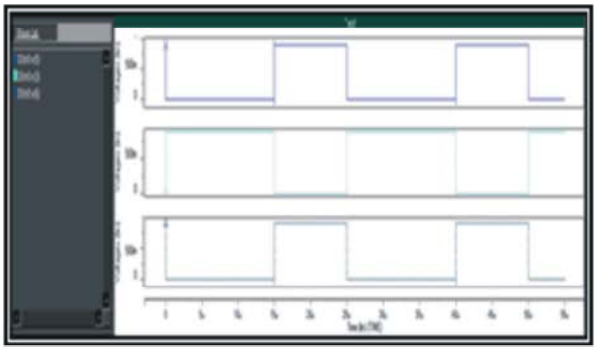


Fig. 8: Waveforms of CNTFET based SRAM designs

From the waveform, whatever the input given in bit Line (BL) will reflect the same in one of the outputs Q and similarly whatever the input given in bit Line Bar (BLB) will reflect the same in one of the outputs QB.

RESULTS

Power consumption is computed for all the designs using Tanner EDA and HSPICE Synopsis. It includes static, dynamic and also average power consumed.

Table 1: Power consumption in CMOS based SRAM Designs

Design	Dynamic Power (watts)	Static Power (watts)
Conventional SRAM	3.695663e-004 watts	6.322254e-007 watts
Single Bit-Line Adiabatic SRAM	3.079335e-004 watts	6.321068e-007 watts
ECRL based SRAM	3.196039e-006 watts	4.169862e-010 watts

Table 2: Power Consumption in FinFET based SRAM Designs

Design	Average power (watts)
Single Bit Line Adiabatic SRAM	1.648e-07
ECRL based SRAM	1.996e-09

Table 3: Power Consumption in CNTFET based SRAM Designs

Design	Average power (watts)
Single Bit Line Adiabatic SRAM	1.921e-06
ECRL based SRAM	1.386e-08

From the above power analysis, ECRL based SRAM design has reduced power consumption during active and idle mode of operation compared to other designs.

Noise analysis can be performed in 0.18um technology at a temperature of 25 deg C. The devices work normally at this temperature i.e., $T_{nor.}$ The output noise and their transfer function of existing and the proposed methods are then compared for various frequencies. This analysis mainly deals with the input noise, output noise and resulting transfer function. Thus the transfer function is obtained as,

$$TF = \frac{Vout}{Vin}$$

Table 4: Noise Analysis for SRAM Designs

Freq	Design	Squared Output Noise Sq V/Hz	Transfer function (Vout/vin)	Input Noise
2 MHz	6T SRAM Cell	8.43756a	999.983m	2.9047n
	Single Bit Line Adiabatic SRAM Cell	8.43756a	999.982m	2.9048n
	ECRL based SRAM Cell	8.43751a	999.983m	2.9047n
20 MHz	6T SRAM Cell	8.43749a	999.979m	2.9048n
	Single Bit Line Adiabatic SRAM Cell	8.43749a	999.978m	2.9048n
	ECRL based SRAM Cell	8.43735a	999.974m	2.9047n
50 MHz	6T SRAM Cell	8.43710a	999.954m	2.9048n
	Single Bit Line Adiabatic SRAM Cell	8.43709a	999.953m	2.9048n
	ECRL based SRAM Cell	8.43650a	999.923m	2.9047n
1 GHz	6T SRAM Cell	8.15669a	982.059m	2.9081n
	Single Bit Line Adiabatic SRAM Cell	8.15040a	981.247m	2.9094n
	ECRL based SRAM Cell	7.84638a	963.781m	2.9064n
5 GHz	6T SRAM Cell	5.54048a	798.053m	2.9494n
	Single Bit Line Adiabatic SRAM Cell	5.54345a	793.533m	2.9670n
	ECRL based SRAM Cell	3.90848a	678.409m	2.9141n
20 GHz	6T SRAM Cell	1.20282a	404.788m	2.7094n
	Single Bit Line Adiabatic SRAM Cell	1.332624a	411.699m	2.7972n
	ECRL based SRAM Cell	5.467e-019	341.212m	2.1668n

CONCLUSION

The proposed designs greatly reduce static as well as dynamic power consumption compared to conventional SRAM design. These designs also have reduced noise compared to conventional one. These adiabatic logics efficiently reduce the energy dissipated during switching events by reusing some of the energy drawn from the power supply. The Cell topology and the operations are thus modified, sometimes drastically. Finally the FinFET and CNTFET based designs also shows reduced power consumption. Further using this low power proposed designs, Memory Array can be implemented

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