Middle-East Journal of Scientific Research 25 (4): 816-821, 2017
ISSN 1990-9233

DOI: 10.5829/idosi.mejsr.2017.816.821

Implementation of Low Power Clocking System in Power Efficient Flip-Flop

P. Jeya priyanka and U. Satheeshwaran

Assistant Professor, Department of ECE, Jeppiaar Engineering College, Chennai, India

Abstract: In this brief, a new power efficient flip flop is presented. The objective of this work is to reduce the power consumption of the total network by reducing the clock distribution network. The new proposed single edge triggered flip flop (PSETFF) which dissolves the floating node problem by introducing the pseudo n-mos technology. Instead of double edge triggering here a single edge triggering is introduced in clock distribution network. The split path technique is presented which is used to reduce the short circuit current and switching activity of the circuit. The performance of the proposed flip flop is superior when compared to the conventional techniques. In proposed design the overall power consumption is reduced from 45.13% to 56.6% and area saving from 26.31% up to 63.3% respectively.

Key words: Flip-flops · Low power consumption · Register element · Single edge triggering

INTRODUCTION

In the past, the major concerns of the VLSI design were performance, area, cost and reliability. The power consideration is secondary only but in recent years it has been changed and increasingly, power is being given comparable weight to area and speed considerations. As the counts of transistor the clock frequencies have increased, the primary design is designed by the constraint compared to power, area and speed. Instantaneously the product of the supply voltage Vdd and the supply current idd(t) is proportional to the power p(t) [1].

$$P(t) = Vdd * idd(t)$$

Power consumption is determined by the factors such as frequency(f), Supply voltage(v), data activity factor(α), Capacitance(C).The total power consumption of the system is expressed as

$$Ptotal = Pstatic + Pdynamic + Pshortcircuit$$

The total power consumption of the system is the summation of the static power, dynamic power and the short circuit power.

$$Pdynamic = \alpha CV^2f$$

The above equation is which express the dynamic power consumption. The short circuit power consumption which is caused by the finite rise and fall time of the input signal which results in both pull up and pull down network to be ON for short while [2].

$$Pleakage = Ileakage * Vdd$$

Leakage is a dominant now because whenever the sub threshold leakage current occurs when the supply voltage is scaling down then the threshold voltage also decreases to maintain the performance. There are many different ways to lower the power consumption based on the following factors [3].

- Capacity of Clocked load reduction
- Low swing Voltage on Clock Distribution
- The ways to reduce switching activity
- Clock gating
- Conditional operation
- Reduction of Short circuit Power
- Edge triggering method

Flip Flop Archetecture Analysis: In this paper four types of techniques have been analysed. They are Conditional Data Mapping Flip flop(CDMFF), Cross Charfe Controlled Flip flop(XCFF), Dual Dynamic node hybrid Flip flop(DDFF) and Double Edge Triggered Flip flop (DETFF).

Corresponding Author: P. Jeyapriyanka, Assistant Professor, Department of Electronics and Communication Engineering, Jeppiaar Engineering College, Chennai, India.

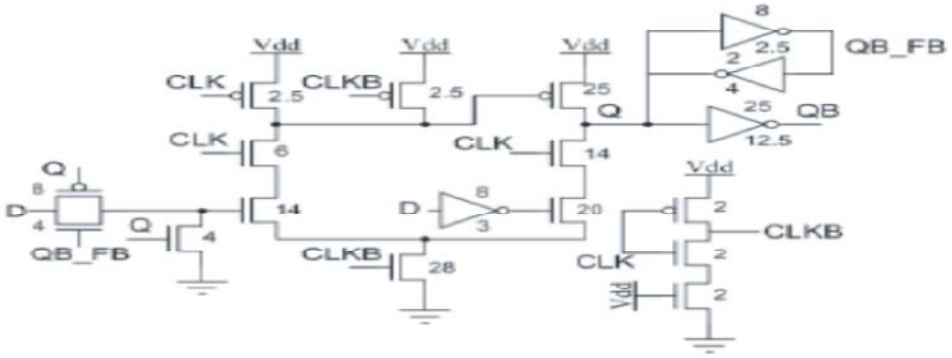

Fig. 1: Conditional Data Mapping Flip-flop (CDMFF)

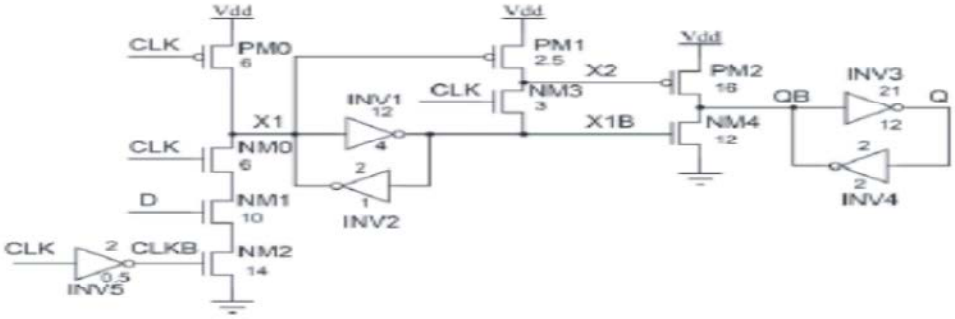

Fig. 2: Cross charge Controlled Flip-flop (XCFF)

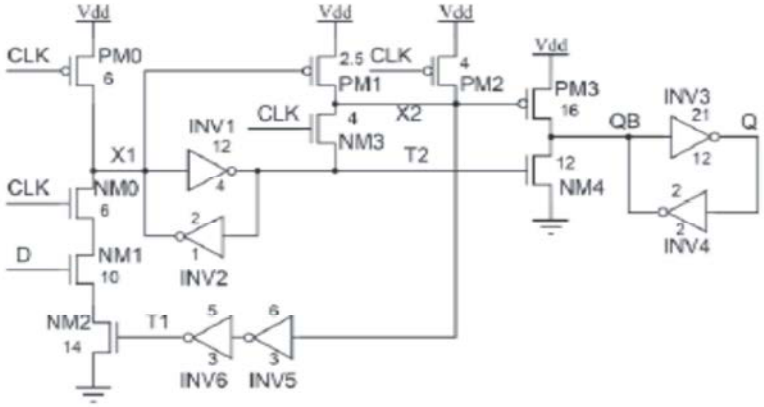

Fig. 3: Dual Dynamic node hybrid Flip-flop (DDFF)

The Conditional Data Mapping Flip flop (CDMFF) is shown in Fig. 1 is one of the method for reducing the redundant data transistors. It is a Single edge triggered flip flop here the total number of transistor is 22 it uses 15 unclocked transistors and 7 clocked transistors [4]. The input data is given in first stage and the output data is in second stage this method has floating node on critical path because first stage is dynamic. It is not used in noise environment and it is difficult to apply low power techniques [5]. The redundant data transistions and large capacitance are the two major sources of power dissipation in the conventional semi-dynamic designs [6]. The CDMFF method is used to reduce the redundant data trnsistion. Another one drawback is precharge node to overcome this drawback moving to XCFF method (Cross Charge Controlled flip flop) this is shown in Fig. 2 here by splitting the dynamic node into two it will separates the pull-up and pull-down transistors to reduce the power dissipation. When the complex functions are embedded into the design therefore charge sharing becomes uncontrollable [7].

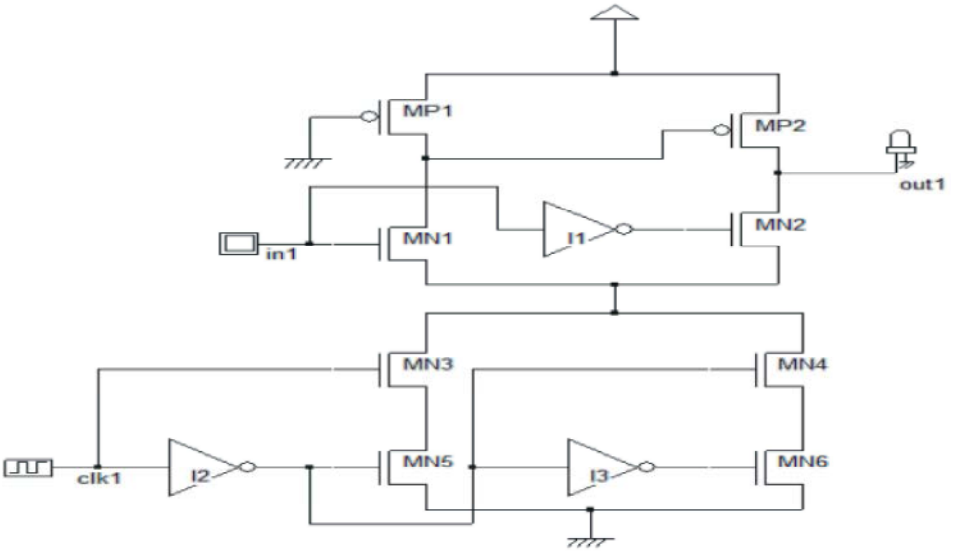

Fig. 4: Double Edge Triggered Flip-flop(DETFF)

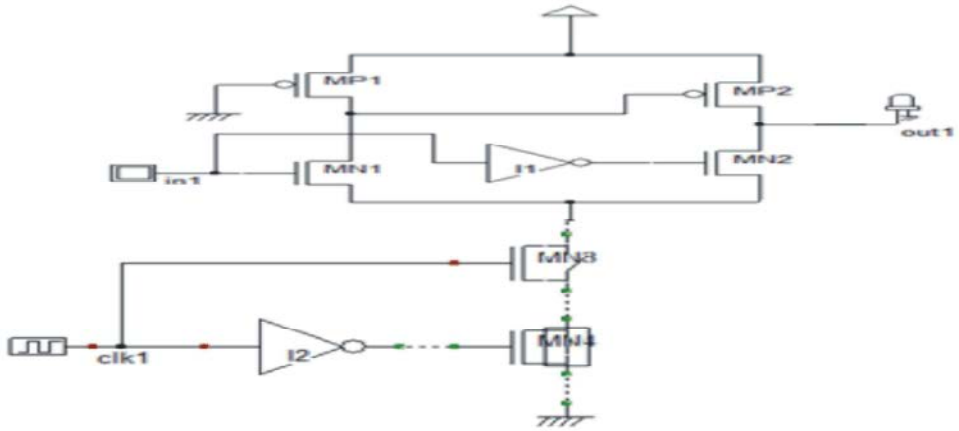

Fig. 5: Proposed Single Edge Triggered Flip flop(PSETFF)

Proposed Single Edge Triggered Flip Flop (PSETFF): The proposed Single Edge Triggered Flip-flop(PSETFF) is shown in Fig. 5. In this proposed design it has 10 transistors including 4 clocked transistors and 6 unclocked transistors [8]. The single edge triggering operation is done by the MN3, MN4 transistors and an Inverter I2. If the clock signal is high then the MN3 transistor will be in ON condition and then the clock. signal will pass through the circuit. If the clock signal is low then the MN4 transistor will be in ON condition then the whole circuit will be shorted to ground. In latch side it has six transistors MN1, MN2, MP1, MP2 and I1 (2 transistors). The gate terminal of the P-mos MP1 transistor is grounded in the circuit which remains the MP1 transistor is in ON condition continuously, so that the drain terminal of the MP1 transistor is high for most of the time [9]. The MP2 is connected by MP1 by split path technique this will reduce the switching activity and short circuit currents. The results of the proposed flip flop is based on 4 operations, operation 1 is when D=0 and CLK=0 then the respective output also 0. Operation 2 is when D=0 and CLK=1 then the respective output also 0. Operation 3 is when D=1 and CLK=0 then the respective output is 1 [10]. Operation 4 is when D=1 and CLK=1 then the respective output is 1. The simulation results were obtained from DSCH & MICROWIND3.1 simulations in 0.12µm CMOS technology at room temperature Vdd is 1.8V. A clock frequency of 250 MHZ is used. Each design is simulated using the circuit at the layout level. Performance parameters such as area, power and delay are obtained by layout simulation. The Table shows the comparison of total number of transistors, total number of clocked transistors, area, power and delay [11].

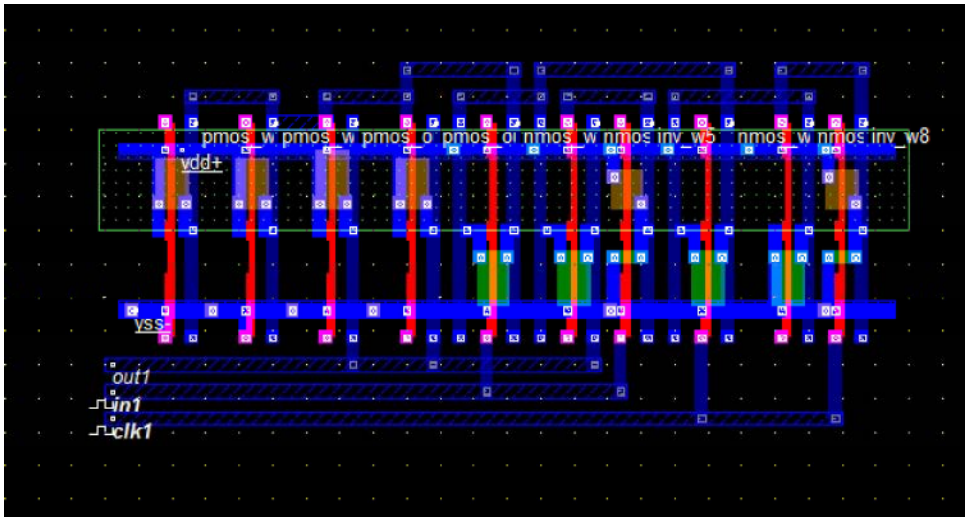

Fig. 6: Layout design of PSETFF

Table: Comparison of No. of transistors, No. of clocked transistors, Area and Total power consumption

Flip flop	No. of tansistor	No. of clocked transistor	Area(μm²)	Power(μw)
CDMFF	22	7	462	13.3
XCFF	21	4	312	14.3
DDFF	18	6	276	13.8
DETFF	14	8	228	11.3
PSETFF	10	4	168	6.23

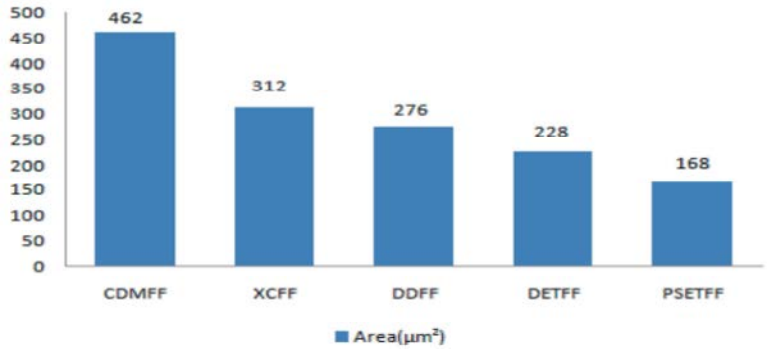

Fig. 7: Comparison of Area

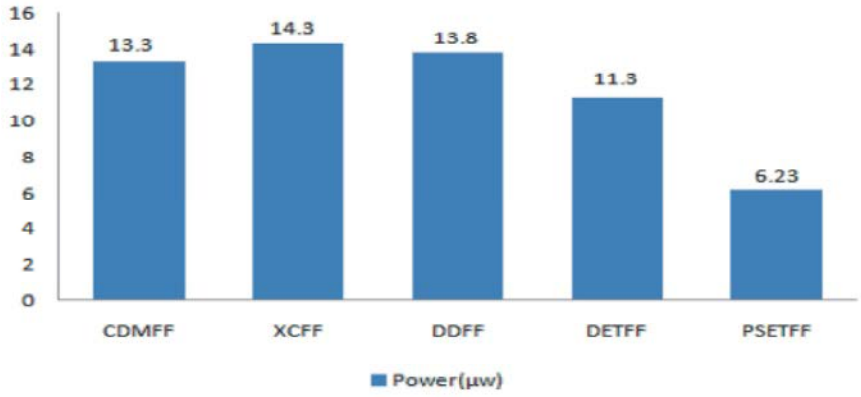

Fig. 8: Comparison of power consumption

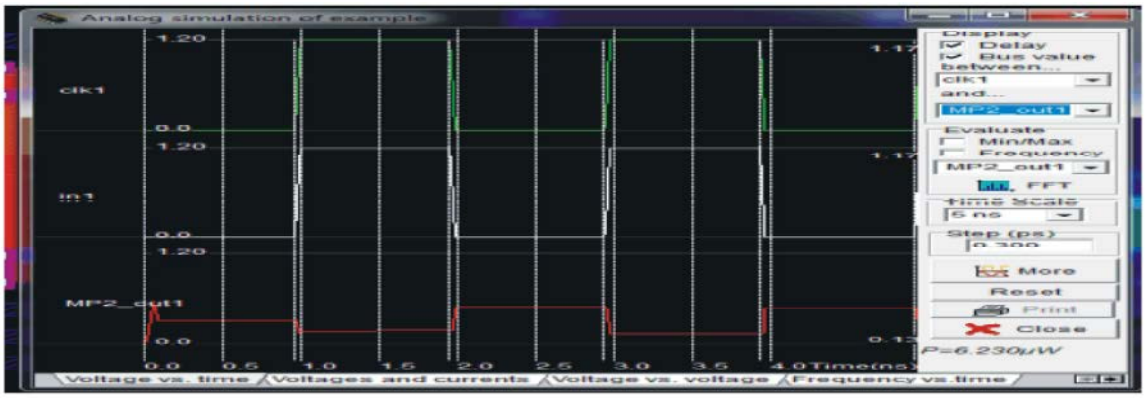

Fig. 9: Output waveform of PSGTFF

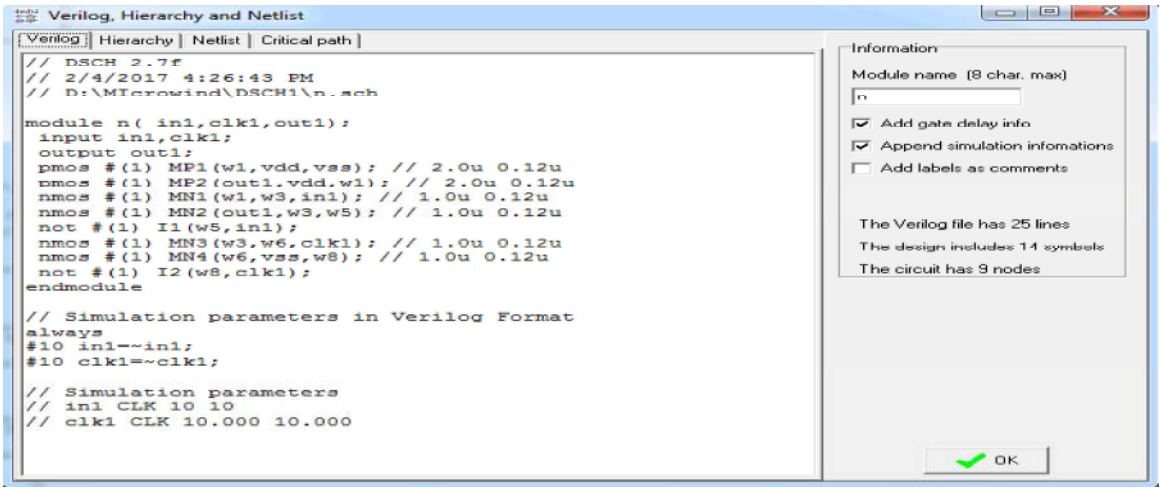

Fig. 10: Verilog file for PSETFF

CONCLUSION

In this paper several design techniques for register elements are reviewed. One effective method, Single edge triggered is elaborated. Following this approach, Single edge triggering flip-flop is proposed, which reduces power about 45.13% to 56.6% and area about 26.31%14 to 21%. The performance analysis is carried out on the register element. In the view of power consumption and area, the proposed SDETFF out performs prior arts in register element design.

REFERENCES

1. Gabariyala Sabadini, C. and P. JeyaPriyanka, 2015. Design and analysis of flip flops for low power clocking system ISSN:2348-8549, ICETSH-2015.
2. Sakurai, T., 1997. Low –power CMOS design through Vth control and low swing Circuits, in Proc. ISLPED, pp: 1-6
3. Chandrakasan, W. Bowhill and F. Fox, 2001. Design of High-Performance Microprocessor Circuits, 1st ed. Piscataway, NJ: IEEE Press.
4. The, C.K., M. Hamada, T. Fujita, H. Hara, N. Ikumi and Y. Oowaki, 2006. Conditional data mapping flip-flops for low-power and high-performance systems, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 14(12): 1379-1383.
5. Markovic, D., B. Nikolic and R. Brodersen, 2001. Analysis and design of low-energy flip-flops, in Proc. Int. Symp. Low Power Electron. Des., Huntington Beach, CA, pp: 52-55.
6. Kong, B., S. Kim and Y. Jun, 2001. Conditional-capture flip-flop for statistical power reduction, IEEE J. Solid-State Circuits, 36(8): 1263-1271.
7. Kawaguchi H. and T. Sakurai, 1998. A reduced clock-swing flip-flop(RCSFF) for 63% power reduction, IEEE J. Solid-State Circuits, 33(5): 807-811.

8. Kalarikkal Absel, Lijo Manuel and R.K. Kavitha, 2013. Low-power Dual Dynamic Node Pulsed Hybrid flip-flop Featuring Efficient Embedded Logic, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 21(9): 1693-1704.
9. Kim, L. and S. Kang, 2002. A low-swing clock double edge-triggered flip-flop, IEEE J. Solid-State Circuits, 37(5): 648-652.
10. Zhao, P., J. McNeely, P. Golconda, M.A. Bayoumi, W.D. Kuang and B. Barcenas, 2007. Low power clock branch sharing double-edge triggeredflip-flop, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 15(3): 338-345.
11. Zhao, P., T. Darwish and M. Bayoumi, 2004. High-performance and low power conditional discharge flip-flop, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 12(5): 477-484.
00. Peiyi Zhao, Pradeep Golconda, Magdy A. Bayoumi, Robert A. Barcenas and Weidong Kuang, 2003. Low-Power Clock Branch Sharing Double-Edge Triggered Flip-Flop, IEEE Trans. Very Large Scale. Mar-2003.