Middle-East Journal of Scientific Research 25 (2): 341-347, 2017
ISSN 1990-9233

DOI: 10.5829/idosi.mejsr.2017.341.347

Performance Evaluation of Seven Level Cascaded H-Bridge Quasi Z -Source Inverter Using Fuzzy Logic Controller

F.X. Edwin Deepak

Assistant Professor, Electrical and Electronics Engineering, PSNACET, Dindigul, India

Abstract: In the area of Power Electronics, the DC/AC phase deposition Pulse Width modulation inverter have been used in industrial application. The quasi- z source seven level inverter typically integrate the stair-case output voltage waveform which has reduced harmonic content. This paper describes the development of design and simulation of the proposed seven level quasi-Z-source cascaded H-bridge inverter (QZS-CMI) systems which inherits the advantages of traditional CMI while overcoming issues with imbalance DC-link voltages. This inverter can produce a better sinusoidal waveform by increasing the number of output voltage levels. This paper also aims to analyse and total harmonic distortion in seven level cascaded H-bridge inverters and evaluates THD in the respective outputs. Simulations of the circuit have been executed in MATLAB/Simulink and the results were verified using fuzzy logic controller.

Key words: Cascaded Multilevel Inverter (CMLI) · quasi-Z-source multilevel inverter (QZS-CMI) · Total Harmonic Distortion (THD) · Fuzzy logic Controller

INTRODUCTION

In recent years, applying various multilevel inverter topologies is getting more and more attention due to the large power-scale and high voltage demands. Among various topologies, Cascaded H-Bridge (CHB) inverter has unique advantages. However, the DC-link voltage in each inverter module is a constant. This case there is no need for voltage balancing circuit [1-2]. Furthermore, in the conventional cascaded multilevel inverter (CMI) based PV system, each module is a buck inverter because the first component of the output AC voltage, always is lower than the input DC voltage [3-5]. The quasi-Z-source inverter (QZSI) has been employed for power generation system due to some unique advantages and features. Unlike quasi Z-source inverter, ZSI has a discontinuous input current during the shoot-through state due to the blocking diode. Quasi-Z-source cascaded multilevel inverter (QZS-CMI) is proposed which inherits the advantages of traditional CMI [6, 7].

Modern power electronics based devices have put a great effect on the development of new powerful applications and industrial solutions. But at the same time, these advances have increased the harmonic problems in line currents, which make distortion in the voltage waveform. The series connection of several bridges allows working with much higher voltages and the stepped voltage waveforms to eliminate the voltage stress in associated equipment, such as transformers. Moreover, the bridges of each converter work at a very low switching frequency which allows working with Low switching frequency losses. The multilevel inverters perform power conversion in multilevel voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility and higher voltage capability. Considering these advantages, multilevel inverters have been gaining considerable popularity in recent years [8].

Comparing conventional two level inverter systems with multilevel inverter systems has the advantages that the lower harmonic components on the output voltages can be eliminated and EMI problem could be decreased [9-10]. Due to these merits, many researches on multilevel inverters have been performed at simulations and an idea of using multilevel inverter instead of conventional inverter is developed.

Topology Description: The topology of the seven- level Quasi Z-Source inverter consists of a series of single phase H bridge inverter units, Quasi Z Source impedance networks and DC voltage sources. DC sources can be obtained from batteries, fuel cells, solar cells.

Corresponding Author: F.X. Edwin Deepak, Assistant Professor, Electrical & Electronics Engineering, PSNACET, Dindigul, India.

Quasi Z-Source Inverter: The QZSI extends several advantages over the ZSI such as continuous current from the input DC source, cut down component ratings and enhanced reliability. Figure 1 shows the basic topology of QZSI.

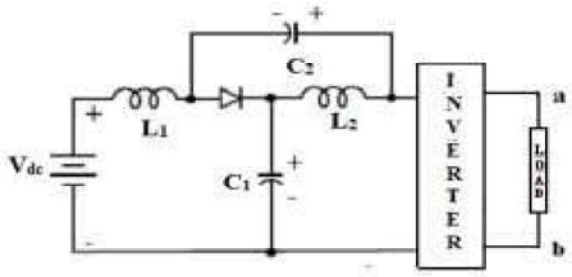


Fig. 1: Basic Topology Of Quasi Z Source Inverter.

Modes of Operation and Circuitanalysis: The two modes of operation of a quasi z-source inverter are:

- Non-shoot through mode (active mode).
- Shoot through mode.

Active Mode: In the non-shoot through mode, the switching pattern for the QZSI is similar to that of a VSI.

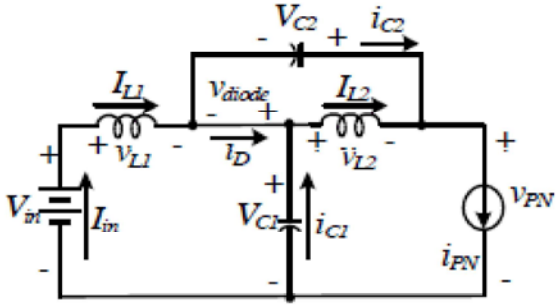


Fig. 2: Active mode of QZSI

The inverter bridge, viewed from the DC side is equivalent to a current source., the input dc voltage is available as DC link voltage input to the inverter, which makes the QZSI behave similar to a VSI.
During the interval of the non-shoot-through states, *T*1

$V_{L1} = V_{in} – V_{C1}, V_{L2} = -V_{C2}$
$V_{PN} = 0, Vdiode = V_{C1} + V_{C2}$

Shoot Through Mode: In the shoot through mode, switches of the same phase in the inverter bridge are switched on simultaneously for a very short duration. The source however does not get short circuited when attempted to do so because of the presence LC network, while boosting the output voltage [11]. The DC link voltage during the shoot through states, is boosted by a boost factor, whose value depends on the shoot through duty ratio for a given modulation index.

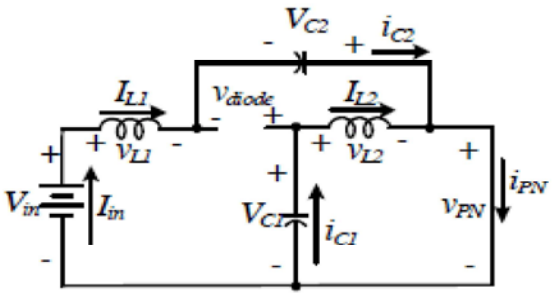


Fig. 3: Shoot through mode of QZSI

Assuming that during one switching cycle, T,
The interval of the shoot through state is T_0 ;
The interval of non-shoot-through states is T_1 ;
Thus one has $T = T_0 + T_1$ and the shoot-through duty ratio, $D = T_0 / T_1$.

During the interval of the non-shoot-through states, T_1

$$V_{L1} = V_{in} – V_{C1},$$
$$V_{L2} = -V_{C2} \quad (1)$$

During the interval of the shoot-through states, *T*0,

$$V_{L1} = V_{C2} + V_{in},$$
$$V_{L2} = V_{C1} \quad (2)$$

$$V_{PN} = 0,$$
$$V_{diode} = V_{C1} + V_{C2} \quad (3)$$

At steady state, the average voltage of the inductors over one switching
cycle is zero.

$V_{PN} = V_{C1} – V_{L2} = V_{C1} + V_{C2}$,
Vdiode = 0

Seven Level Cascaded H-Bridge Quasi Z Source Inverter: The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The multilevel inverter using the cascaded converters with separate DC sources is discussed here [12]. The cascaded multilevel inverter synthesizes a desired voltage from several independent sources of DC voltages which may be

obtained from batteries, fuel cells or solar cells. This configuration has recently become very popular in high-power AC supplies and adjustable-speed drive applications. This converter can avoid extra clamping diodes or voltage-balancing capacitors.

Each single DC sources is associated with a single H-bridge converter. The AC terminal voltages of different level converters are connected in series. Through different combinations of the four switches, S1-S4, each converter level can generate three different voltage outputs,+Vdc, -Vdc and zero [13]. The AC outputs of different full-bridge converters in the same phase are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs. The number of output waveform is the sum of the individual converter Outputs. In this topology, the number of output-phase voltage levels is defined by

m=2N+1,

where N is the number of DC sources.

A seven level cascaded converter consists of three DC sources and three full bridge converters. Minimum harmonic distortion can be obtained by controlling the conduction angles at different converter levels.By switching the MOSFETS at the appropriate firing angles, we can obtain the seven level output voltage. MOSFET is preferred because of its fast switching nature. The switching angles can be chosen in such a way that the total harmonic distortion is minimized [3]. One of the advantages of this type of Seven level inverter is that it needs less number of components comparative to the Diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that of the two types.

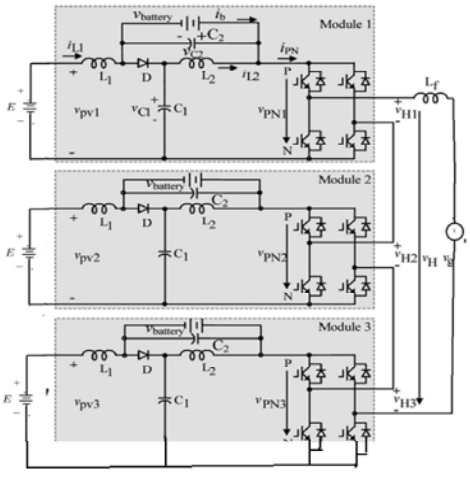


Fig. 4: Circuit Diagram

The inverter has a 12 switches. It will generate the seven different level output voltage. These are,

- +3vdc Mode: S1, S4, S5, S8, S9, S12
- +2vdc Mode: S1, S4, S5, S8, S9, S11
- +1vdc Mode: S1, S4, S6, S8, S9, S11
- 0vdc Mode: S1, S3, S6, S8, S9, S11
- -1vdc Mode: S2, S3, S6, S7, S9, S12
- -2vdc Mode: S2, S3, S6, S7, S10, S12

Table 1: Switching Scheme Of Seven Level Of Cascaded Quasi Z Source Inverter

S_1	S_2	S_3	S_4	S_5	S_6	S_1'	S_2'	S_3'	S_4'	S_5'	S_6'	Vab
1	0	0	1	1	0	0	1	1	0	0	1	+3 Vdc
1	0	0	1	1	0	0	1	1	0	1	0	+2 Vdc
1	0	0	1	0	1	0	1	1	0	1	0	+1 Vdc
1	0	1	0	0	1	0	1	1	0	1	0	0
0	1	1	0	0	1	1	0	1	0	0	1	-1V dc
0	1	1	0	0	1	1	0	0	1	0	1	-2V dc
0	1	1	0	0	1	1	0	0	1	1	0	-3V dc

Fuzzy Logic Controller: Fuzzy logic control uses non-mathematical decision based algorithms that use operator's experiences. This type of control strategy is well suited for non-linear systems. Fuzzy logic control is developed in this work to obtain desired output voltage of the chosen multi-level inverter. In order to obtain the fuzzy control surface for non-linear, time varying and complex dynamic systems, there are a number of steps to be followed as discussed below. The block diagram of fuzzy logic control scheme developed for the chosen single phase seven level inverter is shown in Fig. The FLC is divided into five modules: fuzzifier, database, rule base, decision maker and defuzzifier. The computational structure of fuzzy logic control scheme is composed of the following.

Identification of Inputs and Outputs: The inputs to the FLC are the error $e= V_{ref} - V_o$ and change in error $\Delta_e = e_n - e_n\text{-}1$ where V_n is the actual output voltage of the MLI, V_{ref} is the desired output voltage and subscript n denotes sampling instances. Δm_n is the change of modulation index inferred by the FLC at the nth sampling instant. Using Δm_n, the updated modulating signal ms is obtained and fed to the PWM generator which provides appropriate PWM signals m_n.

Fuzzification of Inputs: The crisp input values of e and Δe are to be fuzzified and seven triangular membership functions are chosen in this work for simplicity.

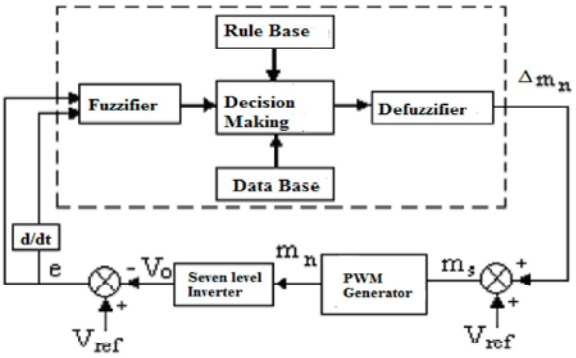


Fig. 5: Fuzzy logic control scheme for Quasi Z-source seven level cascaded h-bridge inverter.

Rule Table and Inference Mechanism: The fuzzy rules are in the form of

R i: If e is A_i and Δe is Bi then Δmn is Ci

Where Ai, Bi and Ci are fuzzy subsets in their universe of discourse. Each universe of discourse is divided into seven fuzzy subsets namely PB (Positive Big), PM(Positive Medium), PS(Positive Small), ZE (Zero), NS(Negative Small), NM(Negative Medium), NB(Negative Big) as in Fig's. The values of e and Δe are normalised to [1,-1] as in Fig and values of Δmn have the range [-1,1] as in Fig. For any combination of e and Δe, a maximum of four rules are adopted.

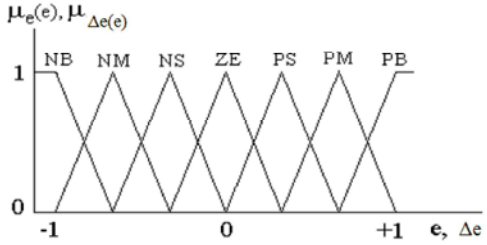


Fig. 6: Membership functions for e and Δe.

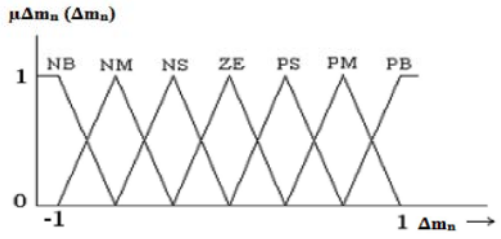


Fig. 7: Membership functions for change in modulation index.

The derivation of fuzzy control rules are heuristic in nature and is based on the following criteria:

- When the output of the seven level inverter deviates far from reference, the change of modulation index must be large so as to bring the output to the reference quickly.
- When the output of the seven level inverter is approaching the reference, a small change of modulation index is necessary.
- When the output of the seven level inverter is near the reference and is approaching it rapidly, the modulation index must be kept constant so as to prevent further deviation.
- When the reference is reached and the output is still changing, the modulation index must be changed a little bit to prevent the output from moving away.
- When the reference is reached and the output is steady, the modulation index remains unchanged.
- When the output is larger than the reference, the sign of the modulation index must be negative and vice versa.According to these criteria, a rule base is derived as in Table

Table 2: Rule base

e/Δe	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

The inference result of each rule consists of two parts, the weighting factor wi of the individual rule and the degree of change of modulation index Ci according to the rule and it is written as

Zi = min {μe(e), μΔe(Δe)} Ci = wi Ci.

Where zi denotes the change in modulation index inferred by the ith rule and Ci is looked up from the rule table which shows the mapping from the product space of e and Δe to Ci.

Defuzzification: The defuzzification is carried out using the bisector of area method.

Analysis of Seven Level Cascaded H-Bridge Quasi Z Source Inverter Using Fuzzy Logic Controller: The seven level output voltage and current is simulated using MATLAB/SIMULINK software.

The simulink model consists of a pulse generation block, cascaded h-bridge quasi z source inverter block. The pulses are given to the inverter to obtain a seven level output voltage [14].

The function of a PWM generation block is a combination of a multicarrier PWM signal and sinusoidal PWM signal to produce a three pulse signal [15]. This pulses are given to the cascaded h-bridge inverter

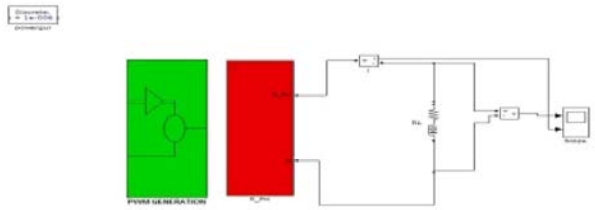


Fig. 8: Simulink model of cascaded h-bridge quasi z source inverter

The seven level output voltage and current is simulated using MATLAB SIMULINK software. The RL load is used. The parameter of the Resistance is 100 ohms and inductance is 50mH. The output of seven level voltage to drive the load and to reduce the total harmonic distortion.

Model of Cascaded H-bridge Quasi Z Source Inverter Using Fuzzy Logic Controller:

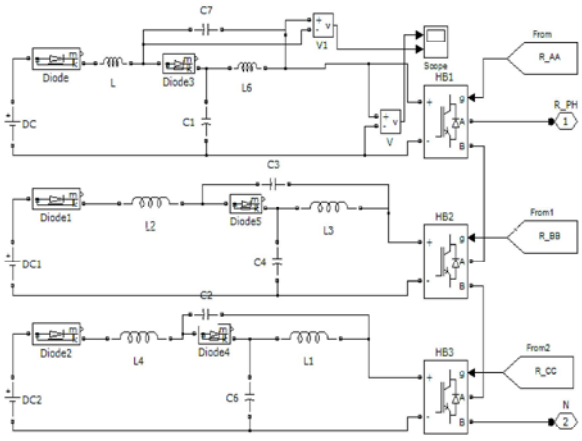


Fig. 9: Simulink model of Quasi Z-source cascaded h-bridge inverter

The multi carrier PWM signal and sinusoidal reference signal are combined to generate a three pulses signal. These signal are used to generate the seven level output voltage [13].

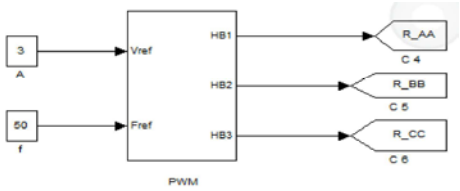


Fig. 10: Model Of PWM Pluses Generation

Inductor Output Current: The inductor initially stores the energy so the initial current is high. Then the inductor current is finally maintained with 5Amps. Fig.6.4 shows the output of inductor current (A) Vs time(sec). The inductor value is used to achieve the shoot through state

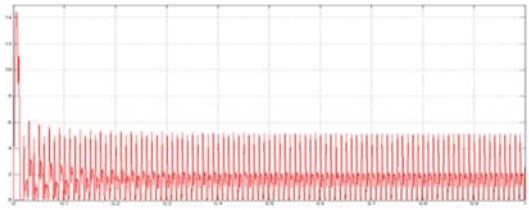
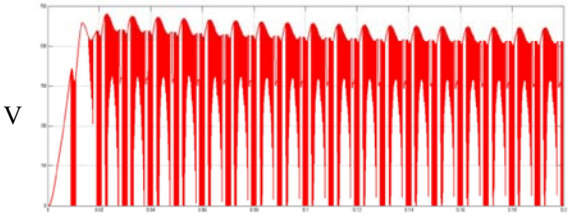


Fig. 11: Inductor current output waveform.

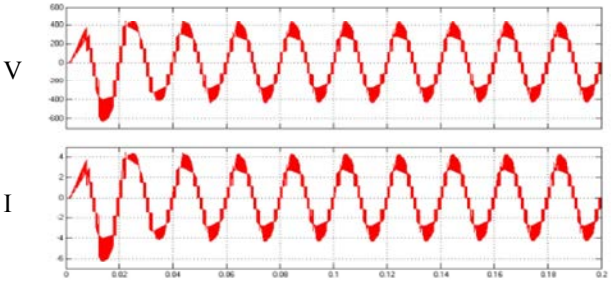
DC Link Voltage: The pulses are given to the cascaded H bridge inverter and produce a seven level output voltage. When the shoot through state is achieved the dc link voltage is boosted that is, the output voltage is greater than the input voltage.



Time (seconds)

Fig. 12: dc link voltage

SEVEN LEVEL OUTPUT VOLTAGE



Time(seconds)

Fig. 13: Output voltage and current.

FFT Analysis: Figure (14) shows the Fast fourier analysis of the seven level output voltage.

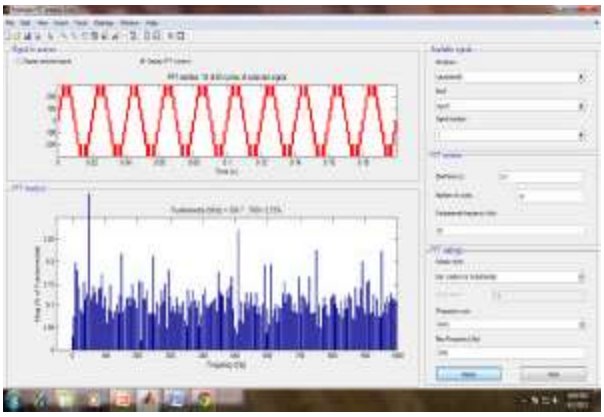


Fig. 14: FFT analysis of seven level output voltage.

The fast fourier transform is used to calculate a total harmonic distortion. The THD level alsoreduces to get a near sinusoidal output waveform. To increase the number of level to reduce the total harmonic distortion.

CONCLUSION

In this research work, MCPWM strategy based quasi Z source seven level cascaded h-bridge inverter have been presented. Quasi Z source multilevel inverter gives higher output voltage through its quasi Z source network.The proposed system is a combination of QZSI and CHB multilevel topology using Fuzzy Logic Controller.This paper presents the THD of 7 level single phase cascaded H bridge multilevel inverter. The results show that as the number of levels increases the THD reduced in single phase inverter. The simulation results show the effectiveness of the proposed QZSCMI.Various PWM control techniques like Phase shifting and Phase disposition were discussed in this paper. Using this Phase shifting technique, high quality output with less THD by cascading the inverter and output of the waveform was analyzed in the MATLAB/simulink through FFT and real time implementation. THD analysis and distortion factor have been estimated.

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