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Multilevel Inverter with Reduced Number of Switches and Reduction of Harmonics

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Abstract: This paper presents a new type of multilevel inverter obtained by cascading two H-bridge inverters using the asymmetric dc voltage sources in the ratio of 1:2.The new inverter can operate as a seven level multi-level inverter providing asymmetrical dc voltage sources. The proposed cascaded H-bridge multilevel inverter (CHBMLI) using asymmetric voltage sources comprises of eight switches. As per the conventional topology where symmetric voltage sources are being used consist of twelve switches. The main objective of the proposed topology is to increase the number of levels with reduced number of switches thereby reducing the harmonic content at the output side by using Sine Property (SP).

Key words: Multilevel Inverter · Cascaded multilevel inverter · Asymmetric sources · Sine Property

INTRODUCTION

HE inverter is an electronic circuit that operates from a dc current source or a dc voltage source and converts it into ac current or voltage sources. Multilevel inverter and inverters do the same function, the main difference between MLI and inverter is capable of producing staircase output form which is nearly equal to sinusoidal. The multilevel inverter is becoming influential in industrial and domestic application mainly because of its ability to generate the output with extremely low distortion, which can reduce the dv/dt stresses therefore electromagnetic compatibility problem, can be reduced. [1-3]. The multilevel inverters can be classified into three types:- Diode-clamped multilevel inverter [1], flying-capacitors [2] and cascaded multilevel inverter [3].

A diode-clamped multilevel (m-level) inverter (DCMLI) consists of (m-1) capacitors on the dc bus and produces m levels in the phase voltage. Some of the features are as follows:

- High-voltage rating for blocking diodes.
- Unbalanced capacitor voltage.
- Unequal switching device rating.

In flying-capacitors, the order is numbered differently from that of the diode-clamped inverter, but the voltage level for the flying capacitors converter is similar to that of the diode-clamped converter. This also contains some characteristics as:

- Balancing capacitor voltages.
- Large number of capacitors.

A cascaded-multilevel inverter consists of a series of H-bridge inverter units[4]. This multilevel inverter has a function to synthesize a desired voltage from several separate dc sources (SDCSs), which may be obtained from fuel cells, batteries or solar cells. It has some characteristics:

- For power conversions from ac to dc or vice-versa, the cascaded inverters need separate dc sources[5]. It is well suited for various renewable energy sources such as fuel cells, photovoltaic and biomass.
- Dc sources can be connected between two converters in a back-to-back fashion is not possible because a short circuit can be introduced [1].

The cascaded topologies are classified into two groups: symmetric cascaded multilevel inverter and asymmetric cascaded multilevel inverter[6]. The asymmetric CMLI generate a higher number of output levels in comparison with symmetric CMLI because of different amplitude of its dc voltage source.

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Asymmetric voltage methodology is performed in the cascaded H-bridge multilevel inverter to increase no of output voltage levels[7]. With the use of cascaded H-bridge MLI, voltage levels can be increased. The main merit of cascaded multilevel inverter is standard layout and packaging. Out of this, it takes less time for manufacturing process and at a low cost[8]. The demerit of this is that it requires an individual dc source for each H-bridge and it involves high number of power switches. Most of the properties of cascaded inverters are allowed to use Sine Property (SP) strategies to control the inverters perfectly.

Configuration of Proposed Converter: The proposed converter has two cascaded H-bridge multilevel inverter with asymmetric sources. It produces output of 7-level and consists of eight switches in the ratio of 1:2. It utilizes two asymmetric dc voltage sources for generating 7-levels. Dc voltage sources have been arranged in the pattern of n, 2n etc where n represents the lowest dc voltage source magnitude. This circuit has eight switches with additional H-bridges like H_1, H_2 which is used to form both positive and negative sequence[9]. Here, two H-bridge inverters with a dc voltage source are connected in series to produce a single-phase 7-level inverter having eight semiconductors switches whereas in case of a conventional symmetric group, the cascaded H-bridges have similar magnitudes of the dc sources which has twelve switches of equal dc voltage sources. By doing so, more number of output voltage levels can be generated with the use of lesser number of power electronic switches but in symmetric cascaded H- Bridge MLI the number of power switches increase as the number of level increases and simultaneously to reduce the harmonic contents at the output voltage side by using the Sine Property.

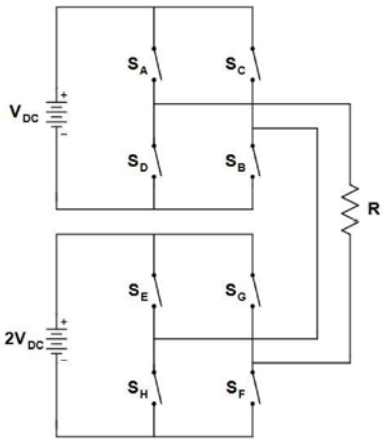

Fig. 1: Proposed single phase 7- level multilevel inverter

In this section, in order to analyze the merits and demerits of the proposed topology and to compare it with the conventional cascaded multilevel inverter with symmetric dc voltage sources, two H -bridges have been used connected in a cascaded form in the ratio of 1:2 which are of 15V and 30V dc voltage sources respectively with eight switches as represented in Figure1.

Single H-Bridge Inverter: In a simple H-bridge inverter, each H-bridge has four semiconductor switches and the four cells can provide output voltage of either positive or negative polarity or it can also be used for zero volt due to the switching pattern of switch performance as shown in Fig. 2. The lowest number of voltage levels for a multilevel inverter by the use of cascaded configuration is three-level. As a full bridge inverter is required to get a waveform of 3-level and basically full-bridge inverter also referred to as H-bridge cell helps in representing how the switches turn ON and OFF according to the switching voltages of a single H-bridge is shown in Table 1. According to single H-bridge, four switching operations are carried out which has three output switch levels i.e. +V,-V and zero that can be considered for voltages across the load. During the inverter operation the switches S_A and S_D are turned off at the same interval so as to provide the positive voltage V_{AB} as well as the path of current and similarly S_B and S_D are turned on to provide the negative V_{AB} with current as in Fig. 3. When all switches are OFF, the current flows through the freewheeling diodes. Two approaches are considered for obtaining zero

level: Case (1) S_A, S_B-ON; S_C, S_D-OFF Case (2) S_A, S_B-OFF; S_C, S_D -ON. To operate at zero level either of the two cases can be considered simultaneously.

Table 1: Output Voltage Values for H-bridge

Switching	SA	SB	SC	SD
Voltage				
0	1	1	0	0
VDC	1	0	0	1
0	0	0	1	1
0	0	0	1	1
$-V_{DC}$	0	1	1	0
0	1	1	0	0

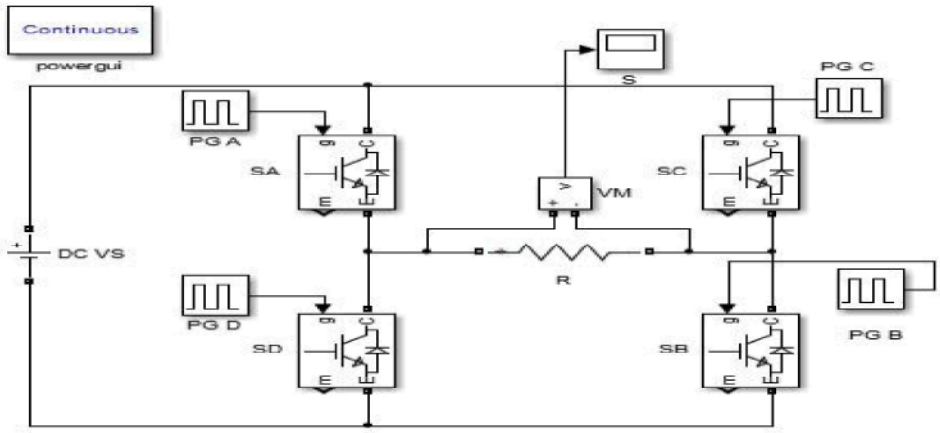

Fig. 2: MATLAB circuit of H-Bridge inverter

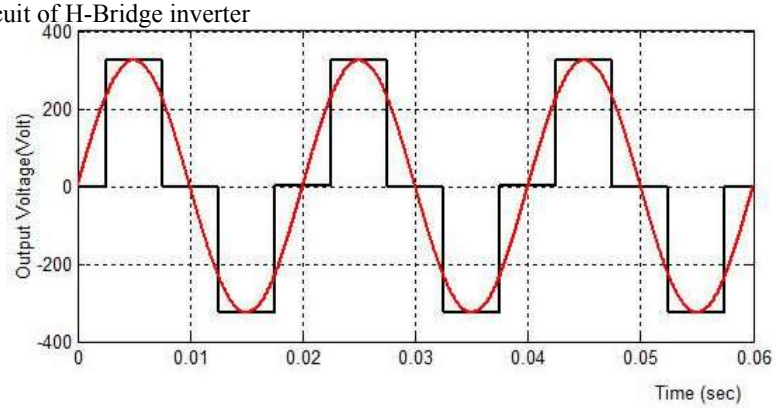

Fig. 3: Simulated waveform for H-bridge inverter

As per Fig. 4, the proposed 7-level cascaded multilevel inverter having eight switches of two H-bridges connected in series with the asymmetric dc voltage sources of ratios 1:2 i.e. 15:30 volts. With help of this converter, we can increase the no. of levels by the use of lesser no. of switches as compared to the conventional topology which requires 12 switches for generating the same no. of levels using symmetric dc voltage sources[10]. The proposed converter does not completely eliminate the harmonic contents in the output. To overcome this, the Sine Property has been used in the same multilevel inverter to reduce the unwanted harmonic components from the output as per the table shown below

According to the switching voltage, all the eight switches will be turned ON and OFF. For the Zero level S_A, S_C, S_E and S_G are turned on or else turning OFF. Likewise all the levels will be performed up to zero level voltage as shown in Table 2.

Table 2: Switching Values for Proposed 7-Level Cascaded H-Bridge

Switching Voltage	S_A	S_B	S_C	S_D	S_E	S_F	S_G	S_H
0	1	0	1	0	1	0	1	0
1	1	1	0	0	1	0	1	0
2	1	0	1	0	1	1	0	0
3	1	1	0	0	1	1	0	0
2	1	0	1	0	1	1	0	0
1	1	1	0	0	1	0	1	0
0	1	0	1	0	1	0	1	0
0	0	1	0	1	0	1	0	1
-1	0	0	1	1	0	1	0	1
-2	0	1	0	1	0	0	1	1
-3	0	0	1	1	0	0	1	1
-2	0	1	0	1	0	0	1	1
-1	0	0	1	1	0	1	0	1
0	0	1	0	1	0	1	0	1

Operation of Chbmli According to the Switching Voltages: In this converter, the switching of voltage sequence is less demanding over its counter parts. As stated by its inherent advantages, it does have produce negative pulses for negative cycle control because of H-bridge inverter. Thus, there will be no additional task for regulating the negative voltage. Although the full bridge performs this condition and the required level is generated by the high-switching-frequency part of the inverter[11]. Then, this level may be translated according to the certain condition whether it will be negative or positive as necessity of the required output voltages. As already discussed the cascaded configurations are comprises of 2 parts: Symmetric and Asymmetric DC sources. As per the Table III, it can be observed that the implementation of symmetric sources on a CHBMLI the higher number of power switches such as 12, 16 and 20 switches have been used for the different levels as mentioned in the table, whereas the number of switches is reduced to achieved the same number of levels.

Table 3: Different Switching Voltages of Different Levels

Level	Symmetric Dc Voltage Source	Asymmetric dc Voltage Source
7-Level	12 Switches	8 Switches
9-Level	16 Switches	8 Switches
11-Level	20 Switches	12 Switches

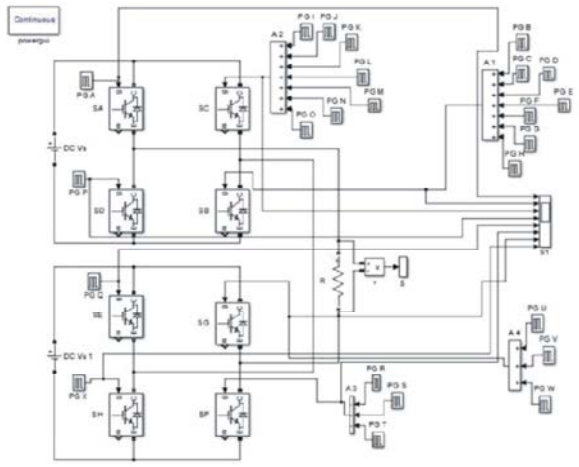

Fig. 4: MATLAB circuit for 7-Level Cascaded H-Bridge Multilevel Inverter

In the above Figure 5 there are two H-bridges which are connected in series arrangement and each H-bridge contain four power switches having an asymmetric DC voltage source of 1:2 ratios. From the Figure 6 and 7 it can

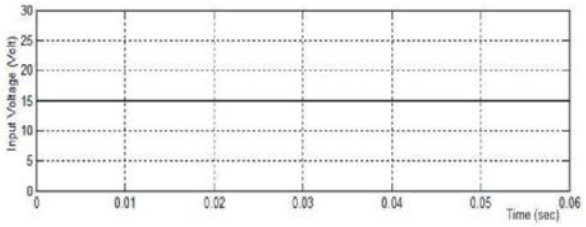

Fig. 5: Simulated Waveform of Input Voltage for H1 Bridge

observe the input voltage and input current of the single H1-bridge.The voltage of 15V can be observed in the input of the voltage and the corresponding current can be observed as 0.0453 A.

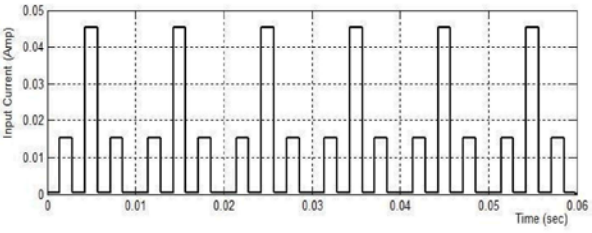

Fig. 6: Simulated waveform of input current for H1 Bridge

In the above Figure 5 there are two H-bridges which are connected in series arrangement and each H-bridge contain four power switches. As shown in Figure 6 here, the input voltage for H1- bridge is given as 15 V it is in a form of 1:2 ratios Likewise, for the H2-Bridge the values of input voltage, current and power are as follows

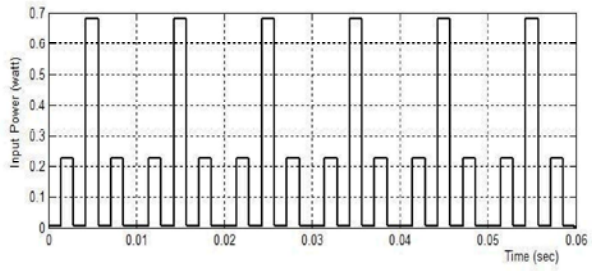

Fig. 7: Simulated waveform of input power for H1 Bridge

As referred to Figures 5, 6 and 7 are waveforms of input voltage, current and power for H1 Bridge. The values are like15 V, 0.047 and 0.69.

Figure 8, 9 and 10, shows the input voltage, current and power of the inverter for H2-bridge. The values of input voltage, current and power are 30V, 0.0456 A and 1.367 W respectively.

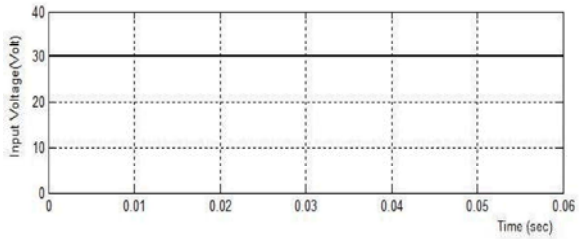

Fig. 8: Simulated waveform of input voltage for H2 Bridge

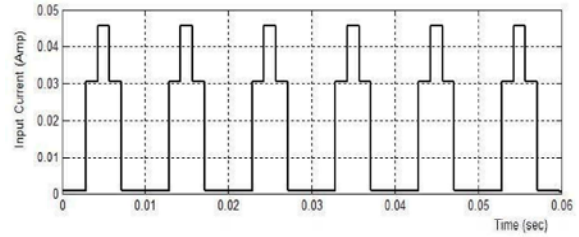

Fig. 9: Simulated waveform of input current for H2 Bridge

At last it can conclude that the designed scheme of CHBMLI, if these two H-bridges are being connected in series arrangement then 7-Levels CHBMLI has been formed.

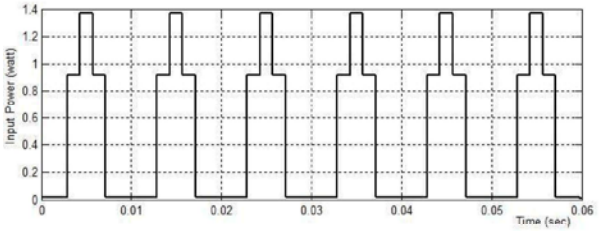

Fig. 10: Simulated waveform of input power for H2 Bridge

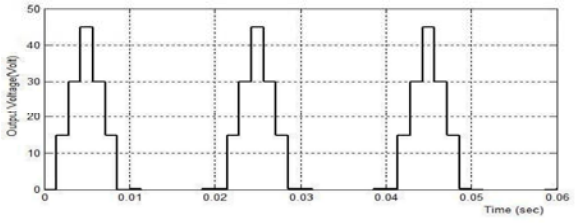

Fig. 11: Simulation Output Voltage Waveform for 7-Level Cascaded H-bridge Multilevel Inverter

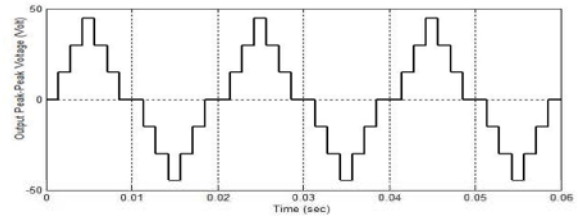

Fig. 12: Simulation Output Peak-Peak Voltage Waveform for 7-Level Cascaded H-bridge Multilevel Inverter

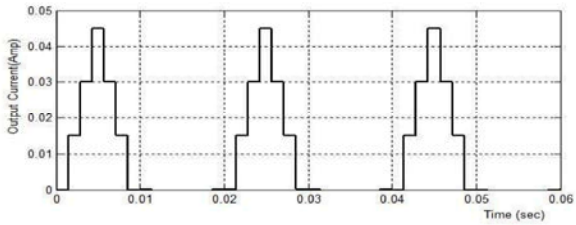

Fig. 13: Simulation Output Current Waveform for 7- Level Cascaded H-bridge Multilevel Inverter

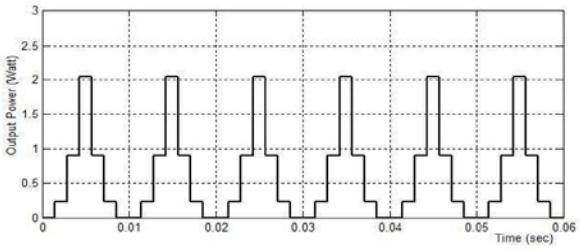

Fig. 14: Simulation Output Power Waveform for 7-Level Cascaded H-bridge Multilevel Inverter

Likewise, for both the H1 and H2-bridges the values of input voltage, current and power are exactly same in case of Sine Property. But only the difference is the waveform of output voltage it is resemblance like Sinusoidal form so ultimately it reduces harmonic contents.

Sine Property and its Calculation: The switching angles are a factor for deciding the performance of the MLI. It can be rectified by using any optimization methods such as Genetic algorithm, Resultant theory and Newton Rapson method but with the use of these methods we go through under more mathematical calculation regardless to go to the Property of the sinusoidal wave to allow proper switching angles so that its leads to resemblance output waveforms to sinusoidal waveforms. These angles for M level inverter can be obtained by,

Sin β (

Where p= 1, 2……n and m= (M-1)/2

- m is calculated by using the formula, m= (No. of levels-1)/2
- Desired Firing angle (in terms of degree):

Sin β (1) =0.5/m, Sin β (2) =1.5/m, Sin β (3) =2.5/m, Sin β (4) =3.5/m, up to required no. of angles.

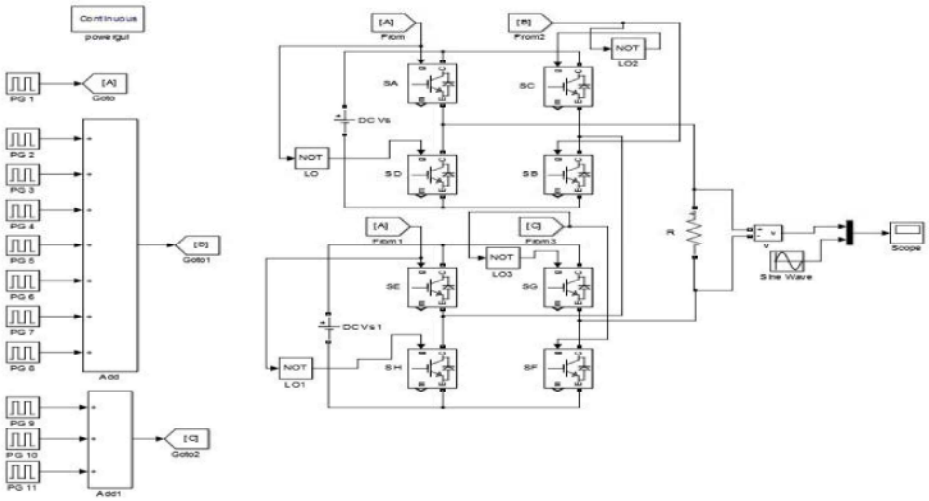

Fig. 15: MATLAB circuit for 7-Level Cascaded H- Bridge Multilevel Inverter by using Sine Property

This model is designed for the same input voltage as being used in above model and output voltage is also same i.e. 45 V. But the only difference is the waveform gets differ from above topology. In this waveform resembles like a sinusoidal form, it is also reduces harmonics content from output voltage.

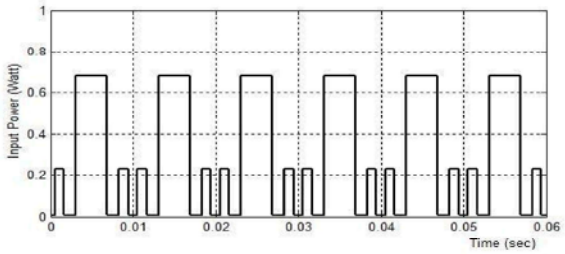

Fig. 16: Simulated Waveform of Input Power for H1 Bridge with use of Sine Property

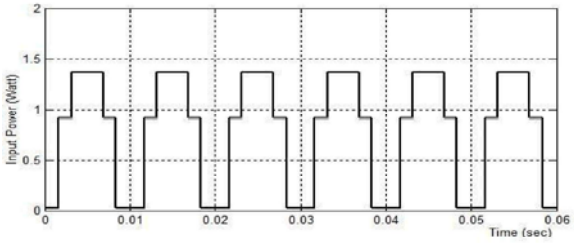

Fig. 17: Simulated Waveform of Input Power for H2 Bridge with the use of Sine-Property

As compared to Figure 12 with Figure 18 the waveform which is obtained by using SP has got less harmonic contents in the outside voltage of CHBMLI.

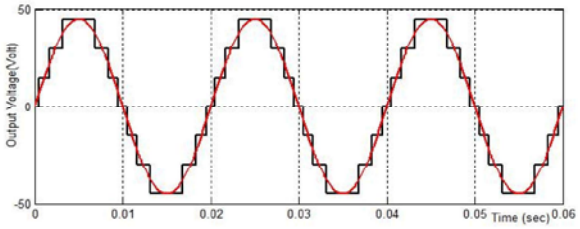

Fig. 18: Simulation Peak-Peak Output Voltage Waveform for 7-Level Cascaded H-bridge Multilevel Inverter using Sine Property

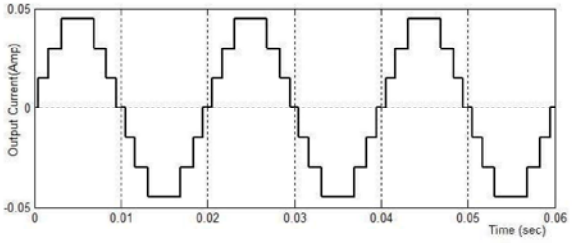

Fig. 19: Simulation Output Current Waveform for 7-Level Cascaded H-bridge Multilevel Inverter using Sine Property

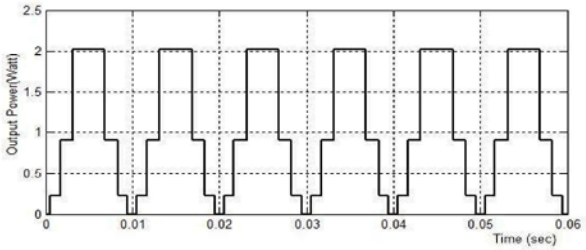

Fig. 20: Simulated Waveform of Output Power with the use of Sine-Property

Comparison of Total Harmonic Distortion with and Without Sine Property in 7-Level Chbmli:

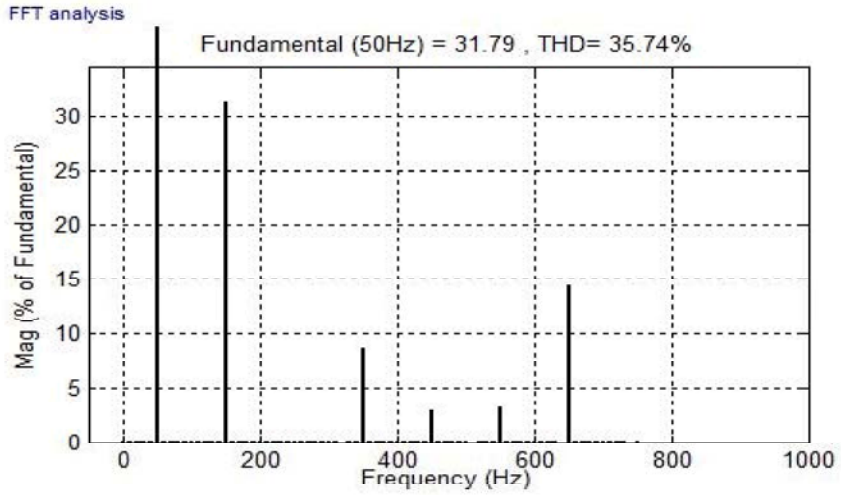

Fig. 21: THD Analysis of 7-Level CHBMLI without SP

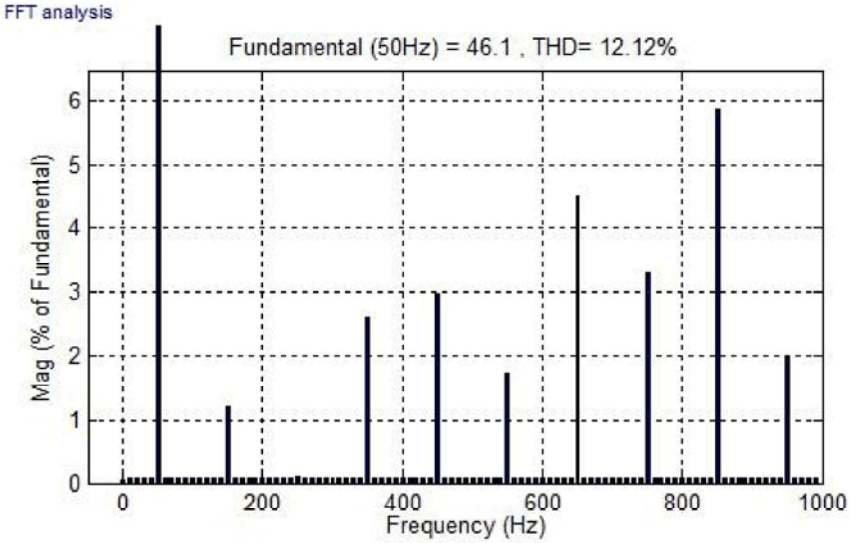

Fig. 22: THD Analysis of 7-Level CHBMLI with SP (Sine Property)

The analytical results have shown in Figure 8 and Figure 9 by which the THD of 7-Level CHBMLI without and with using Sine Property is compared. Here the THD is around 35.74% in 7-Level whereas by the use of SP it is about 12.12%. In our analysis for the same level, the THD content can be minimized up to 12.12% from 35.74%.

CONCLUSION

A new multilevel inverter topology is studied which uses less number of switches than the conventional inverter topology and hence the possibility of producing higher number of level with same switches as in conventional topologies is made. The harmonic content is reduced by using a new Sine Property, which basically changes the step angle of each level so as to resemble to the sine waveform. The switching sequence multilevel inverter is designed to generate 7-Levels. The simulation for multilevel inverter with Asymmetric DC voltage sources is performed using MATLAB. The MATLAB Model is developed for the generation of switching pulses using Sine Property. Proposed Multilevel Inverter is simulated with and without Sine Property. The results are compared and proved that with the proposed topology; the harmonic content is reduced by Sine Property.

Problem causing for performing and overcome of it: The hardware was performed for a 7-level MLI. The pulses have been generated for this level. In the 7-Level Multilevel inverter on giving low level input voltage of ratio 1:2 up to 4V:8V in an inverter, we are getting a 7-staircase output but while increasing further voltage i.e. 15V & 30V,driver supply was tripped off. Therefore this problem occurs due to common grounding between driver circuit and power circuit. It has been rectified and successfully achieved output.

FFT Analysis: The results are shown in Fig. 21 and Fig. 22 by which the THD of 7-Level CHBMLI without and with using Sine Property is compared. The THD is around 35.74% in 7-Level whereas by the use of SP it is about 12.12%. In our analysis for the same level, the THD content can be minimized up to 12.12% from 35.74%.

Table 4: Comparison of THD level (%)

Inverter Configuration	THD Level (%)
7-Level CHBMLI without SP	34 %
7-Level CHBMLI with SP	15.7 %

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