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Analysis of Fhss Receiver Using BPSK Demodualtion in VHDL

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Abstract: To increase the resistance against interference, jamming and security FH/BPSK (Frequency Hopping Spread Spectrum/ Binary Phase Shift Keying) is widely used. It combines the advantage of BPSK and FHSS in a single logic. The paper dealswith generation of analog carrier and the simulation of the entire system. The entire system is coded in VHDL and simulated and verified using Xilinx and Matlab software. The simulation result shows that the FH/BPSK is efficient interms of resource usage in Field Programmable Gate Array (FPGA). The estimated power in FPGA is efficient for this system and it is of 113 mW.

Key words: FHSS · BPSK · FH/MPSK receiver · VHDL · FPGA

INTRODUCTION

Wireless communications have been in development for several years to be used in a variety of applications from radio to bluetooth. As technology progress, recent researches are converging every processing component on a single chip solution. This enables to fabricate limitless number of application on a single chip.In wireless communication, security is a major concern, since the signal can be easily tapped. The security aspect is assured by the use of Code Division Multiple Access (CDMA). CDMA employs Spread Spectrum (SS) technique. In SS, the data is transmitted in slightly wider bandwidth rather than available frequency band. The spreading of data over a frequency spectrum makes the signal resistant towards interference [1], [2], jamming [3], eavesdropping, provide security and reduces the transmitted power spectral density. In order to discriminate the signal in the frequency band, SS use randomly generated code signal called spread code. Spread Spectrum has two popular techniques that are Direct Sequence Spread Spectrum (DSSS) and Frequency Hopping Spreading Spectrum (FHSS).DSSS can transmit the data in the form of digital itself. DS-CDMA (Code Division Mulitple Acess) transmitter and receiver implementation is carried for the digital data. FPGA implementation of such DSSS system makes the trasnceiver efficienct in terms of area utilization [4], ASIC implementations [5] and high data rate [6]. Frequency hopping was first used by the German militaryin an attempt to prevent the eavesdropping of the transmitted data and to suppress interference [7]. In FHSS, the information is spread over a frequency spectrum with the help of pseudo random number and different carrier frequencies. The pseudorandom code is known at thetransmitter and receiver to de-spread the received signal to extract the original bit sequence.FH/BPSK signal is identified to reduce attenuation and interference. Attenuation of the signal is greatly reduced with the help of carrying the data over a high frequency. It is addressed in this paper by Binary Phase Shift Keying (BPSK). BPSK is employed, due to the advantage that the digital modulation is less complex and can be efficiently transmit over a longer distance without fading.BPSK implementationin VHDL is complex due to the analog signal creation. The solution to the problem is addressed by IP CORDIC [8], [9] and Direct Digital Frequency Synthesizer (DDFS) [10]. Once the carrier signal is generated, multiplexer logic for implementing BPSK modulation in VHDL [11] is used to vary the phase of the carrier signal according to the binary data. At receiver coherent BPSK detection [12] is employed to extract the bit sequence in VHDL. The paper is organized into five sections. Section II briefly describes the general theory of FHSS de-spreader, BPSK demodulator and FH/BPSK receiver respectively. Section IIIpresents architecture and

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design of the system. Section IV deals with the simulation results to verify the waveforms and compares measured results. Finally, Section V concludes the section.

Theory of FH/BPSK Receiver

Frequency Hopping Spread Spectrum: In DS, the use of PN sequence to spread a signal succeeds instantaneous spreading of the transmission bandwidth. To handle the effect of jammers, processing gain (*PG*) is determined, which depends on the PN sequence length.

$$PG = W_c / R_b \quad (1)$$

where W_c and R_b are baseband parameter of DSSS. W_c is the bandwidth of the PN sequence and R_b is the bit rate. When *PG* is made larger, it permits a larger transmission bandwidth with more chips per bit. *PG* not still large to overcome the effect of interference and forces another method, FHSS to overcome the jamming effect. In FHSS, spreading occur sequentially rather than instantaneously. The carrier signal hops randomly from one frequency to another in a pseudo random ordered sequence of hops is termed as "sequential" in FHSS.

Binary Phase Shift Keying: BPSK modulation is used to transmit the digital bits '0' and '1' over a bandpass channel. The digital data may be used in several applications like digital computer outputs or PCM waves generated by digitizing voice or video signals which can be send through the bandpass channel. In coherent BPSK system, pair of signals used to represent the symbols of '0' and '1'. The message point in BPSK is located at the two regions. In demodulation, for making a decision in favor of message point at symbol '0' or '1' detection rule is obtained. This makes the detection process less complex. The modulation makes the signal efficient interms of the channel bandwidth and transmitted power.

FH/BPSK Receiver: In order to use the advantage of both FHSS and BPSK, FH/BPSK is combined. FHSS is more resistant towards interference and jamming and provide security with the help of spread code. Also the FHSS makes the signal to be deliberately spread over a wide spectrum by hopping among different carrier frequencies. The BPSK signal can achieve the goals like maximum data rate, minimum transmitted power and minimum channel bandwidth. FH/BPSK signal combines the advantage of both the system into a single system and attain the greater efficiency interms of power.

Architecture of FH/BPSK Receiver: In FH/BPSK receiver, the input to the system is spreaded signal. FH/BPSK Receiver architecture is shown in Figure 1. The block describes the entire FH/BPSK system of the FHSS de-spreading and demodulating the received signal to extract the original bit. The FHSS receiver architecture is divided into four stages. The first stage will receive the spreaded signal and makes synchronization with the clock signal. The next stage is to process the received signal with the spreading frequency to despread the spreaded signal. Then Coherent BPSK denodulation (digital demodulaion) is carried out for the FHSS despreaded signal with the help of carrier signal. Finally, impulse detector is used to match exactly with the demodulated signal to extract the original bit.

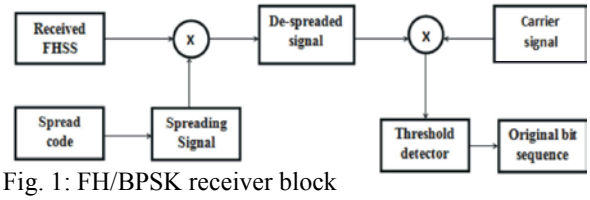

Fig. 1: FH/BPSK receiver block

FHSS De-Spreading in VHDL: FH/BPSK receiver is carried to extract the original bit from the received signal (spreaded signal). The process of FHSS de-spreading is shown in Figure 1. In this, FHSS carrier signal is produced by means of frequency synthesizer. Frequency synthesizer generates carrier signal with different frequencies. These carrier frequencies hopped by means of spread code to achieve a spreading frequency same as that of transmitter. In VHDL, it is carried out with the help of multiplexer. The multiplexer logic is shown in Figure 2. By using spreading frequency, FHSS de-spreading is carried out by multiplying spreaded signal with spreading frequency. FHSS de-spreading logic is shown in Figure 2.

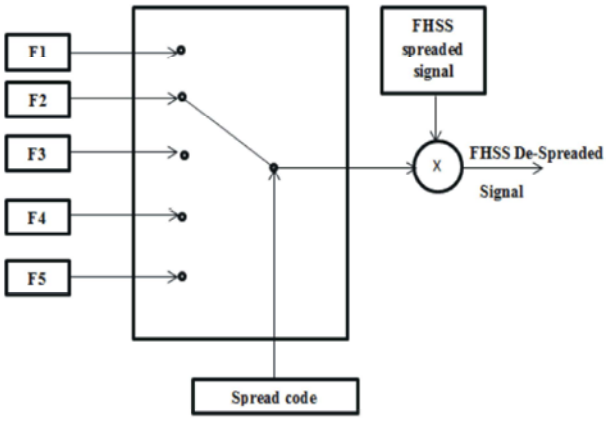

Fig. 2: FHSS de-spreading

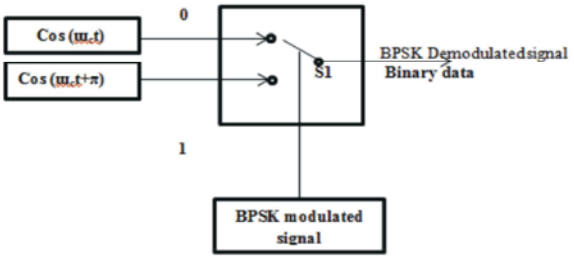

Fig. 3: BPSK demodulation

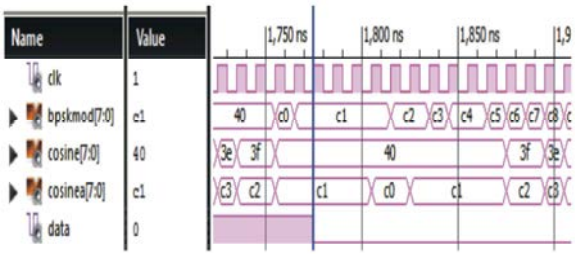

Fig. 4: Simulation of BPSK demodualtion

BPSK Demodulation in VHDL: The BPSK demodulation is a process of translating the band pass to baseband, with recovery of the band limited message waveform. The input to the FH/BPSK demodulation block is the de-spreaded signal. While in BPSK demodulation, one can regain the original bit sequence using multiplexer concept in VHDL is shown in Figure 3.

RESULTS AND DISCUSSION

In VHDL, carrier signal are generated through LUT, which can have 'n' number of sampled values and 'm' number of bit for accuarate respresentation.

Simulation of BPSK Demodulator: Figure 4, presents a coherent BPSK demodualtion in VHDL. This explains the receiver has exact knowledge of the carrier signal's phase. The frequency of the carrier signal is determined by the time period (t_b)of the master clock and 'n'. The carrier signal is represented by 180 number of sampled values and hence the frequency of the carrier signal is 0.55MHz and master clock frequecny is 0.1GHz. With the help of the received signal and carrier signal, the data bits are extracted from the demodulated signal.

Figure 5 shows the BPSK demodulation in VHDL. The received signal is taken from VHDL and plotted. The received signal is a BPSK modulated signal, in which the carrier signal phase is changed according to the data bit is shown in Figure 5(a). In this, the carrier signal is sampled as 180 digitized values, it takes 180 clock cylce to represent a single clock cycle of carrier signal. The carrier signal with the frequency of 0.55MHz is generated shown in Figure 5(b). For coherent detection, the modulator uses a local oscillator that generates a frequency which is exact replica of the carrier signal at the transmitter.Intilally, the carrier signal is inphase with received signal, so the data bit is extracted as '1'. At 720ns the carrier signal is out of phase withreceived signal, hence the data bit is extracted as '0'and it is shown in Figure 5(c).

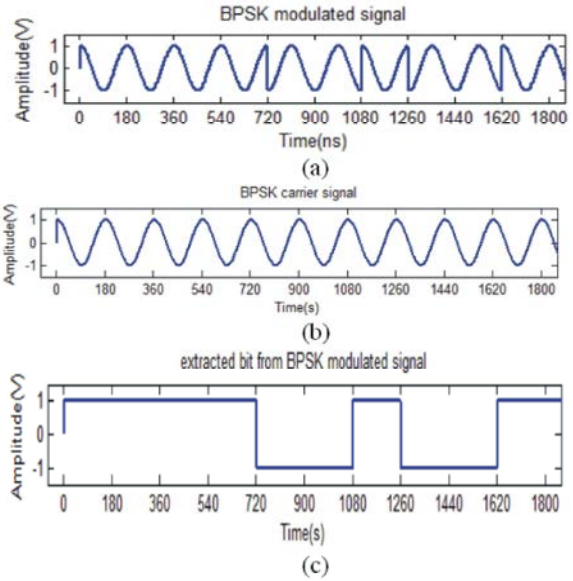

Fig. 5: (a), (b) and (c) Simulation of BPSK demodualtion using matlab

Simulation of FHSS De-Spreader: Figure 6, presents a FHSS de-spreader. The receiver has exact knowledge of the spreading frequency as that of transmitter. The master clock has a frequency of 0.1GHz. The spreading frequency is generated in VHDL with the help of multiplexer with frequency range varies from 0.55MHz to 11.1MHz. The received signal is multipled with spreading frequency to extract the bit sequence and it shown in Figure 6.

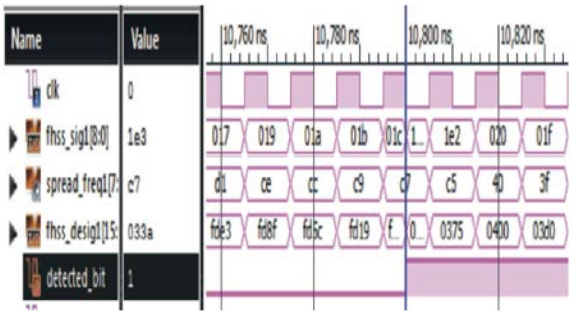

Fig. 6: Simulation of FHSS de-spreader

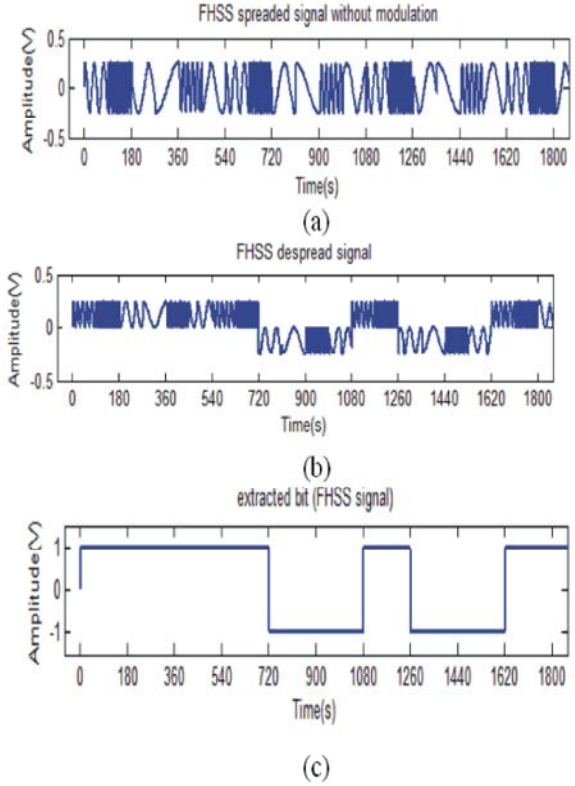

Fig. 7: (a), (b) and (c) Simulation of FHSS de-spreader using matlab

Figure 7 explains the FHSS de-spreading in VHDL. FHSS received signal is shown in Figure 7(a). FHSS de-spreading is performed for the received signal with the help of spreading frequency is shown in Figure 7(b). The de-spreaded signal has low power spectral density, since it is defined as digital words rather than bits. Now matched filter is used to generate the peak impulse singal, to extract the bit sequence at that instant. From the de-spreaded signal data bit is extracted at the presence of impulse signal is shown in Figure 7(c).

Simulation of FH/BPSK Receiver: Figure 8, presents a FH/BPSK receiver. The receiver has exact knowledge of the carrier signal and spreading frequency. The carrier signal and spreading frequency are phase locked with the received signal, which is same as that of the transmitter. The spreading frequency range varies from 0.55MHz to 11.1 MHz. Initially, the received signal is multipled with spreading frequency to de-spread the signal to a narrow band. With the help of the de-spreaded signal and carrier signal, the demodulation is performed and then the data bitis extracted from the demodulated signal.

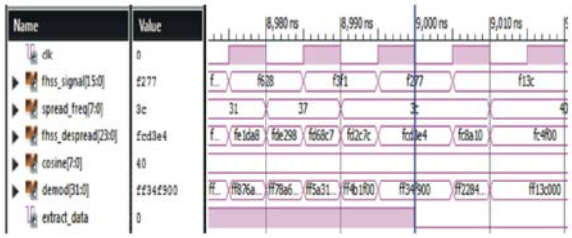

Fig. 8: Simulation of FH/BPSKreceiver

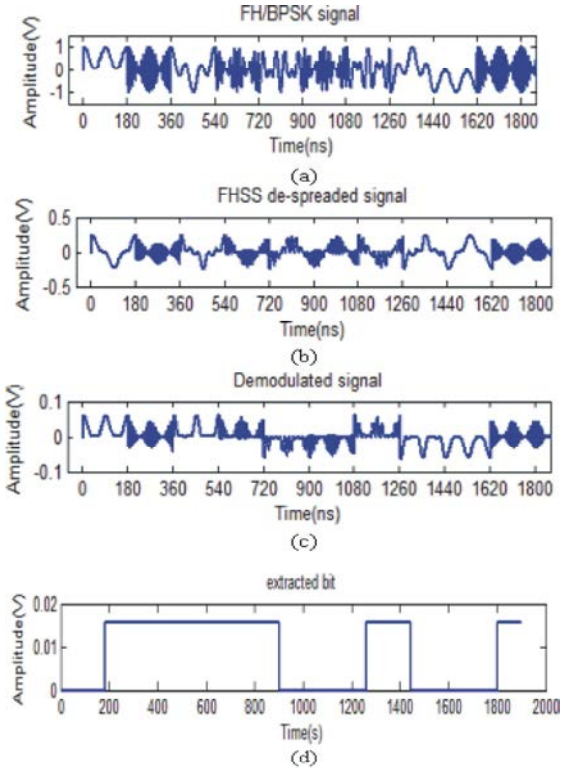

Fig. 9: (a), (b), (c) and (d) Simulation of FH/BPSK receiver

Table 1: FPGA resource usage comparison

Parameter	BPSK	FHSS	FH/BPSK
Memory usage (KB)	41884	41990	42235
CPU usage(ms)	1216	1107	1575
Estimated Power in FPGA (mW)	186	113	113.45

Figure 9 depicts the FH/BPSK receiver in VHDL. FH/BPSK received signal is shown in Figure 9(a). The received signal is multiplied with the spreading frequency to de-spread the signal is shown in Figure 9(b). Now, the despreaded signal is multiplied with the BPSK carrier signal to get the demodulated signal and it is shown in Figure 9(c). From the demodulated signal data bit sequence is extracted at the presence of impulse signalis shown in Figure 9(d).

FH/BPSK signal is compared with the FHSS de-spreaded and BPSK demodulated signal based on the simulation on Spartan 6 XC6SLX150- FGG484 device. Table 1 shows the resource usage comparison, simulated on Spartan 6 family for FHSS, BPSK and FH/BPSK signals. The hardware simulation is more effective for FH/BPSK by attainting the advantage of both FHSS and BPSK in a single system. The power estimation for FH/BPSK is comparativelyhigher than the FHSS and BPSK system.

CONCLUSION

In this paper, it is proposed a FHSS receiver using BPSK demodulation in VHDL. The functionality of the paper was demonstrated though simulations using the Xilinx system edition and Matlab simulation software and its results were discussed. Comparisons between BPSK, FHSS andFH/BPSK have been made on the basis of the resource usage. Among all, the features of FH/BPSK receiver shows optimized interms of estimated power in FPGA on the basis of Table 1.

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REFERENCES

1. Kalita, S. and P.P. Sahu, 2015. “An Anti-jamming Underwater Communication Transceiver model using Uncoordinated Direct Sequence Spread Spectrum Technique,” IEEE International Conference on Electronics and Communication System, pp: 972.
2. Kewu, Huang and Ran Tao, 2010. “Interference Suppression in Spread Spectrum Systems Using the CR-Fractional Fourier Transform,” International Conference on Pervasive Computing, Signal Processing and Applications, pp: 560.
3. Christina Popper, Mario Strasser and Srdjan Capkun, 2010. “Anti-Jamming Broadcast Communication using Uncoordinated Spread Spectrum Techniques” IEEE Journal on Selected Areas in Communications, 28(5): 703.
4. Gaurav P. Channe and C.N. Bhoyar, 2014. “VHDL implementation of DS SS-CDMA Transmitter and receiver for adhoc-network,” IRF International Conference, pp: 100.
5. Vaibhav K. Kakade, 2013. “Implementation of DS CDMA Transmitter and receiver in VHDL for FPGA,” International Journals of Latest Trends of Engineering and Technology, pp: 158.
6. Tasneem S. Mahbub, Salsabil Ahmed and Iqbalur R. Rokon, 2011. “Transmitter implementation using DS-CDMA technique in FPGA using Verilog VHDL,” International conference on Electrical, Electronics and Civil Engineering, pp: 204.
7. Guey-Yun Chang, Jen-Feng Huang and Zheng-Hua Wu, 2014. “A Frequency Hopping Algorithm against Jamming Attacks under Asynchronous Environments, ” IEEE Conference on Ad Hoc and Sensor Networking Symposium, pp: 324.
8. Antonius P. Renardy, Nur Ahmadi, Ashbir A. Fadila, Naufal Shidqi and Trio Adiono, 2015. “FPGA Implementation of CORDIC Algorithms for Sine and Cosine Generator, ” International Conference on Electrical Engineering and Informatics, pp: 1.
9. Parichay Kalra, Anand Kukde and B. Venkataramani, 2014. “CORDIC based BPSK Modulator, ” International Conference on Computer and Communication Technology, pp: 335.
10. Bindiya Kamboj and Rajesh Mehra, 2012. “Efficient FPGA Implementation of Direct Digital Frequency Synthesizer for Software Radios”, International Journal of Computer Applications, 37(10).
11. Erdoğan, C., I. Myderrizi and S. Minaei, 2012. “FPGA Implementation of BASK-BFSK-BPSK Digital Modulators,” IEEE Antennas and Propagation Magazine, 54(2): 262.
12. Faruque Ahamedand Frank A. Scarpino, 2005. “An Educational Digital Communications Project Using FPGAs to Implement a BPSK Detector,” IEEE Transactions on Education, 48(1): 191.