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A Review of Various Carrier Pwm Techniques for Trinary Cascaded Multilevel Inverter

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Abstract: This paper presents a review of various carrier based PWM techniques for trinary cascaded multilevel inverter. The higher switching frequency causes higher losses in the power stack whereas lower the carrier, the more the harmonics and motor losses. This may be necessary for SMPS or VFD. Novelty: A pure sinusoidal waves is obtained among the various carrier based PWM methods by providing appropriate carrier frequency with less switching devices. Practically, a carrier frequency is limited to 2.5 to 4 KHz for variable frequency drives, hence to improve the power level it is proposed to operate the inverters in parallel by phase shift carrier, level shift carrier and carrier overlapping methods. The better spectral quality and good performance in load voltage is achieved by using asymmetric cascaded H-bridge nine-level multilevel inverter. A detailed study of the techniques was carried out through MATLAB / SIMULINK for THD and Verified experimentally by PIC 16F877A microcontroller for R-load.

Key words: Cascaded Multilevel Inverter (CMLI) · Phase Shifted PWM (PSPWM) · Level Shifted PWM(LSPWM) · Carrier Overlapping PWM(COPWM) · Total Harmonic Distortion (THD)

INTRODUCTION

Multilevel inverters are mainly suitable for high power applications, due to higher voltage operating capability, lower dv/dt's and to synthesize desired output voltage. There are three topologies for multilevel inverters: flying capacitor, diode clamped and cascaded H-bridge [1]. The proposed topology is the cascaded H-bridge inverter which significantly reduces the switches and the harmonic content as the number of voltage levels increases. The cascaded MLI is favorable for high power applications due to its modular structure, because it does not require clamping diodes or voltage balancing capacitors and the problem of voltage unbalance is eliminated by reducing the number of dc sources [2]. Multilevel inverters are commonly modulated by using carrier based pulse width modulation techniques such as phase-shifted (PSPWM), level-shifted (LSPWM) and carrier overlapping (COPWM) modulation. The Level Shifted (LSPWM), which includes Phase Disposition (PD-PWM), Phase Opposition Disposition (POD-PWM) and Alternative Phase Opposition Disposition (APOD-PWM) [3]. The three types of carrier overlapping PWM methods are also focused which operate the Control Freedom Degree (CFD) of vertical offsets among the carriers. The carriers are disposed such that the bands they occupy overlap vertical distance between each carrier is half of the amplitude [4].The other multicarrier methods such as carrier rotation PWM and modified level shifted multicarrier PWM techniques are require complex shape of the carrier signal and difficult to increase the number of levels which is given in the literature [5-6]. The phase shifted PWM is applicable for cascaded H-bridge and flying capacitor MLI topologies whereas, the level shifted PWM topology is independent [7]. The carrier based Pulse Width Modulation works with a constant carrier frequency it doesn't synchronized with fundamental stator frequency which gives an optimal utilization of switching frequency. However, carrier based level-shifted modulation technique produces the best harmonic performance than the carrier based phase-shifted modulation technique. This technique is very

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simple and efficient for higher-level cascaded H-bridge inverters.The paper is organized as follows. Introduction of trinary cascaded multilevel inverter has been presented in section I. Carrier based PWM techniques have been presented in sections III and Experimental results have been provided in section IV. The conclusion of this paper have been presented in section V.

Trinary Cascaded Multilevel Inverter: A typical configuration of a nine level trinary cascaded H-bridge MLI is shown in Fig. 1. The optimal asymmetry has been obtained using voltage sources proportionally to the two or three H bridge gives the number of levels in phase voltage obtained as follows.

$$m = 3^n \quad , if V_{dci} = 3^{(i-1)} V_{dc,} i = 1, 2, \ldots, n$$

where, n is the number of H-bridge cells per phase.

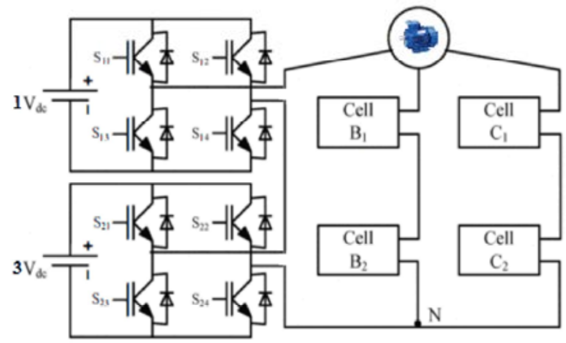

Fig. 1: Typical configuration of a Nine Level Cascaded H-Bridge Inverter

The output voltage of each phase is summed by the output voltage of two H-bridge cells. The output voltage of the first H-bridge is denoted by V_1 and the second H-bridge is denoted by V_2. The output voltage is $V = V_1 + V_2$. This inverter can generate sinusoidal waveform output voltage with the lesser harmonics.

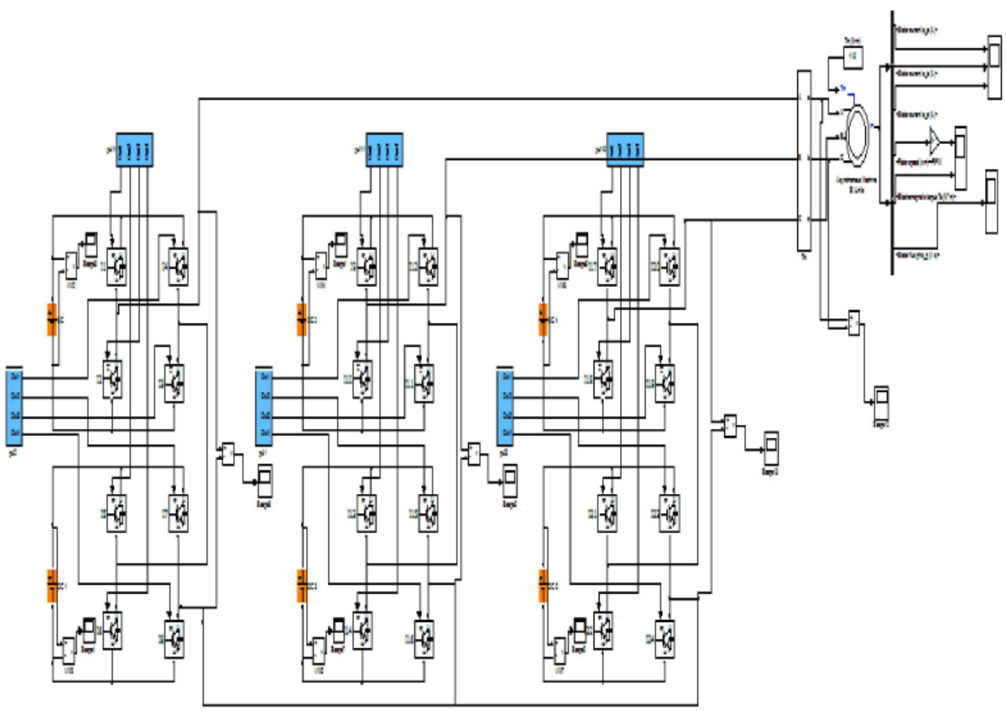

Fig. 2: SIMULINK Schematic diagram of a Nine Level Cascaded H- Bridge Inverter

To evaluate the different methods, the following definitions should be considered:

Frequency modulation index [8] is given by

$$mf = fc / fr \qquad (1)$$

where fc is the frequency of carrier signals and fr is the frequency of the reference signal.

Amplitude modulation index [8] is given by

$$ma = Ar / Ac \qquad (2)$$

where Ar is the amplitude of reference signals and Ac is the peak-to-peak value of the carrier signal.

Carrier Based Pwm Techniques: These carrier-based PWM techniques are also applicable for multilevel inverters and they are generally classified into two categories: Phase shifted multicarrier modulation (PSPWM) and Level shifted multicarrier modulation (LSPWM) [7, 9]. The other multicarrier methods such as carrier overlapping pulse width modulation (COPWM).

Phase Shifted Modulation: The multicarrier sinusoidal pulse width modulation employs m-1 carriers for producing m level output. The modulation control strategies that are proposed under Multicarrier sinusoidal pulse width modulations are carrier phase disposition method and carrier phase shift modulation. The carrier phase shift modulation technique is preferred because the stresses on the switches are equally distributed compared to carrier phase disposition method particularly in producing the upper and lower levels. The width of each pulse is proportionally varied to the amplitude of a sine wave evaluated at the middle of the same pulse. The generation of the gating signals are produced by comparing sinusoidal reference signal with triangular carrier frequency (fc). The frequency of reference signals (fr), determines the inverter output frequency and its peak amplitude (Ar) which controls the modulation index ($m_{a)}$ and rms output voltage (V_o). The number of pulses per half cycle based on carrier frequency [10]. The phase-shift PWM modulation technique have been used to generate a phase-voltage with m levels, this method uses (m–1) carriers with the same amplitude, but sinusoidal reference signal is phase shifted with 120° among themselves [11]. Therefore, for a nine-level inverter, this method uses eight carriers. The reference and carrier waveforms for phase shift PWM technique is shown in Fig. 3.

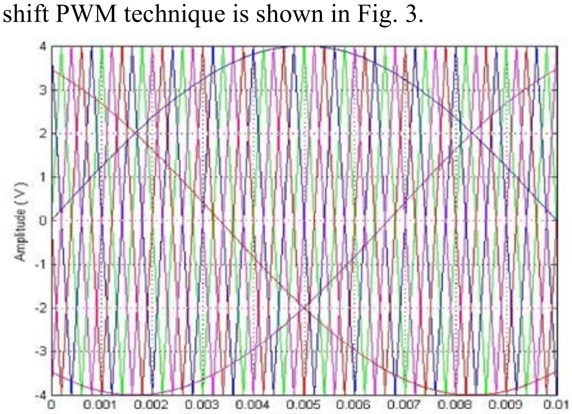

Fig. 3: Carrier and Modulating waveforms

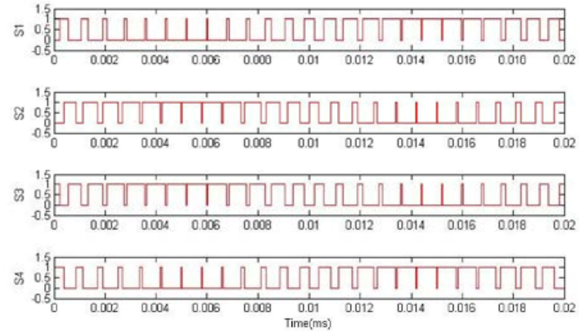

Fig. 4: Gate Pulses of upper switches waveforms

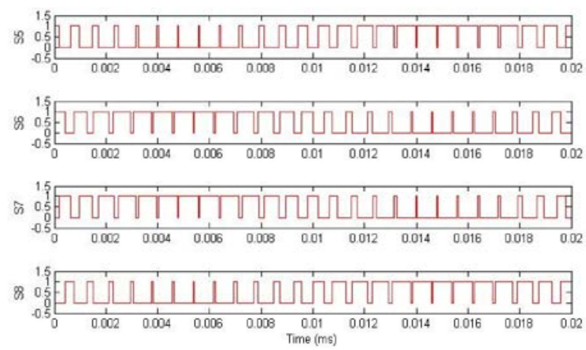

Fig. 5: Gate Pulses of lower switches waveforms

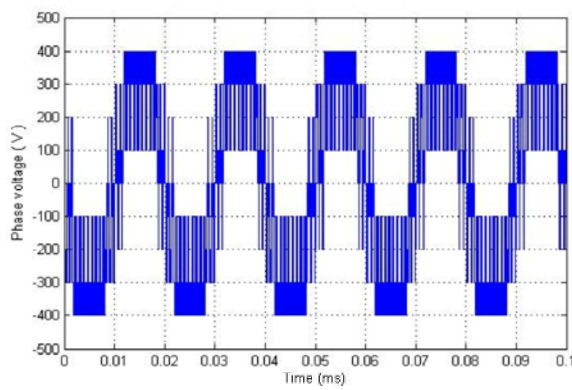

Fig. 6: Line to neutral voltage waveforms

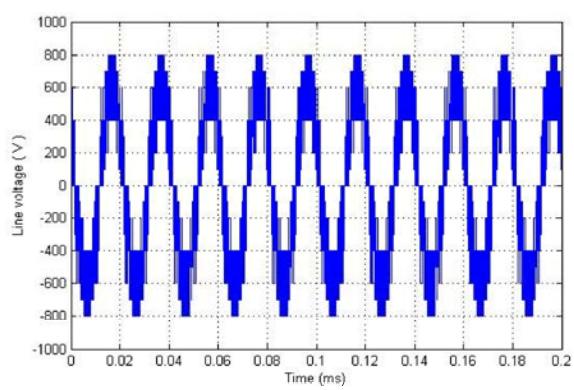

Fig. 7: Line to line voltage waveforms

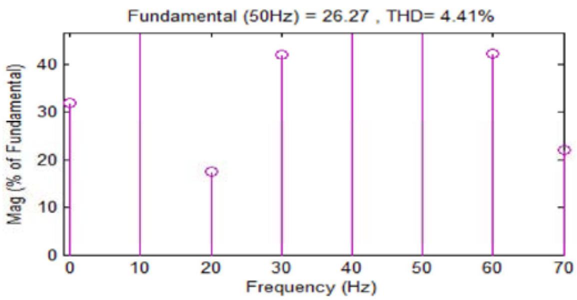

Fig. 8: Harmonic spectrum of stator current

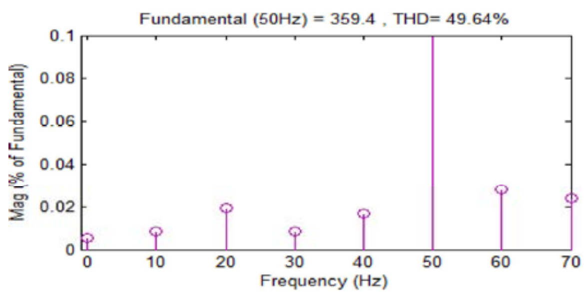

Fig. 9: Harmonic spectrum of phase voltage

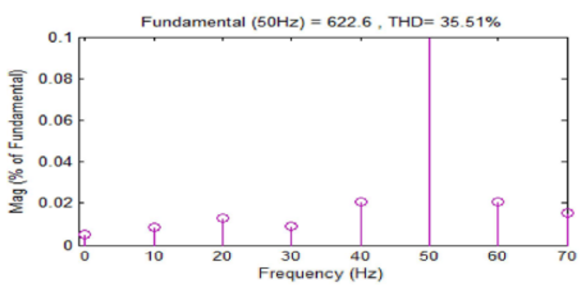

Fig. 10: Harmonic spectrum of line –to-line voltage

Level Shifted Modulation: Level Shifted methods are based on amplitude shifts between carriers which is associated to a specific voltage level. When the reference signal is over one carrier signal, the corresponding level is generated [12, 13].

Phase Disposition PWM (PD-PWM): In phase disposition PWM (PD-PWM) method, all the carriers have the same frequency and amplitude which is based on a comparison of a sinusoidal reference waveform to vertically shifted carrier waveforms [6, 13]. The PD-PWM method uses, m-1 carrier signals which are in phase with each other to generate the m-level inverter output voltage [11]. Figure 5 shows the carriers with reference signal and figure 6 shows the resulting PWM signals (with *ma* = 1.1 and *mf* =100) which gives the gate signals for the switches S1, S2, S3, S4, S5, S6, S7 and S8 of figure 1.

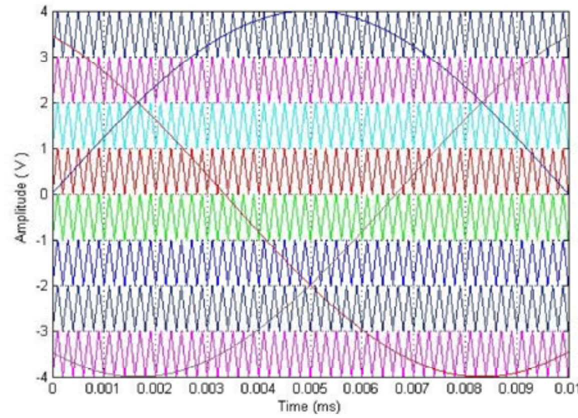

Fig. 11: Carrier and Modulating waveforms

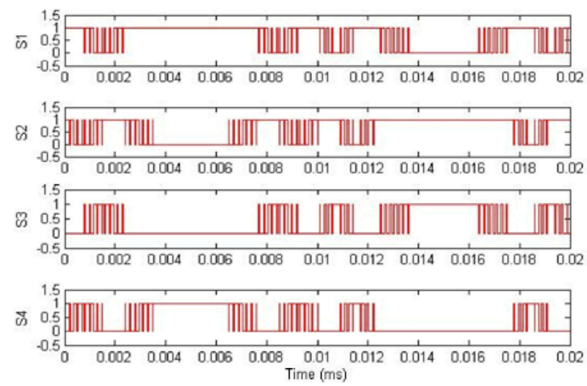

Fig. 12: Gate Pulses of upper switches waveforms

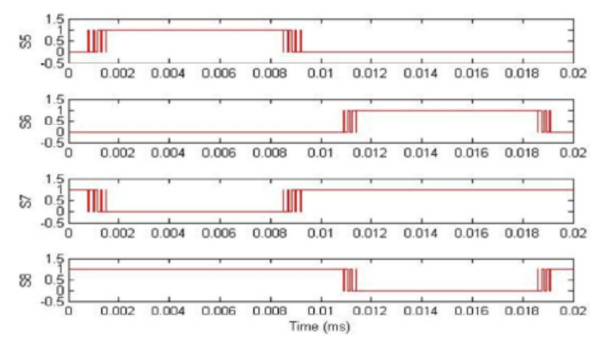

Fig. 13: Gate Pulses of lower switches waveforms

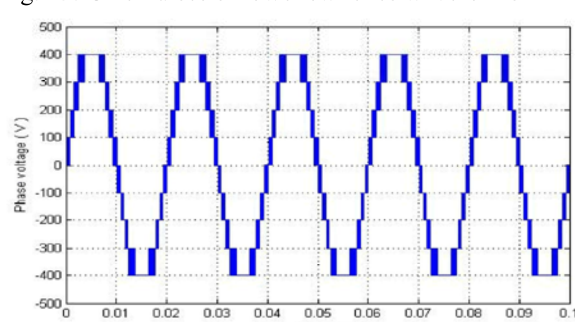

Fig. 14: Line to neutral voltage waveforms

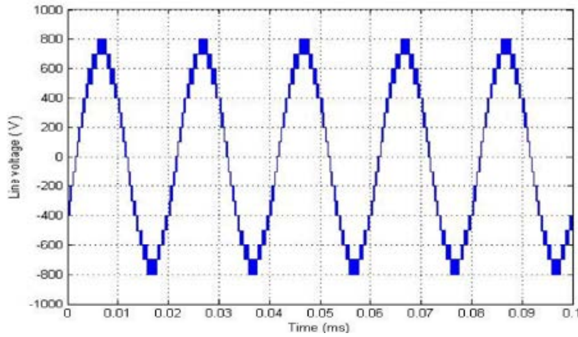

Fig. 15: Line to line voltage waveforms

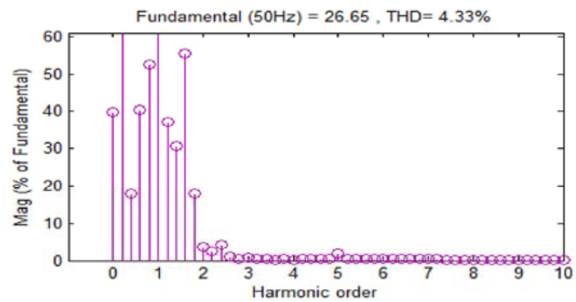

Fig. 16: Harmonic spectrum of stator current

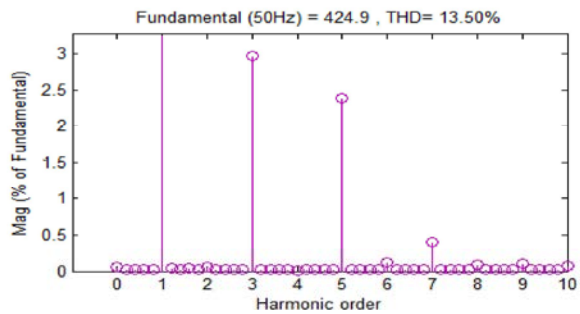

Fig. 17: Harmonic spectrum of phase voltage

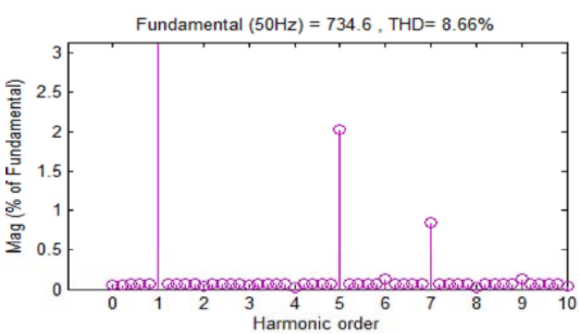

Fig. 18: Harmonic spectrum of line –to-line voltage

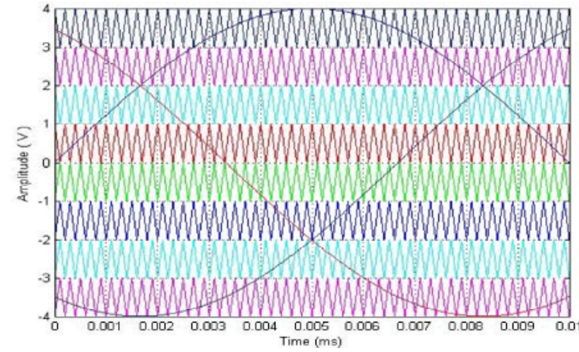

Fig. 19: Carrier and Modulating waveforms

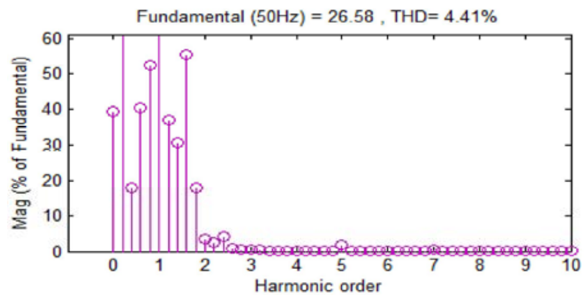

Fig. 20: Harmonic spectrum of stator current

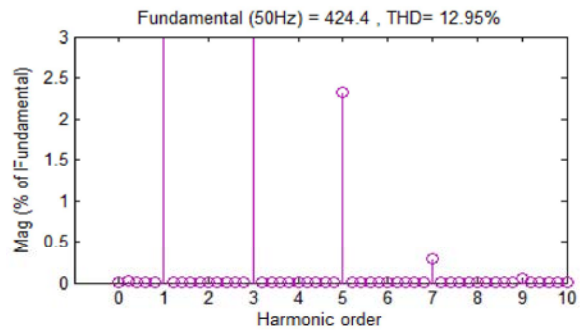

Fig. 21: Harmonic spectrum of phase voltage

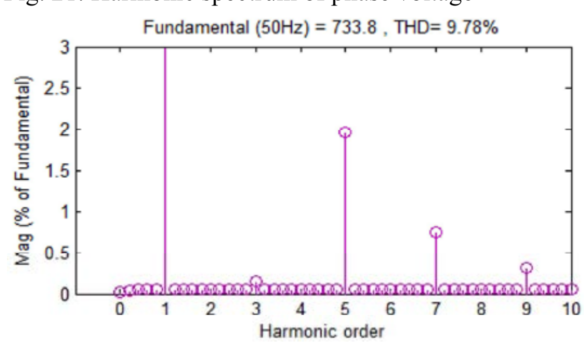

Fig 22: Harmonic spectrum of line –to-line voltage

Phase Opposition Disposition PWM (POD-PWM): In the POD-PWM method, the carrier signals above the zero axis are in phase [14, 13]. The carrier signals below zero are also in phase, but 180 degrees phase shifted, all the carrier wave have same frequency, same amplitude as Fig. 7.

Alternative Phase Opposition Disposition PWM (APOD-PWM): In the APOD method, every carrier waveform is out of phase with its neighbouring carrier by 180 degrees, all the carrier waveform have same frequency, same amplitude as shown in Figure 8.

Odd carrier waveforms are in phase but when compare to even carrier waveform are out of phase shift 180 degree [15, 13].

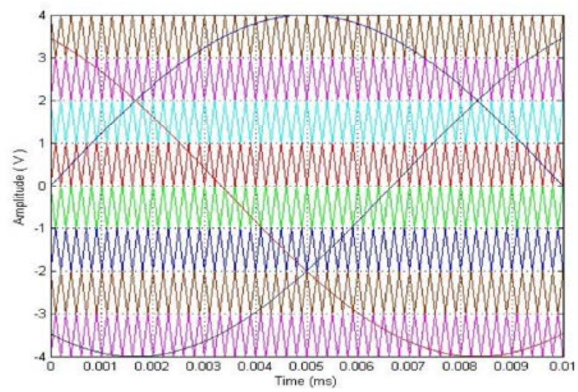

Fig. 23: Carrier and Modulating waveforms

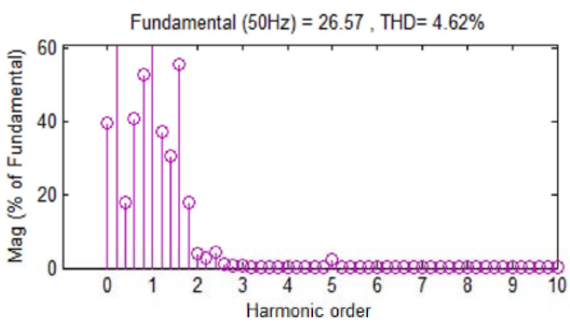

Fig. 24: Harmonic spectrum of stator current

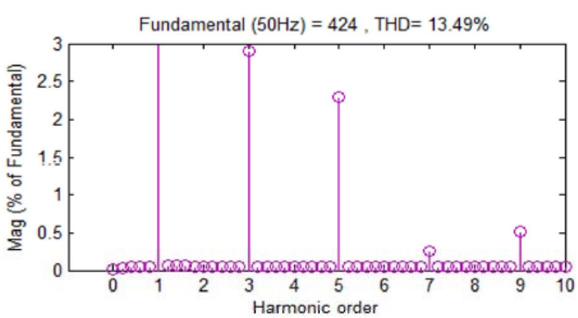

Fig. 25: Harmonic spectrum of phase voltage

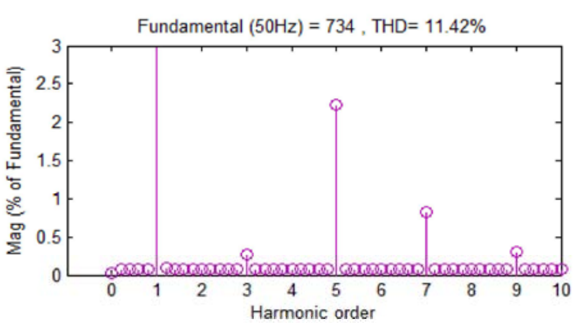

Fig. 26: Harmonic spectrum of line –to-line voltage

Carrier Overlapping Modulation: There are three types of Carrier Overlapping; they are COPWM-A, COPWM-B and COPWM-C which utilize the control freedom degree of vertical offsets among the carriers [16]. The multicarrier sinusoidal pulse width modulation employs N-1 carriers for producing N level output with the same frequency(fc) and same peak-to-peak amplitude (Ac) are disposed such that the bands dwell in overlap each other. The overlapping vertical distance between each carrier is 0.5Ac. The reference waveform is center in the middle of the carrier signals which are continuously compared with each of the carrier signals [16, 17]. The active devices are switched on, if the reference wave is more than a carrier signal. Otherwise, the device switches off.

COPWM-A Technique: The vertical offset of carriers for nine-level inverter with COPWM-A method is shown in Fig. 2. In this technique, the six carriers are overlapped with other and the reference sine wave is placed at the middle of the eight carriers [16].

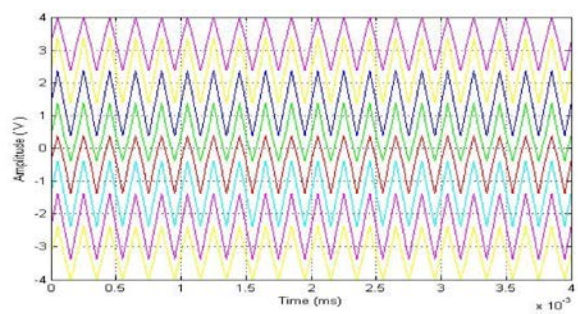

Fig. 27: Carrier waveforms of COPWM-A

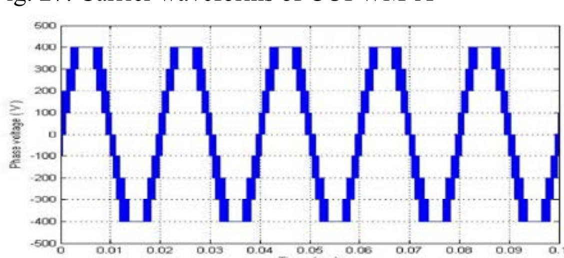

Fig. 28: Line to neutral voltage waveforms

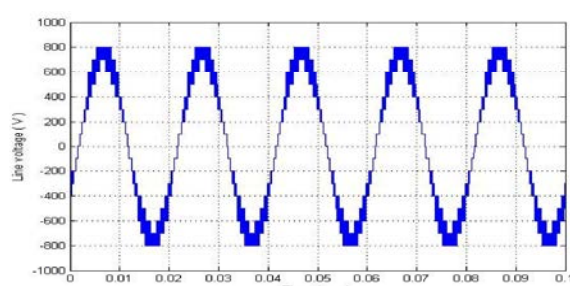

Fig. 29: Line to line voltage waveforms

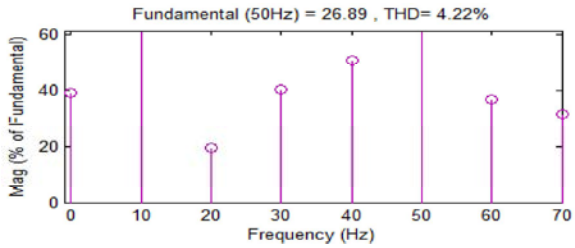

Fig. 30: Harmonic spectrum of stator current

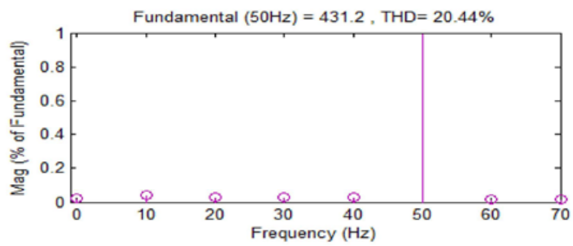

Fig. 31: Harmonic spectrum of phase voltage

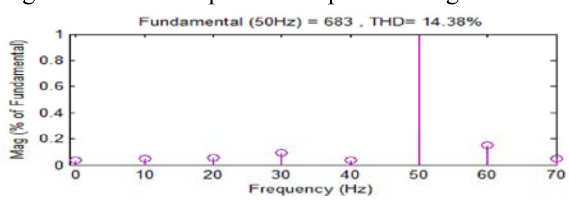

Fig. 32: Harmonic spectrum of line –to-line voltage

COPWM-B Technique: Carriers for nine-level inverter with COPWM-B method is shown in Fig.3. In this technique, the carriers are divided equally into two groups according to the positive and negative average levels which are opposite inphase with each other [16].

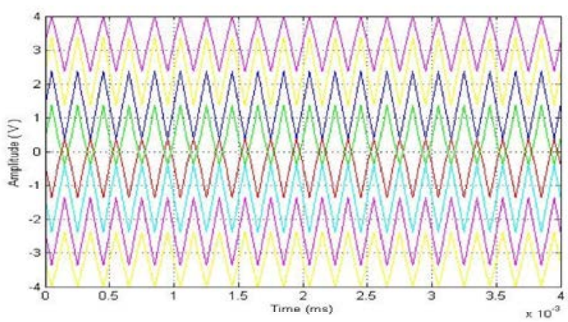

Fig. 33: Carrier waveforms of COPWM-B

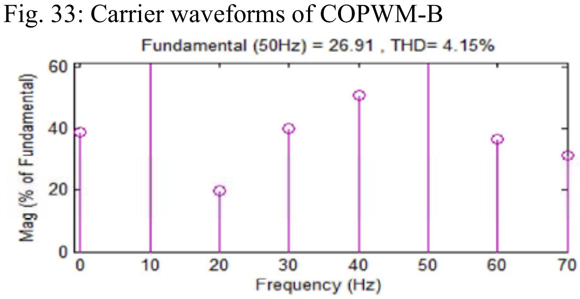

Fig. 34: Harmonic spectrum of stator current

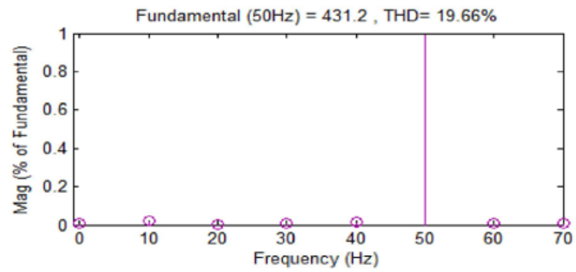

Fig. 35: Harmonic spectrum of phase voltage

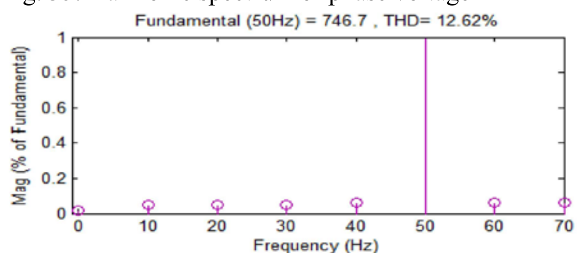

Fig. 36: Harmonic spectrum of line –to-line voltage

COPWM-C Technique: Carriers for nine-level inverter with COPWM-C method are shown in the Fig.4. In this technique, the carriers invert their phase in turns from the previous one. It is identified as PWM amplitude overlap and neighbouring phase interleaved carriers. The pattern B and C have second control freedom which change with the carriers which horizontally phase shifted from pattern A above and beyond the offsets in vertical [16].

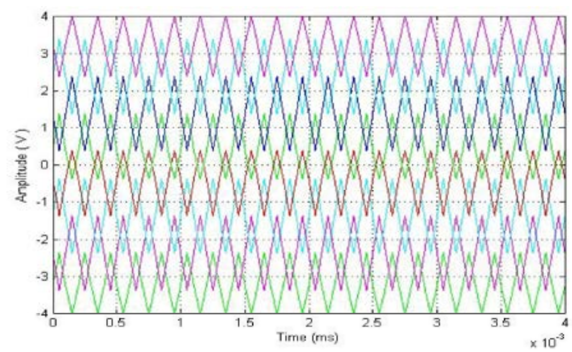

Fig. 37: Carrier waveforms of COPWM-C

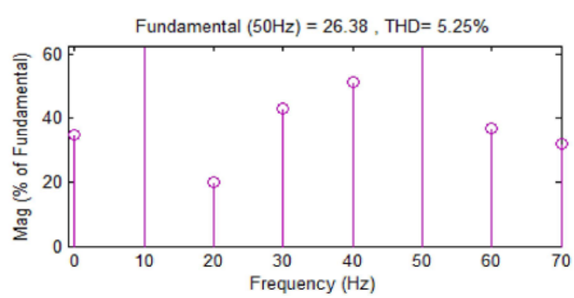

Fig. 38: Harmonic spectrum of stator current

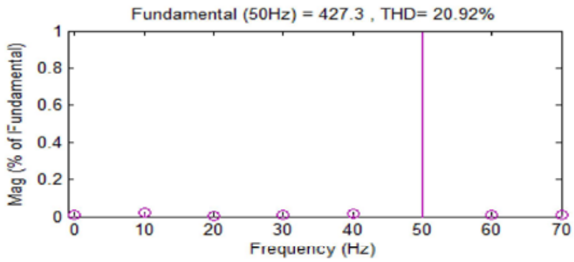

Fig. 39: Harmonic spectrum of phase voltage

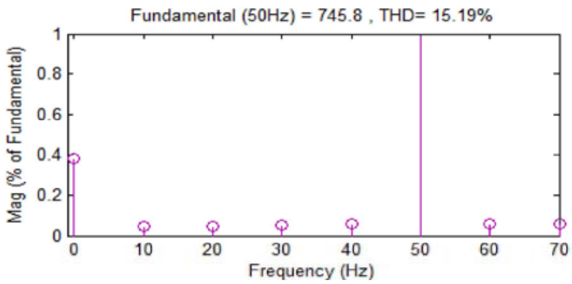

Fig. 40: Harmonic spectrum of line –to-line voltage

To verify the proposed methods, a simulation model for a three phase nine level trinary cascaded MLI with induction motor load is implemented. The simulation parameters are shown in Table I. and Validation of simulation results are shown in Table II.

Table 1: Motor Specifications

S.No	Parameters	Values
1	Ratings	4 KW, 400V, 50 Hz, 1430 rpm.
2	Stator resistance (Rs)	1.405 Ω
3	Rotor resistance (Rr)	1.395 Ω
4	Inductance	Ls=0.0058 H, Lm=0.1722 H.
5	Moment of Inertia	0.0131 J
6	Friction factor	F=0.002985
7	Pole pairs	2
8	Main DC source voltage (Vdc)	300 V
9	Modulation Index (ma)	1.1
10	Carrier Frequency	5KHz
11	Rated Output Frequency	50 z

Table 2: Validation of Simulated Results

Total Harmonic Distortion (THD) %	Phase shifted PWM	Level shifted PWM			Carrier overlapping PWM		
		PD	POD	APOD	CO PWM-A	CO PWM-B	CO PWM-C
Phase Voltage	49.64	13.50	12.95	13.49	20.44	19.66	20.92
Line Voltage	35.51	8.66	9.78	11.42	14.38	12.62	15.19
Stator Current	4.41	4.33	4.41	4.62	4.22	4.15	5.25

The harmonic spectrum of the inverter output voltage waveforms are dependent on frequency modulation index (mf) whether if it is even or odd. Comparing the above three techniques, the PD-PWM method have better output voltage quality with lower distortion and has significant harmonic energy at the carrier frequency which is suitable for three phase applications. The triplen harmonics are cancelled in the line-to-line voltage of three phase systems, So that the low order harmonics can be found only in the phase voltage.

Experimental Results: To validate the single-phase asymmetric cascaded H-bridge multilevel inverter with R load which have the value of R = 10 ohms, a prototype module of Phase Dispostion (PD) PWM is built using IRF840 as the switching devices and is experimented as shown in figure 41.PIC16F877A micro controller is used to implement the gating pattern that associates and evaluates with other modules, hybrid MLI setup (Optocoupler, driver & power circuit) and load configuration. This will be helpful to design the hardware for induction motor load.

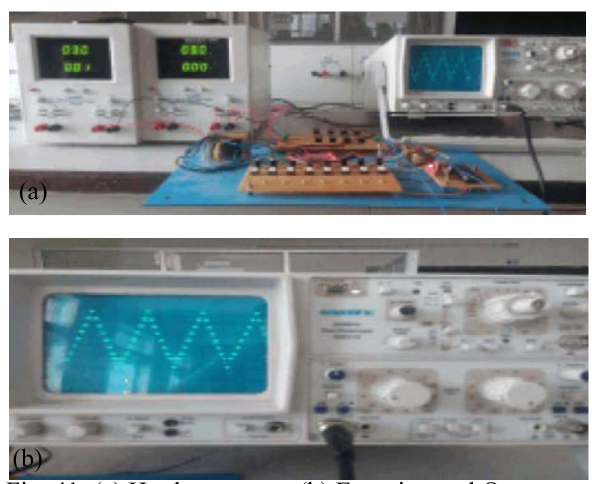

Fig. 41: (a) Hardware setup (b) Experimental Output

CONCLUSION

This paper has investigated a three-phase asymmetric nine-level cascaded multilevel inverter with minimum number of switching devices thus decreasing the complexity and the cost of the circuit. A Level shifted

PWM technique has been employed and the performance of the inverter with induction motor load has been studied. From the simulation results, it is observed that the Phase Disposition (PD) proposed technique reduces THD and balances the switching action among the switches in MLI. Particularly, FFT spectrum shows the triplen harmonics are cancelled in the line-to line voltage with LSPWM technique which is suitable for three phase systems, thereby contributing to lesser torque ripples. The proposed MLI with reduced number of switches can be employed for electric vehicle applications. The multilevel inverter can be controlled by PIC 16F877A microcontroller for high speed operation.

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