Middle-East Journal of Scientific Research
24 (Recent Innovations in Engineering, Technology, Management & Applications): 74-80, 2016
ISSN 1990-9233; © IDOSI Publications, 2016
DOI: 10.5829/idosi.mejsr.2016.24.RIETMA113

Design of Single Phase Nine Level Inverter for an Unbalanced Capacitor

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Abstract: This paper presents an effective circuit configuration of a nine level inverter. In this proposed system, the unbalanced capacitor voltage that occur in series connected capacitor will be compensated by connecting resistors in parallel and then by the number of power electronic switches, the output voltage level is improved. The circuit consists of single dc source, series capacitor and eight number of switching devices. This proposed method is very efficient to achieve nine level output voltage and reduction in total harmonic distortion. The experimental results correlate well with simulation and a prototype drive has been built and tested to verify its practical viability.

Key words: Inverter · Multilevel systems · Total harmonic distortion · Stepped pulse width modulation (PWM)

INTRODUCTION

Recently, variable powers are required in many industrial applications. The advent of power electronic components such as thyristors, triacs, GTO, IGBT, power transistor, etc., have a major impact on industrial world. These components are used to develop converters which inject harmonic currents on the electrical network and draw non-sinusoidal currents from utility grids, thus contributing to degradation of power quality in distribution or industrial power systems [1]. Multilevel inverter that can increase the number of output voltage levels with a reduced number of circuit components [2]. Thus, the multilevel inverter has an alternative for both medium voltage and high power situation. The need of multilevel inverter is to give a high output power from medium voltage source like a batteries, super capacitor etc., are medium voltage sources.

Cascaded H-bridge (CHB) multilevel inverters have been considered as an alternative in the medium-voltage converter market and experimental electric vehicles. Their variant, the asymmetrical CHB (ACHB) inverter, optimizes the number of voltage levels by using dc supplies with different voltages [3]. Many number of voltage levels ensures a high quality output voltage which shows a good total harmonic distortion. In order to attain high voltage levels ,a multilevel inverter using switched series/ parallel dc voltage source was introduced in [4]. Although its output voltage level rises, the pattern of switching is difficult and it escalation the conduction losses. A solar cell array used for power generation along with seven level inverter was introduced in [5]. It consists of dc-dc converter, a solar array cells and seven level inverter to generate a power. However the power circuit is simplified, the cost is expensive due to presence of solar cell array

A single phase seven level inverter with less number of power elements for grid connection was introduced in [6]. Even though it reduces total harmonic distortion it requires eight switches for producing seven level of output voltage and it has two voltage sources. A multilevel inverter using dc voltage source was introduced in [7]. It produces output voltage stages, but it does not reduce the number of dc source. A seven level PWM inverter employing series connected capacitors was introduced in [8]. It presents a seven level inverter with seven switches. Its output voltage has the following seven levels: zero, +Vdc, +Vdc/3, +2Vdc/3, -Vdc, -Vdc/3, -2Vdc/3. This inverter topology uses the carrier signals to generate PWM signals for the switches.

The proposed inverter produces nine level output voltage are: zero, +Vdc/4, +2Vdc/4, +3Vdc/4, +Vdc, -Vdc/4, -2Vdc/4, -3Vdc/4, -Vdc. In this proposed inverter have eight switches for nine level output voltage. Here we overcome the problem of voltage unbalance that happens in series connected capacitor.

The proposed system has many advantages:

- It reduces number of dc voltage sources by using passive element (capacitor).
- The nine level output voltage is generated by using eight switches.
- FPGA controller is used in the proposed system, because it consists of 144 I/O pins.
- FPGA processing speed is very high compare to DSP.

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Proposed System

Circuit Configuration: The circuit configuration of proposed nine level inverter consists of single dc voltage source which is parallel to four capacitor connected in series. Each capacitor connected in parallel with resistor. The two diodes are anti-parallel to get full wave. The output voltage levels are: zero, +Vdc/4, +2Vdc/4, +3Vdc/4, +Vdc, -Vdc/4, -2Vdc/4, -3Vdc/4, -Vdc [9]. The highest voltage and lowest voltage levels (+Vdc or –Vdc) are produced by the switches S1, S2, S3 and S4. The remaining levels are generated by S5, S6, S7 and S8. The resistive load is connected across the H-bridge circuit, inductive load is also applicable.

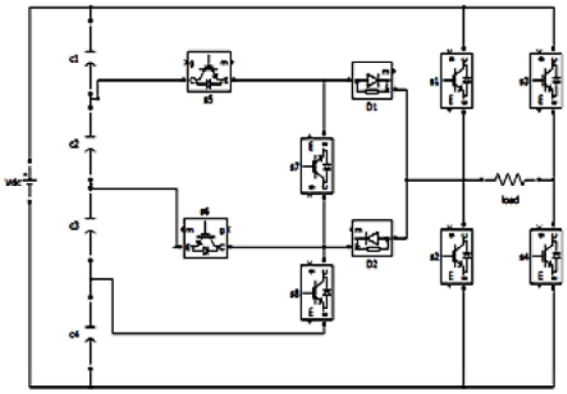

Fig. 2.1: Proposed nine level inverter

Modes of Operation: The modes of operations are used to define the current flow in switching components to obtain output voltage levels.

Mode 0: The switches S1 and S3 are contribute to produce the voltage level with zero volts.

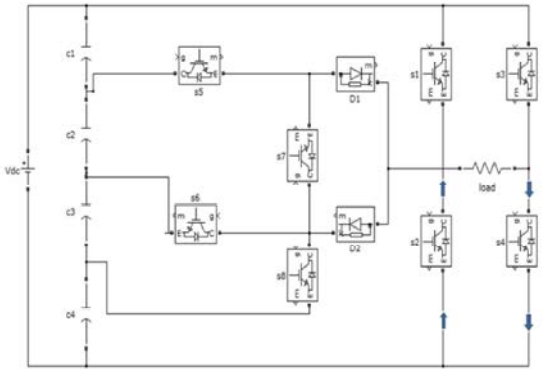

Fig. 2.2 (a): Mode '0'

Mode 1: (+Vdc/4) The switches, diodes DS8, S7, D1 and S4 are contribute to produce the voltage level with +Vdc/4 voltage.

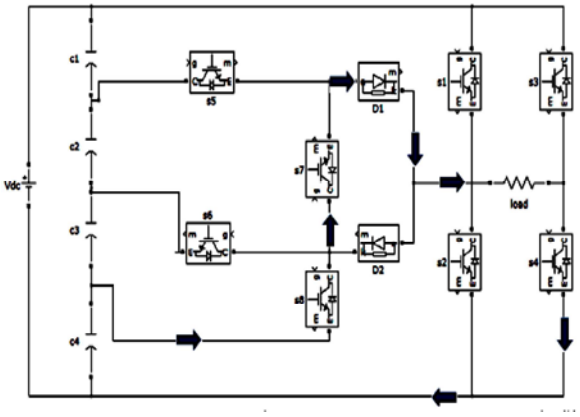

Fig. 2.2(b): Mode '1'

Mode 2: (+2Vdc/4): the switches, diodes DS6, S7, D1 and S4 are contribute to generate the voltage level with +2Vdc/4 voltage.

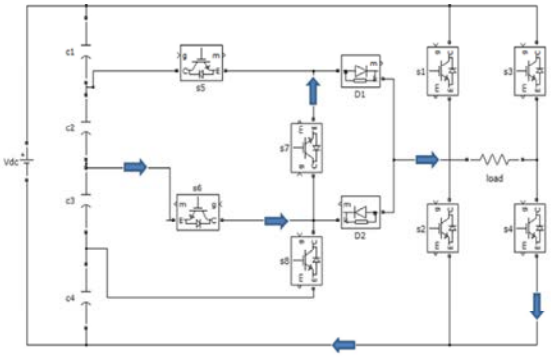

Fig. 2.2(c): Mode '2'

Mode 3: (+3Vdc/4): the switches, diodes S5, D1 and s4 are contribute to generate the voltage level with +3Vdc/4.

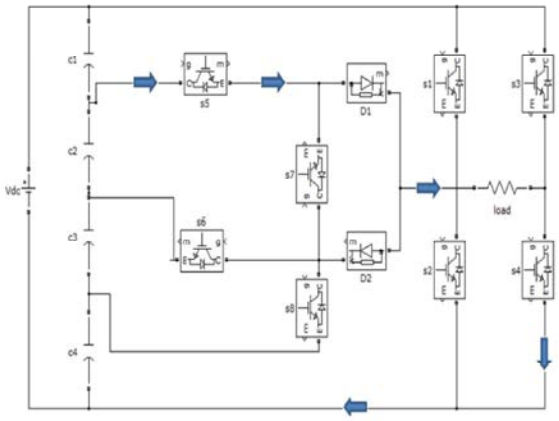

Fig. 2.2(d): Mode '3'

Mode 4: (+Vdc): the switches S1 and S4 are contribute to generate the voltage level with Vdc voltage.

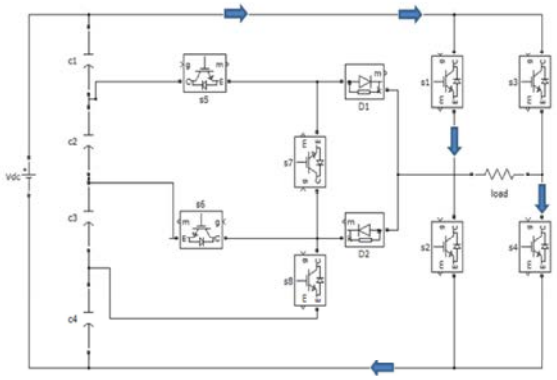

Fig. 2.2(e): Mode '4'

Mode 5: (-Vdc/4): the switches, diodes S3, D2 , S7 and DS5 are contribute to produce the voltage level with –Vdc/4 voltage.

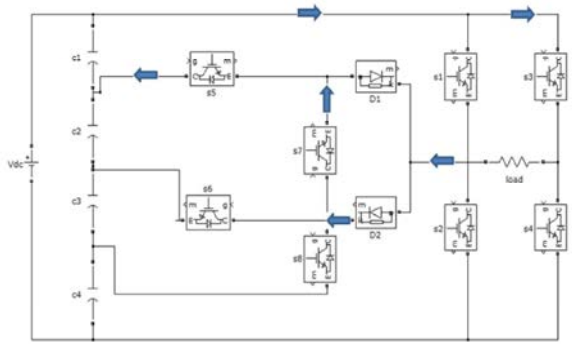

Fig. 2.2(f): Mode '5'

Mode 6: (-2Vdc/4): the switches, diodes S3, D2 and S6 are contribute to produce the voltage level with -2Vdc/4 voltage.

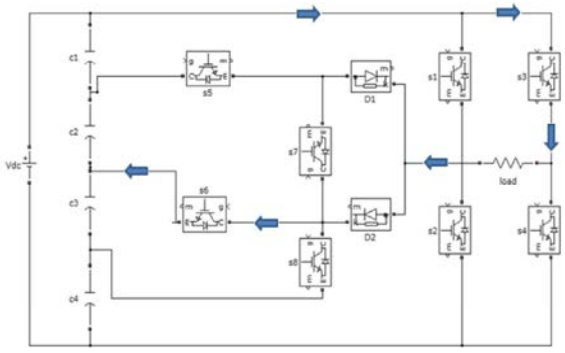

Fig. 2.2(g): Mode '6'

Mode 7: (-3Vdc/4): the switches, diodes S3, D2 and S8 are contribute to produce the voltage level with -3Vdc/4 voltage.

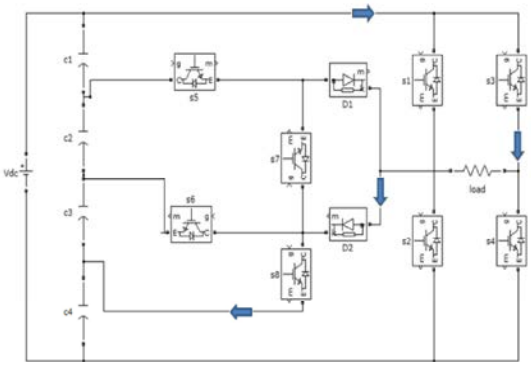

Fig. 2.2(h): Mode '7'

Mode 8: (-Vdc): the switches S2 and S3 are contribute to produce the voltage level with –Vdc voltage.

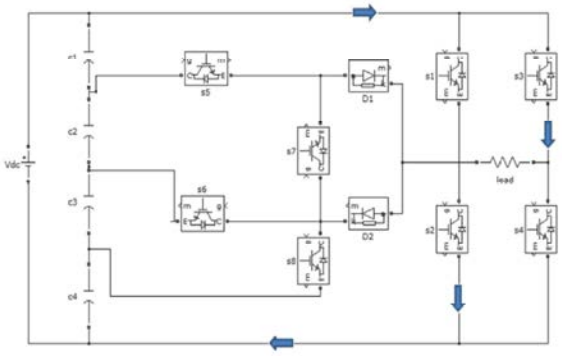

Fig. 2.2(j): Mode '8'

Table of Switching Operation :

Table 2.1: Switching operation

S.no	Output voltage	Direction of current flow	On states
1	+vdc/4	Positive	DS8, S7, D1 ,S4
2	-vdc/4	Negative	S3, D2, S7, DS5
3	+2vdc/4	Positive	DS6, S7, D1, S4
4	-2vdc/4	Negative	S3, D2, S6
5	0	-	S1, S3
6	+3vdc/4	Positive	S5,D1,S4
7	-3vdc/4	Negative	S3, D2, S8
8	+vdc	Positive	S1,S4
9	-vdc	Negative	S2,S3

Switching Pulses: The nine level inverter produces output voltage of nine levels with the help of stepped PWM technique. PWM is a modulation technique used to encode a message in to a pulsing signal. The ratio of carrier time to the fundamental sinusoidal time gives

certain time duration, which is split to produce ON and OFF time to generate pulses. FPGA is used to control the stepped PWM signal and it has 144 I/O ports. In FPGA, rather than making changes in entire hardware, it can be done by changing the code itself.

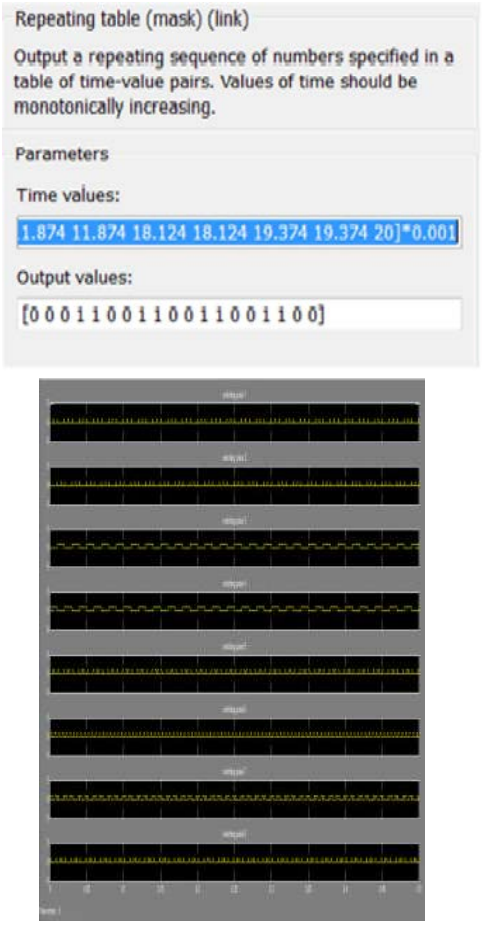

Fig. 2.3: Generation of Step Signals

Compensation of Unbalanced Voltage: A space vector modulation (SVM)-based approach that benefits from the switching state redundancy of an n-level FCC to implicitly carry out the voltage balancing task within the switching strategy [10, 11]. In this this system instead of SVM the siusoidal PWM (SPWM) has proposed. Generally capacitor will have voltage unbalance because of charging and discharging properties. the capacitor which is near to the sources will get charged first up to its maximum limits. Then capacitor next to that will not get its requried voltage limits,which affects the voltage level generation in the output side. In order to sort out this problem resister is connected in parallel with capacitor. So that charging and discharging will occur almost equally in all the capacitor. The balanced voltage is given by:

$$\text{Voltagebalance} = \frac{\text{Maximum deviation from Average Voltage}}{\text{Average voltage}} X100$$

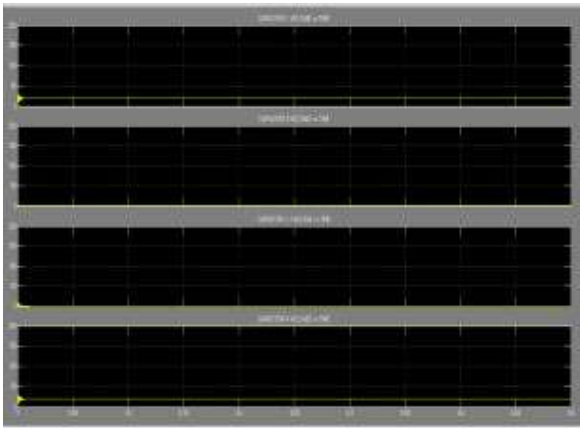

Fig. 2.4: Unbalanced capacitor voltage

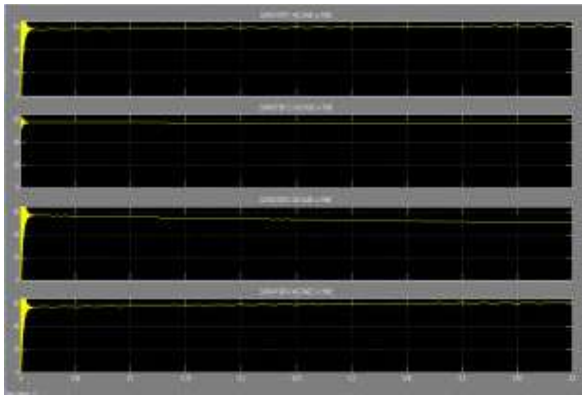

Fig. 2.5: Balanced capacitor voltage

Simulation Result

Existing System:

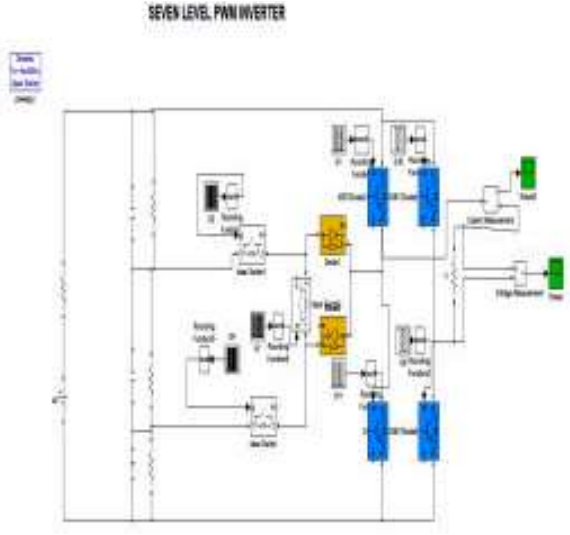

Fig. 3.1: Existing seven level inverter

The above setup is seven level inverter which is of symmetrical in nature which generates output voltage of seven level. The seven level inverter consist of seven switches to generate seven levels.

Total Harmonic Distortion: It is the ratio of RMS value of harmonic to the fundamental RMS value;

$$THD_V = \frac{\sqrt{\sum_{n=2} V_n^2}}{V_1}$$

where V1: fundamental components

Vn: Harmonic Order: The output voltage of seven levels is shown in Figure 3.1(a) and the FFT analysis is carried out to compute total harmonic value using MATLAB simulation is shown in figure 3.1(b). From the simulation output the Total Harmonic Distortion (THD) of the existing seven level inverter using FFT analysis is 21.84%.

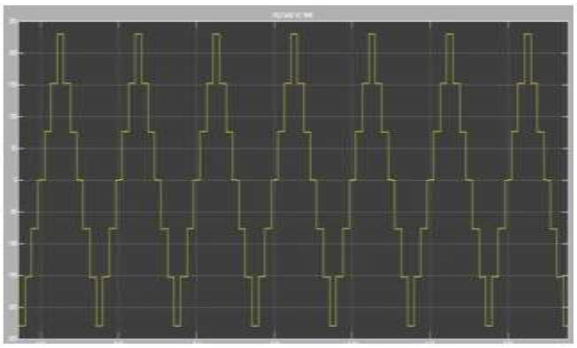

Fig. 3.1 (a): Seven level Output Voltage

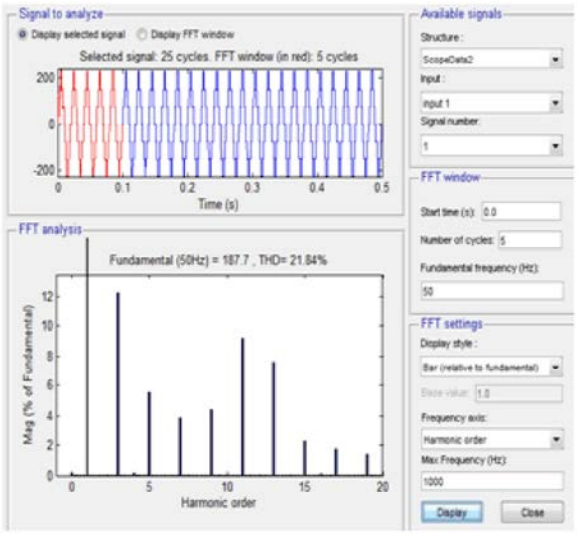

Fig. 3.1 (b): FFT analysis of Seven level Inverter

Proposed Nine Level Inverter System

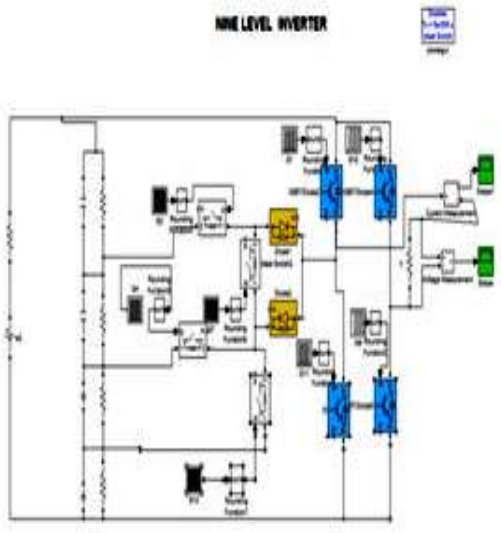

Fig. 3.2: Proposed Nine level inverter

The above Fig. 3.2 shows the circuit configuration of proposed nine level inverter which generates nine level of output voltage with eight switches and then single dc source with four passive element. The output voltage of Proposed nine level inverter voltage and the THD value is calculated by the MATLAB simulation. The proposed system generates nine level output voltage with eight switches and their THD value is 18.50% but in existing system by using seven switches, they produced seven level output voltage and their THD value is 21.84%.

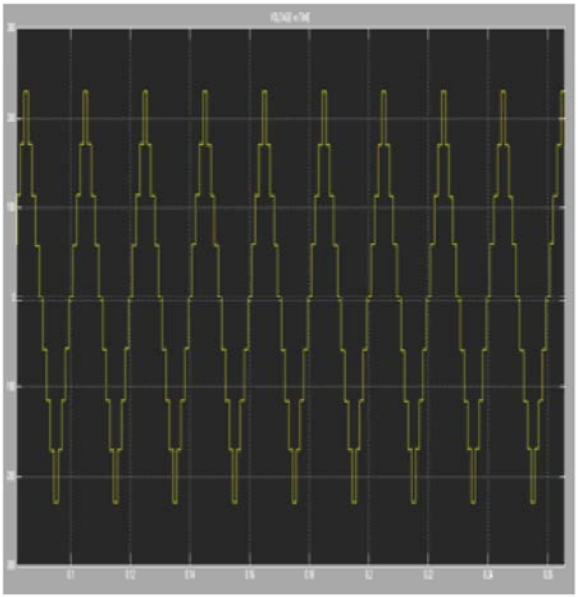

Fig. 3.2 (a): Output Voltage of Proposed Nine level inverter

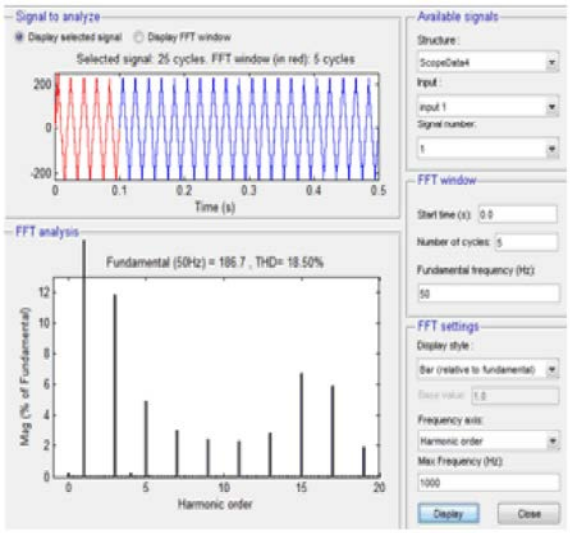

Fig. 3.2 (b): FFT analysis of Nine level inverter

Experimental Results: The simulation result is well correlated with experimental result .The hardware consists of 4 units:

- Power supply unit
- Capacitor bank
- Controller unit
- Switching unit

Power Supply Unit: The power supply unit have stepdown transformer of (0-18V) to supply 12V for the components and then another stepdown transformer of (0-9V) to supply 5V FPGA. To produce 12V bridge rectifier, fliter. Then to generate 5V regulator unit is used.

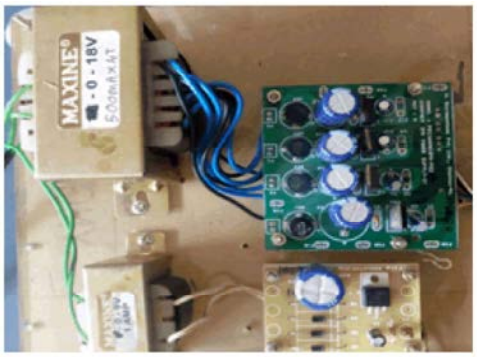

Fig. 4.1 (a): Power Supply Unit

Capacitor Bank: Generally, multilevel inverter requires separate dc source for each level. Inorder to reduce the number of dc sources, four series capacitor(passive element)is used. The rating of capacitor is 4700 micro farad.

Fig. 4.1 (b): Capacitor bank Unit

Controller Unit: FPGA controller is used in the proposed system which has XILINX SPATRAN 3E, A Field-programmable Gate Array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing-hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL).JTAG connector is used to feed the program to controller. Serial port is used to connect the FPGA and switches.

Fig. 4.1 (c): Controller Unit

Switching Unit: The H bridge consists of four switches S1, S2, S3 and S4 which are used to generate polarity voltage level and switches S5, S6, S7 and S8 are used to generate remaining voltage levels. The MOSFET is used as switching devices voltage rating is 400V, current rating is 8A.

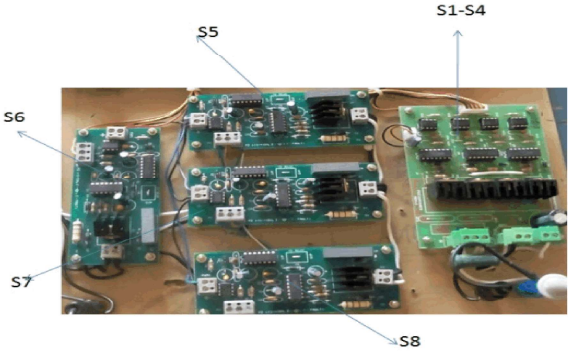

Fig. 4.1 (d): Switching Unit

The output of the proposed nine level inverter prototype is analysed with the help of CRO.

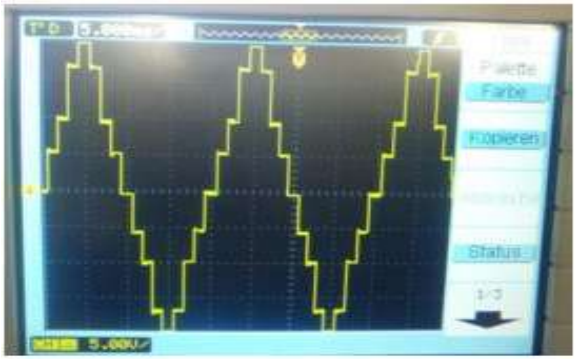

Fig. 4.1 (e): Experimental output voltage waveform

The result is compared with the existing system also.

Table 3.1: Comparison of exisiting and proposed system

Parameter/technique	Exisitng system	Proposed system
No.of.switches	7	8
Levels	7 level	9 level
PWM technique	sinusoidal	stepped
THD value	21.84%	18.50%
Controller	DSP	FPGA
Switching loss	high	less

CONCLUSION

This paper has persented “design of single phase nine level inverter for an unbalanced capacitor voltage to get the desired nine level output voltage by reducing the number of power electronic switches. The proposed nine level inverter reduces the THD value, also the unbalanced capacitor voltage is balanced by adding series resistor in the input of inverter circuit.

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