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Design of a 1.2-V, 4-Bit Flash ADC Using Sub Threshold CMOS Voltage Reference

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Abstract: In this paper, a 4 bit ADC (Analog to Digital Converter) is designed for low power CMOS. It requires 2^N-1 comparators and an encoder. This ADC is integrated with proposed subtheshold CMOS voltage reference which is generated by replacing the analog amplifier in the conventional voltage reference circuit by low voltage comparator, charge pump circuit and a digital control unit. It is going to generate 274mv reference voltage at 374mV supply voltage and consumes less power. The design is simulated in cadence environment using spectre simulator under 90nm technology. The pre simulation results for the design shows a low power dissipation of 6.984mW for the designed ADC. The circuit operates with an input frequency of 6MHz and 1.2V supply with a conversion time of 6.182ns.

Key words: Subthreshold · Flash ADC · Encoder · Low power · Voltage reference

INTRODUCTION

ADC (Analog to Digital Converter) provides link between the analog world and the digital systems. It will produce digital output D as a function of analog input A as follows D=f (A). It can be accomplished by generating a set of reference voltages and comparing it with the analog input and selecting the input which is closest to the reference. In most of the ADC's analog input is a voltage quantity because comparing, routing and storing are easier for voltages rather than currents. As there is demand for low power design, different kinds of voltage reference circuits had been used in ADC to generate reference voltage which will be used for comparing with input voltage.

Low voltage and Low power operation are two consequential design criteria for voltage reference. In CMOS technology, a parasitic vertical bipolar junction transistor is often utilized in voltage reference circuits. Filanovsky and Allam studied MOSFET temperature deportment pointing out that below a certain technology dependent partialness point, the gate-source voltage of a MOSFET, inequitable with a fine-tuned drain current, decreases with temperature in a quasilinear fashion [1]. Starting from this observation, a gate to source voltage can be used in instead of a base-emitter voltage to design a voltage reference independent of temperature. The Bandgap Voltage Reference (BVR) circuits are commonly used owing to their high precision. These have been implemented in standard CMOS technologies exploiting parasitic vertical Bipolar Junction Transistors (BJT).Several BVR circuits are implemented in submicron BICMOS technology [2]. This circuit operates with a supply voltage of 1 V. Later several low voltage low power Voltage Reference (VR) predicated on incipient circuit topology and on subthreshold MOSFETS. It exploits the fact that the gate source voltage of MOSFET, after biasing with constant drain current decreases linearly with temperature [3]. Several techniques for sub 1-V operation has been proposed to reduce the supply voltage [4].

The other techniques are implemented by superseding the p-n junction circuit with the diode-connected NMOS transistors partial in the subthreshold region [5]. This brief proposed a subthreshold CMOS voltage reference circuit, which is predicated on conventional CMOS voltage reference circuit. So the low power operation is obtained by placing this sub threshold CMOS voltage reference design in the ADC.

Conventional Voltage Reference Design: This conventional CMOS voltage reference circuit shown in Fig. 1 where the diode connected NMOS transistors M1 and M2 in the subthreshold region replace the BJTs in the traditional bandgap reference circuits.

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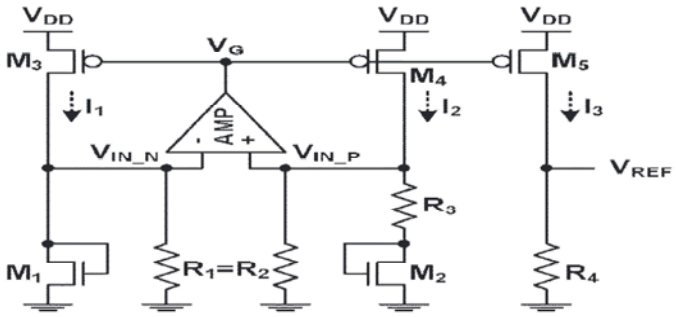

Fig. 1: Conventional CMOS voltage reference circuit

MOSFET in Subthreshold Region: In this section we will explore the behavior of the MOS transistor in the subthreshold regime where the channel is weakly inverted.

In NMOS transistors in the subthreshold region, the Temperature Coefficient (TC) for the effective Gate-source voltage V_{GS} is negative. V_{GS} can be approximated as a function of temperature, where the quantity of K_G is negative, T is the absolute temperature and T_0 is the room temperature.

$$I_D = I_{DO} e^{\frac{V_{GS}-V_{th}}{V_t}} \quad (1)$$

where I_{DO} is current at $V_{gs} = V_{th}$ and $V_T = \frac{KT}{q}$

Equation (1) is used to derive the sub threshold current of MOSFET.

Circuit Operation:

$$V_{GS} = V_{GS}(T_o) + K_G\left(\frac{T}{T_o} - 1\right) \quad (2)$$

The channel width of transistor M_2 is N times larger than that of the transistor M_1.

The amplifier makes two voltages V_{IN_N} and V_{IN_N} equal. The voltage over the resistor R_3 (V_{R3}) is express as follows;

$$V_{R3} = V_{GS1} - V_{GS2} = nU_T \ln(n) \quad (3)$$

Where n is the substrate factor and U_T is the thermal voltage.

The PMOS transistors M_3,M_4,M_5, have the same size.Because resistors R_1 and R_2 are equal, currents I_1, I_2 and I_3 are equal to $(nU_T \ln(N) + \frac{R_3}{R_1} V_{GS1})$.

So the output reference voltage is defined as follows:

$$V_{REF} = \frac{R_4}{R_3}(nU_T \ln(N) + \frac{R_2}{R_1} V_{GS1}) \quad (4)$$

Thermal voltage U_T and gate–source voltage V_{GS} have positive and negative TCs, respectively. The voltage reference circuit makes a temperature-in sensitive reference voltage by selecting the R_3/R_1 value. Outputre ference voltage V_{REF} is controlled by choosingthe R_4 value.

The schematic and simulation result of conventional voltage reference is shown in Fig. 2 and Fig. 3.

Proposed Voltage Refrence Circuit: This circuit is implemented by using the conventional design as shown in Fig. 4. It has been implemented by replacing the analog amlifier in the conventional design by a low voltage comparator and a charge pump circuit and control unit circuit.

Control Unit: This control circuit shown in Fig. 5 is going to generate four control signals named as follows:

- SAE1 (Sense Amplifier Enable1)
- SAE2 (Sense Amplifier Enable2)
- CS (Charge Sharing)
- PC (Pre Charge)

Here D Flipflop(D-FF) is implemented by using transmission gates.

Low Voltage Comparator: The proposed Low voltage comparator as shown in Fig. 6 detects the voltage difference between V_{IN_N} and V_{IN_P}. And is is going to add an auxiliary amplifier to the conventional sense amplifier type comparator. The auxiliary amplifier will improve the sensing speed and expanse the range of input voltages of comparator because its amplification is independent of Vin.

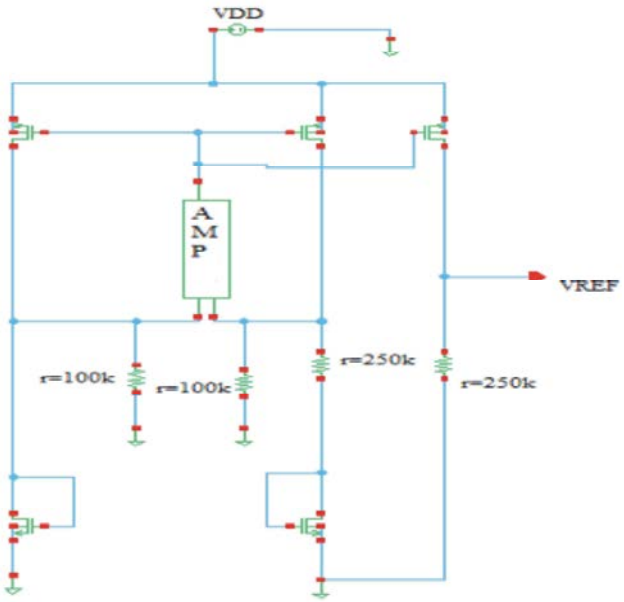

Fig. 2: Conventional Voltage Reference circuit

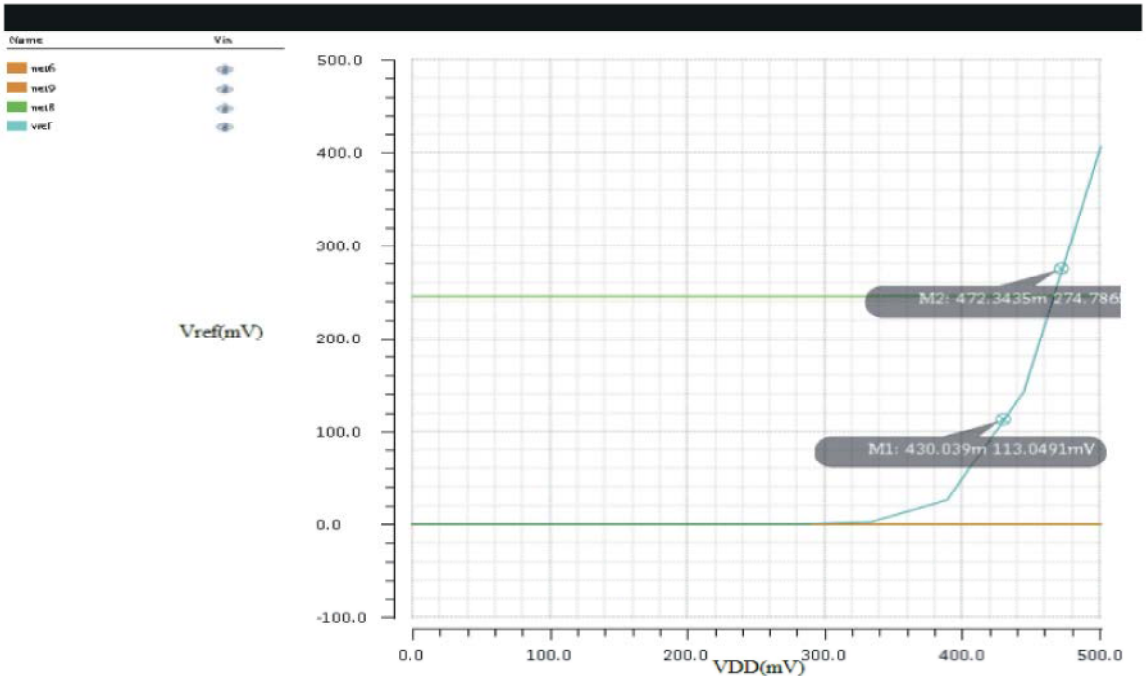

Fig. 3: Variation of supply voltage vs Reference voltage in conventional design

The comparator without the auxiliary amplifier operates very slowly when two input voltages (i.e. V_{IN_N} and V_{IN_P}) are low and the input voltage difference ($\Delta V_{IN} = V_{IN\_N} - V_{IN\_P}$) is small. When V_{IN} is low, the current difference between M_1 and M_2 ($\Delta I_{CMP} = g_{m1,2} \times \Delta V_{IN}$) becomes quite small; hence, the voltage difference on nodes V_1 and $V2$ ($\Delta V_{1,2} = V_1$-V_2) increases very slowly. In addition, the voltage amplification on the nodes V_1 and V_2 by the cross- coupled latch M_3-M_6) is very slow because the pull-down current of the cross-coupled latch is limited to the drain currents of M_3 and M_6 (i.e., I_{D1} and I_{D2}). Then, the drain currents significantly decrease proportional to VIN. Moreover, the comparator without the auxiliary amplifier does not operate at very low input voltage where

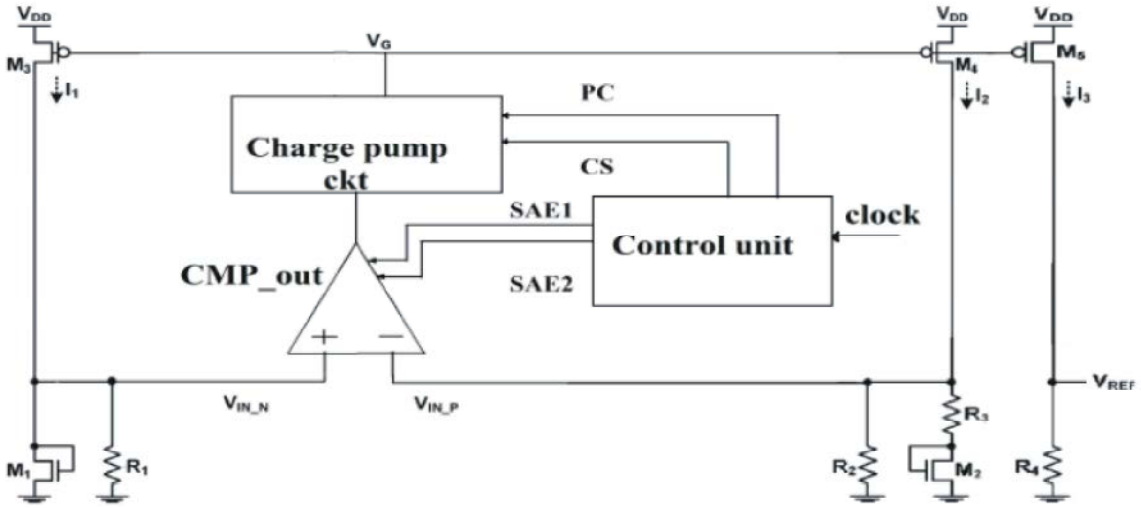

Fig. 4: Proposed voltage reference circuit desig

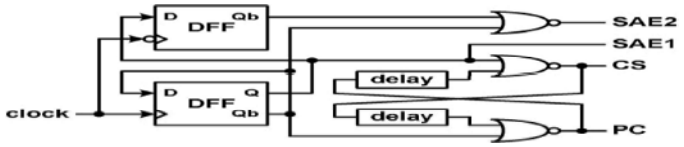

Fig. 5: Digital control unit

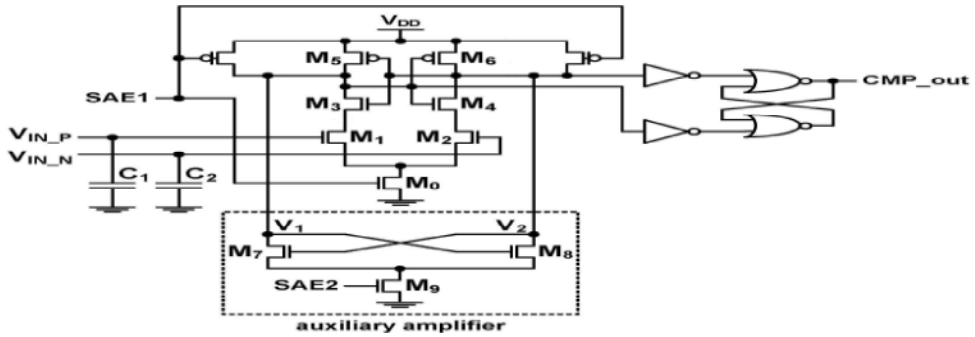

Fig. 6: Low voltage comparator schematic

the pull-down current of the cross-coupled latch is very weak. The auxiliary amplifier (M_7-M_9) pulls node V_1 or V_2 down during the second amplifying operation. The comparator with auxiliary amplifier however increases the sensing speed with its rapid voltage amplification.

Charge Pump Circuit: The proposed charge pump circuit as shown Fig. 7 adjusts the gate voltage according to the comparator output value (CMP_out).

Initially, V_G is discharged to the ground by a positive pulse startup signal. Transistors M_3, M_4 and M_5 in Fig. 7 begin to flow currents I_1, I_2 and I_3, respectively. Two input voltages of the comparator (i.e., V_{IN_N} and V_{IN_P}) increase to near V_{DD}. After the start-up operation, the charge-pump circuit changes V_G slightly every clock cycle. At the precharge (PC) phase, node V_{CAP} is connected to the ground by the PC signal and node V_{DRV} is connected to the ground or V_{DD} according to the comparator output. At the charge-sharing (CS) phase, node V_{CAP} is connected to node V_G by the CS signal and V_{DRV} changes from the ground to V_{DD} or from V_{DD} to the ground. Output reference voltage V_{REF} is controlled by V_G.

Fig. 8 shows the schematic of the proposed volage reference and the simulation result is shown in Fig. 9 and Fig. 10. The proposed voltage refere is given by 600mV clock pulse and it is going to generate required control signals for producing the reference voltage. This proposed method produces 274 mV reference voltage at 374 mV and it requires 250mV minimum supply voltage.

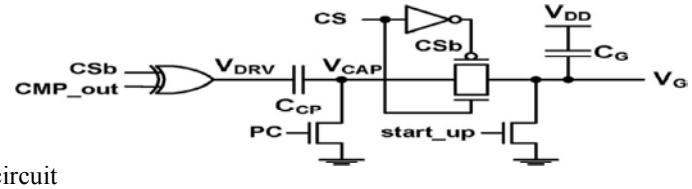

Fig. 7: Charge pump circuit

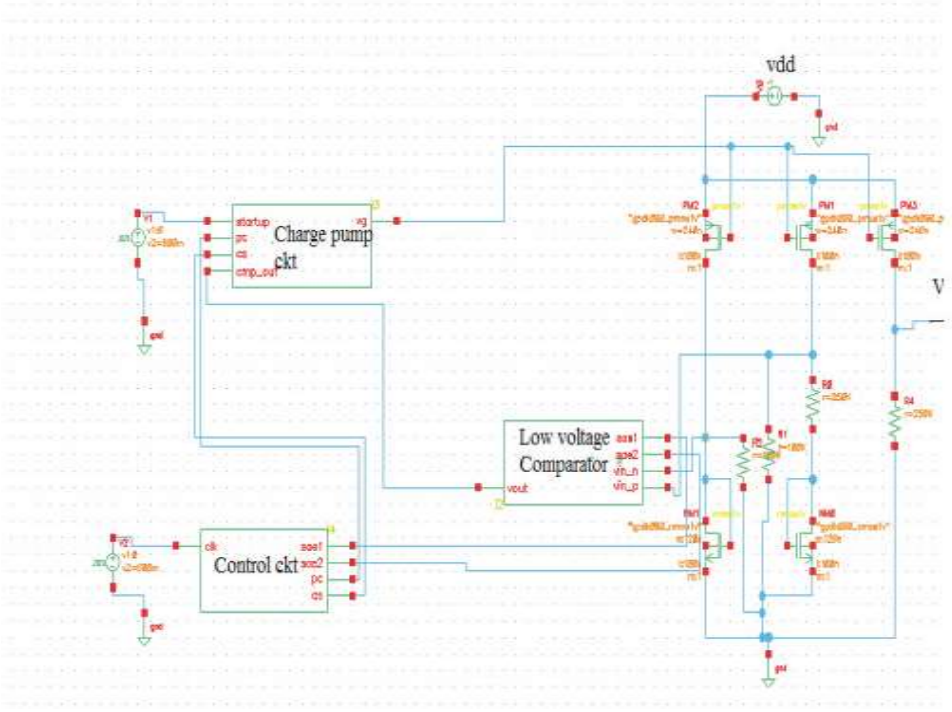

Fig. 8: Proposed Subthreshold CMOS voltage reference circuit

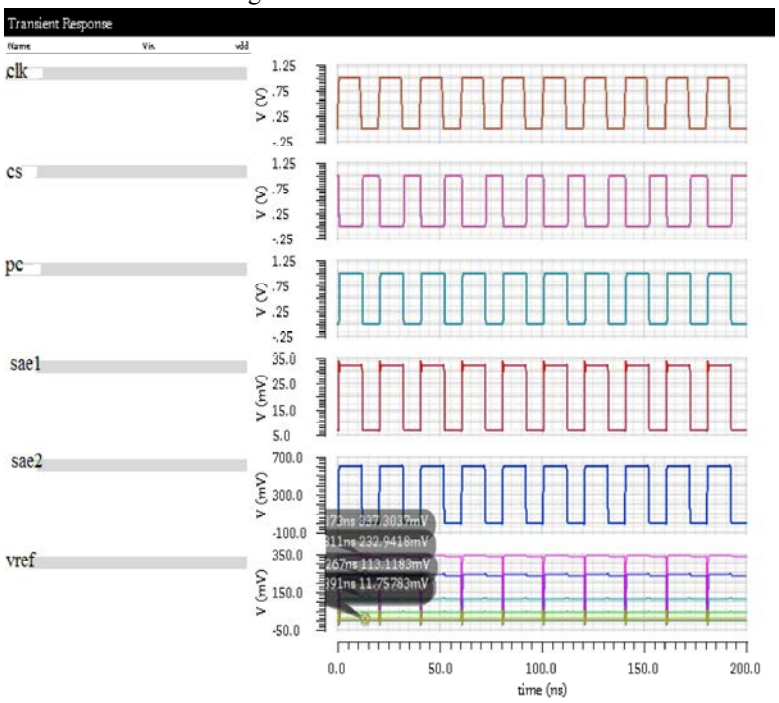

Fig. 9: Transient response of proposed voltage reference

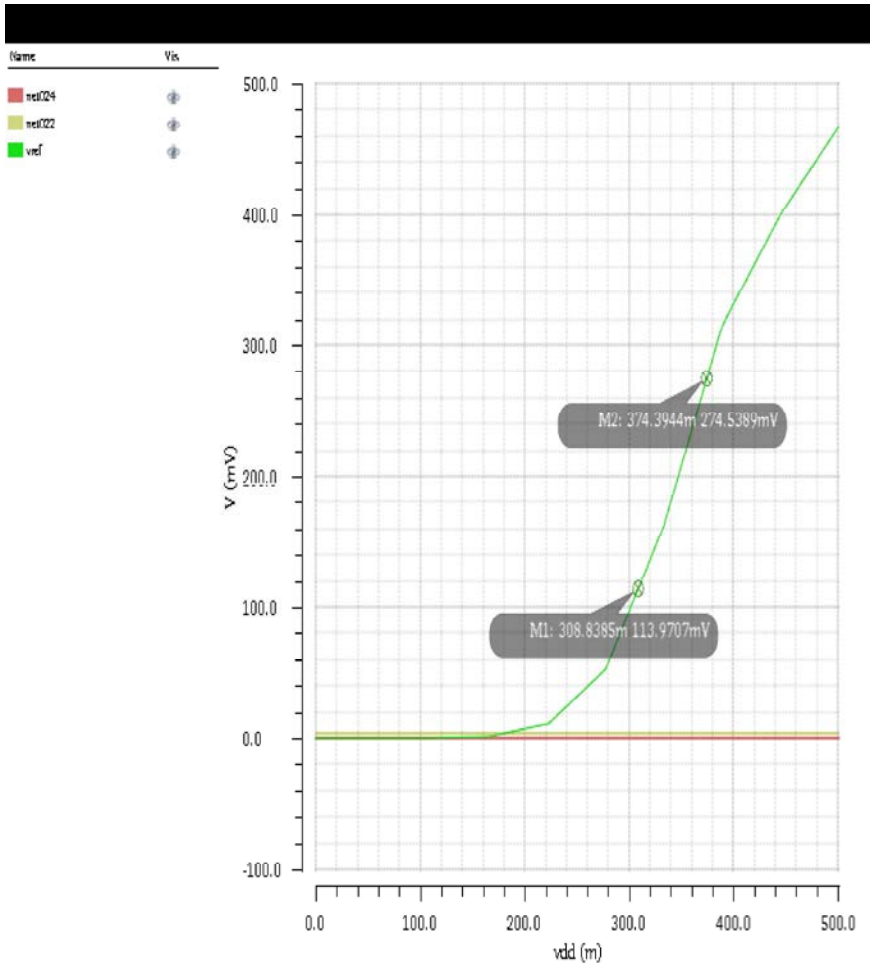

Fig. 10: Variation of supply voltage vs reference voltage

Table 1: Comparsions of Low-voltage Voltage References

	Conventional	Proposed
Process (nm)	90	90
Power (µw)	7.33	5.35
V_{DD}	472	374
V_{REF}	274	274

Flash ADC: Flash ADCs (sometimes called parallel ADCs) are the fastest type of ADC and use large numbers of comparators. The input signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input and the encoder N-bit output by only a few gate delays on top of that, so the process is very fast. An N-bit flash ADC consists of 2^N resistors and 2^N–1 comparators arranged as in Figure Fig 1. Each comparator has a reference voltage which is 1 LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point will have their input voltage larger than their reference voltage and a "1" logic output and all the comparators above that point will have a reference voltage larger than the input voltage and a "0" logic output.

Comparator: The low power comparator circuit used in the design of Flash ADC is shown in Fig. 12. This circuit uses a preamplifier and a positive feedback stage. In the preamplifier stage to achieve an acceptable gain the input differential pair uses NMOS transistors and the load uses PMOS transistors. Positive feedback stage determines which input signal is larger. Output buffer stage amplifies this information and gives digital signal. simulation result of low voltage comparator is shown in Fig. 13.

Priority Encoder Design: This is a multiplexer based encoder which converts thermometer codes to binary codes. The multiplexers used are designed using transmission gates for better accuracy.

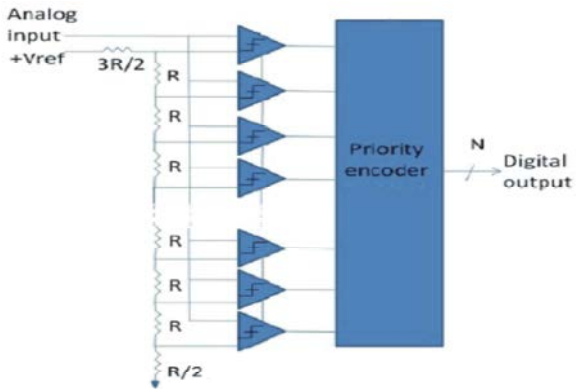

Fig. 11: N-bit Flash ADC

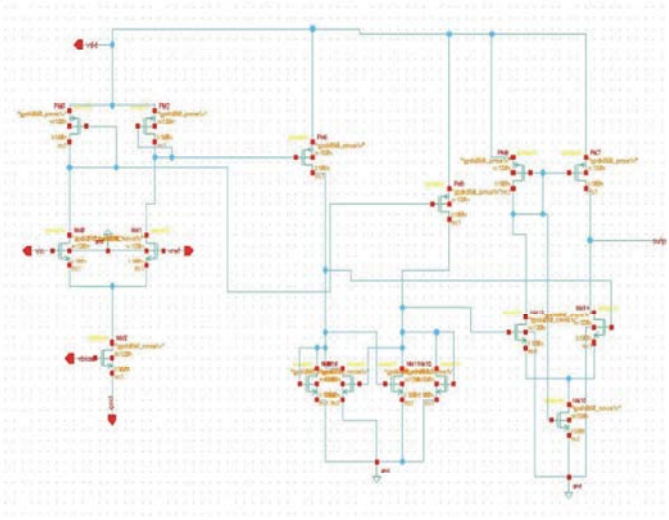

Fig. 12: Schematic of Comparator

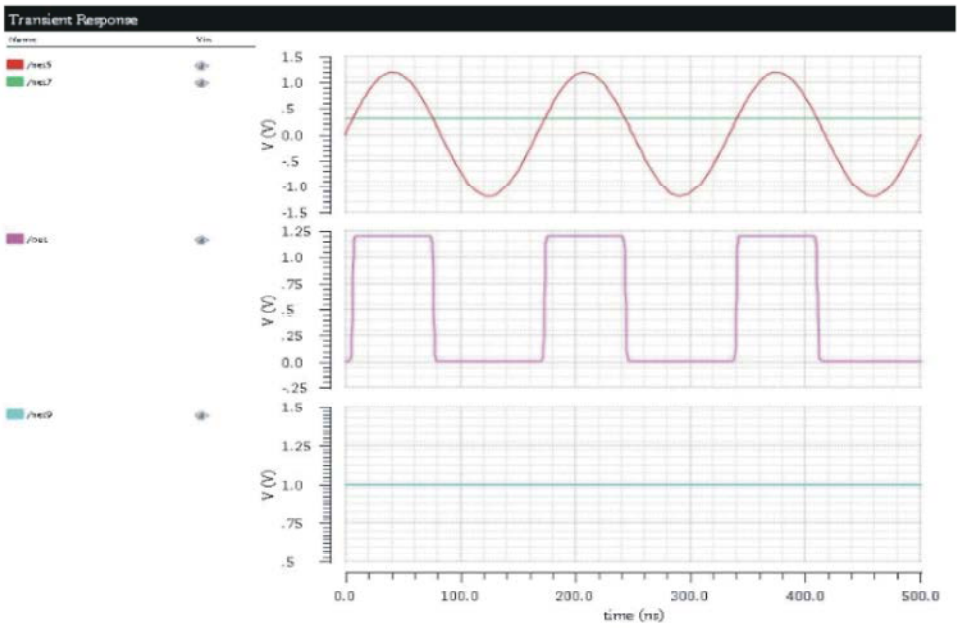

Fig. 13: Transient Response of Comparator

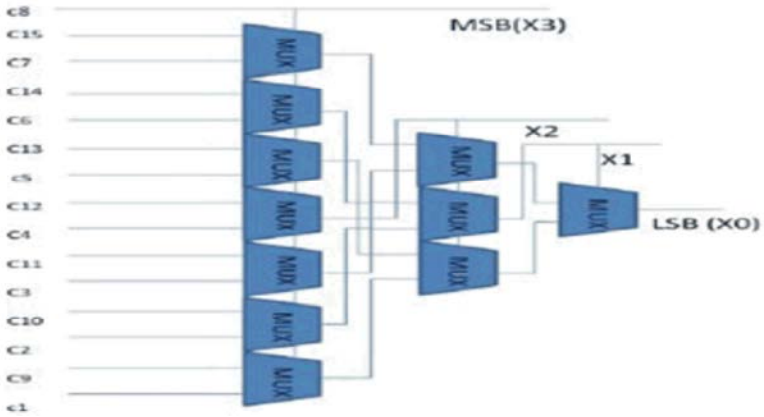

Fig. 14: Priority encoder design

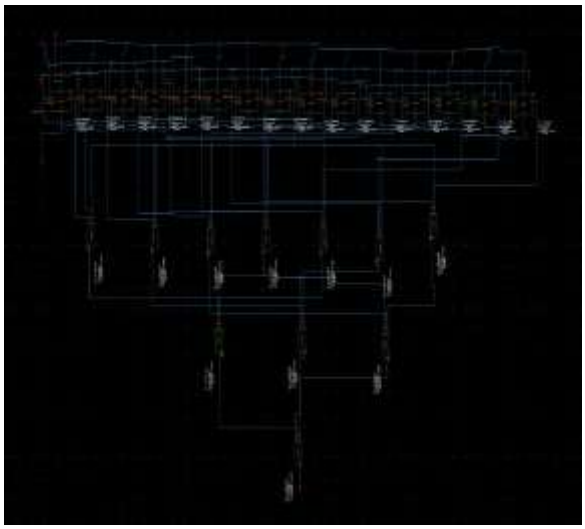

Fig. 15: 4 bit Flash ADC schematic

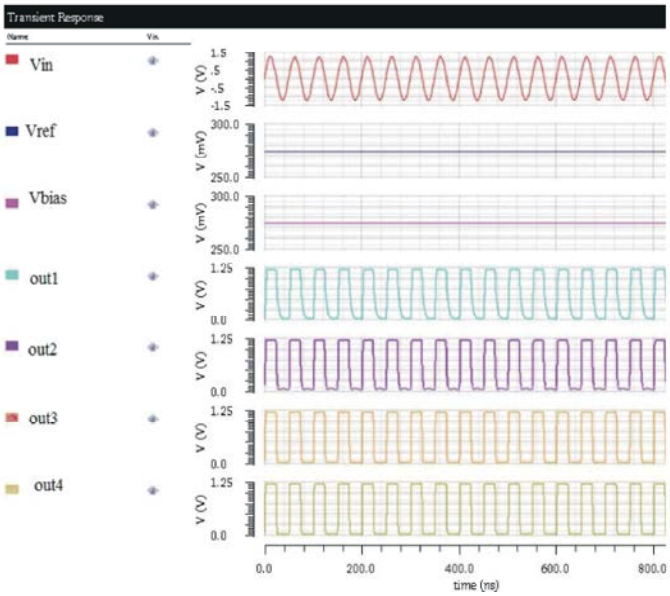

Fig. 16: Simulation result of 4 bit Flash ADC

Table 2: Parameter Values of 4 BIT Flash ADC IN 90 nm

Resolution	Frequency	Power dissipation	Conversion time
4 bit	6 Mhz	6.943 mW	6.182 nS

The schematic of 4 bit Flash ADC is designed in 90nm CMOS technology by using Cadence virtuoso and it is integrated with the proposed reference voltage design. The simulation result of 4 bit Flash ADC is shown in Fig. 15 and Fig. 16.

CONCLUSION

The problem of flash ADCs lies with limited resolution, high power dissipation because of the large number of high speed comparator. In this regard we have made an attempt to design a low-power 4bit ADC. The design and simulation are carried out in 90nm CMOS technology by using Cadence virtuoso. This ADC is integrated with the proposed reference voltage circuit, which requires 20% less supply voltage and consumes 27% less power as shown in Table.1.From Table.2 it can be concluded tis 4 bit Flash ADC can be used in low power and high speed applications.

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