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Implementation of Cascaded H-Bridge Multi Level Inverter

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Abstract: Multilevel inverter is a power electronic device that has become more popular in electric high power and medium voltage applications. Multilevel inverters have unique structure which makes it possible to reach high voltages with fewer harmonics content and lower Electromagnetic interference (EMI). The harmonic content of the output voltage waveform reduces as the number of output voltage increases. This paper proposed a three-phase cascaded multilevel inverter using less number of switches. The proposed system uses the topology of Asymmetrical cascade H-Bridge Multilevel inverter with separate not equal dc sources for the switching circuit. As the number of step level for voltage increases in the output voltage waveform has more steps, this produces a desired output waveform with low harmonic distortion. Application of cascaded multilevel inverter for high power equipments in industry has become popular because of its high-quality output waveform. The method has been designed as a twenty seven level three phase cascaded multilevel inverter and compares the Total harmonic distortion. The models discussed in this paper have been simulated on Matlab/Simulink software and the relevant Total harmonic distortion (THD) has been determined by Fast Fourier Transformation (FFT) analysis of the output waveform by the software.

Key words: Multilevel Inverters · Total Harmonic Distortion · H-Bridge · Fast Fourier Transform

INTRODUCTION

The developments in power electronic devices and semiconductor technology have triggered improvements in power electronic systems. So, dissimilar circuit configurations like multilevel inverters have become popular and considerable interest by researchers are being given on them. The output voltage waveforms in multilevel inverters can be generated at low switching frequencies with low alteration and elevated frequency. The concept of multilevel inverters has been introduced since 1975. The cascaded multilevel inverter was first introduced in 1975. Separate DC-sourced full bridge cells were placed in series to synthesize a staircase AC output voltage. In 1992, capacitor-clamped (or flying capacitor) multilevel inverters and in 1996, cascaded h-bridge multilevel inverters were proposed [3]. The first ever introduced topology is the series H-bridge design [1]. This H-bridge inverter was followed by the diode-clamped inverter [2-4] which utilizes a bank of series capacitors to divide the dc bus voltage. Hybrid multilevel converters have been offered in [5], [6].

In the hybrid topologies, the degrees of dc voltage sources are unequal or altered dynamically depending upon the need [7]. These converters are very capable in the size and cost and improve the reliability since less number of semiconductors and capacitor is use in this topology [8]. The hybrid multilevel converters consist of altered multilevel topologies which are having uneven value sources of dc voltage magnitude and different modulation techniques [9]. With appropriate mixture of switching devices and technique, the converter cost is reduced Although the cascade multilevel inverter was pretend previously, its application did not prevail until the mid 1990s.The advancement in the pitch of power electronics and microelectronics made it probable to reduce the degree of harmonics with multilevel inverters, in which the number of levels of the inverters are increased fairly than increasing the size of the filters. The performances of multilevel inverters enhance as the number of levels of the inverter increases. The imaginary higher bound that is achieve for an in?nitely high switching frequency is practically quite accurate for the ratios of switching and fundamental frequencies that are

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higher than 25-30 and is suitable for both single and three-phase inverters [11]. The theoretical voltage quality lower bound is achieved for a low amount of synchronous switching that is formerly between any two adjacent voltage levels [12, 13].

This paper presents a three-phase cascaded multilevel inverter is using less number of switches. The proposed system uses the topology of Asymmetrical cascade H-Bridge Multilevel inverter with separate unequal dc sources for the switching circuit. As the number of step level and voltage increases in the output waveform has more steps, which produce a desired output waveform with low harmonic distortion. Application of cascaded multilevel inverter for more power equipments in industry has become popular because of its high-quality output waveform. The method has been designed as a twenty seven level cascaded multilevel inverter and the Total harmonic distortions are compared.

Multilevel Inverters: The unique structure of voltage source inverters allows them to reach high voltages with low harmonics without the use of series-connected synchronized switching devices or transformers. The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries and renewable energy voltage sources can be used as the multiple dc voltage sources The simplest techniques involve the parallel or series connection of conventional converters to form the multilevel waveforms. More complex structures effectively insert converters within converters.

The voltage or current rating of the multilevel converter becomes a multiple of the individual switches and so the power rating of the converter can exceed the limit imposed by the individual switching devices. Several multilevel inverter topologies have been developed; i) diode clamped, ii) flying capacitors and iii) cascaded or H-bridge. Referring to the literature reviews, the cascaded or H-bridge multilevel inverter with separated DC sources is clearly the most feasible topology for use as a power converter for medium & high power applications. For a single phase seven-level inverter, twelve power electronic switches are required in both the diode-clamped and the flying capacitor topologies. Uneven voltage innovation is utilized as a part of the cascaded H-bridge multilevel

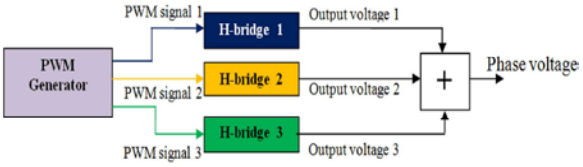

Fig. 1: Block diagram of three phase H-bridge multilevel inverter

inverter to permit more levels of output voltage, so the cascaded H- bridge multilevel inverter is appropriate for applications with expanded voltage levels. Two H- bridge inverters with a dc voltage of numerous connections can be associated in cascade to create a single stage seven-level inverter and eight power electronic switches are utilized.

The PWM generator generates three PWM signals for three H-bridge cells per phase. Each H-bridge produces its output voltage according to the applied PWM signal. The obtained phase voltage is the sum of these three output voltages. The PWM signals are exchanged between the H-bridges every cycle of the modulation signal (0.02sec). After three cycles, the process is repeated; (a) the first state where PWM signal is applied to the H-bridge 1, PWM signal 2 is applied to H-bridge 2 and PWM signal 3 is applied to H-bridge 3. (b) The second state where PWM signal 3 is applied to H-bridge 1, PWM signal 1 is applied to H-bridge 2 and PWM signal 2 is applied to H-bridge 3. (c) The third state where PWM signal 2 is applied to H-bridge 1, PWM signal 3 is applied to H-bridge 2 and PWM signal 1 is applied to H-bridge 3.The basic block diagram of the three phase H-bridge multilevel inverter is shown in Figure 1.

Cascaded H-bridge Inverter: The converter topology is based on the series connection of single-phase inverters with separate dc sources. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. In order to solve the problem of unbalanced switching of the H-bridge cells, the equal switching distribution method is proposed. The method uses the operation principle of the multilevel inverter the control unit of the inverter generates the desired PWM signals that are applied to the H-bridge cells; each H-bridge cell produces its own output voltage according to the applied PWM signal. There are three H-bridges that receive three PWM signals per phase. The proposed

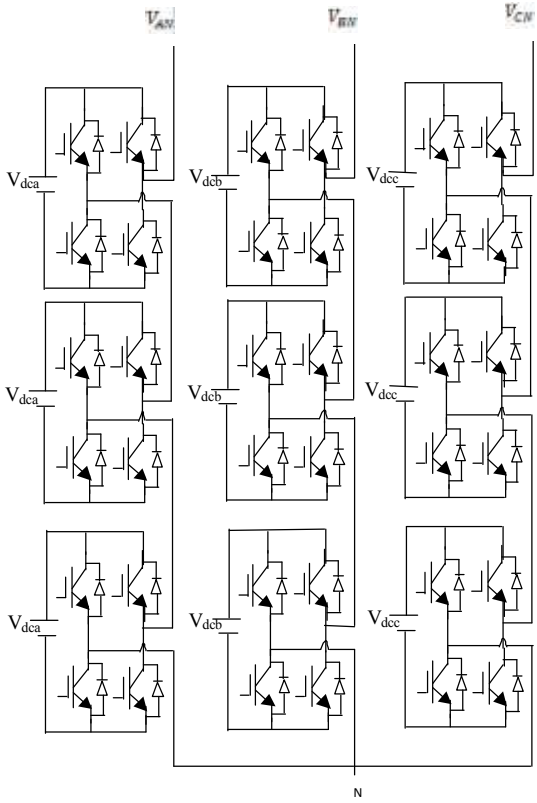

Fig. 2: Three phase structure of a cascaded H-bridge inverter

equal switching distribution method periodically exchanges these three PWM signals between the three H-bridge cells.

Figure 2 shows a three phase structure of cascaded H-bridge inverter with separate dc source. In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: $+V_{dc}$, 0, $-V_{dc}$ (zero, positive dc voltage and negative dc voltage). This is made possible by connecting the capacitors sequentially to the ac side via the power switches. The resulting output ac voltage swings from-V_{dc} to $+V_{dc}$ with three levels, -2 V_{dc} to +2 V_{dc} with five-level and -3 V_{dc} to +3 V_{dc} with seven-level inverter. The staircase waveform is nearly sinusoidal, even without filtering. For a three-phase system, the output of three identical structure of single-phase cascaded inverter can be connected in either star or delta configuration. The three phase cascaded multi level inverter using three H-bridge cells and three separate dc sources per phase.

From Figure 3 V_{an} is voltage of phase A, which is the sum of V_{a1}, V_{a2} and V_{a3}. The same method is applied to phase B and phase C. To synthesize seven-level phase voltage, three firing angles are required. The same three switching angles can be used in all the three phases with delaying 0, 120 and 240 electrical degrees for phase A, B and C respectively.

According to the phase theory, line voltage can be expressed in term of two phase voltages. The potential difference between phase A and B is V_{ab}, which can be written as follows,

$$V_{ab} = V_{an} - V_{bn} \quad (1)$$

V_{ab} is line voltage
V_{an} is phase A voltage with respect to point N and
V_{bn} is phase B voltage with respect to point N

Theoretically, the maximum number of line voltage levels is 2m-1, where m is the number of phase voltage levels. The number of line voltage level depends on the modulation index and the given harmonics to be eliminated. The seven-level cascaded inverter, for example, can synthesize up to thirteen-level line voltage.

The advantage of three-phase system is that all triplen harmonic components in the line voltage will be eliminated by one-third cycle phase shift feature. Therefore, only non-triplen harmonic components need to be eliminated from phase voltage. In single phase nine-level waveform, for example, the 3rd, 5th and 7th harmonics will be eliminated from output phase voltage. Compared to single-phase inverter, in three-phase nine-level inverter, the 5th, 7th and 11th harmonics will be eliminated from output phase voltage. Thus, the 9th harmonic is the lowest harmonic component in phase voltage in single phase system, while the 13th harmonic is the lowest harmonic component appearing inline voltage of three-phase system.

Advantages

- The regulation of the DC buses is simple.
- Modularity of control can be achieved. Unlike the diode clamped and capacitor clamped inverter. Where the individual phase legs must be modulated by a central controller, the Full-bridge inverters of a cascaded structure can be modulated separately.
- Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.
- Soft-switching can be used in this structure to avoid bulky and lossy resistor Capacitor-diode snubbers.

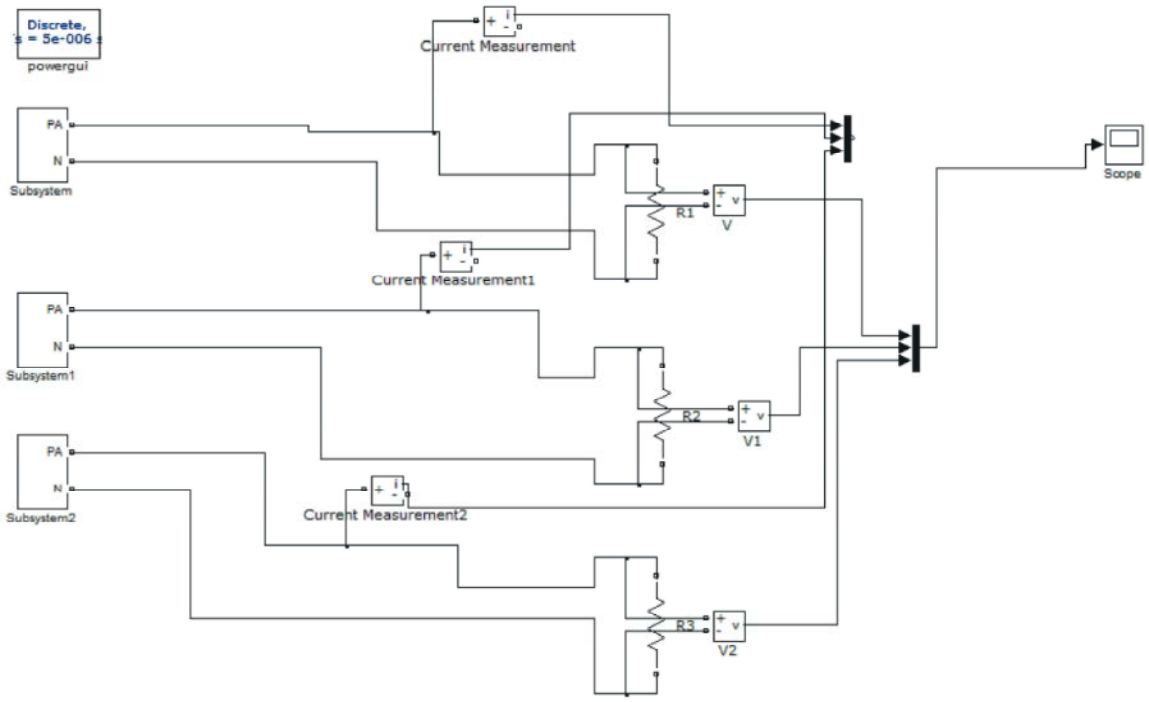

Fig. 3: Simulink model of 27-level inverter

- Higher voltage levels can be obtained, thus eliminating the need for costly, bulky and Weighty transformers.
- Lower harmonic distortion with increase in the number of DC voltage levels, thus leading to a lower requirement for output filter.

Modelling of Single Phase Multilevel Inverter: A single phase twenty seven level is an asymmetrical multilevel inverter that has three H-bridge with unequal DC voltage source. Each H Bridge has four switches.

$$V_{oi} = V_{dc} (S_{1i} - S_{2i}) \quad (1)$$

where i=1, 2, 3 (number of H-bridge inverter).

For twenty seven level inverter DC voltages are inverter of 1vdc, 3vdc and 9vdc.

Simulation Results: The feasibility of the proposed approach is verified using computer simulations. A model of the three phase multi-level inverter topology is constructed in MATLAB-Simulink software. A new strategy with decreased number of switches is employed. The new multilevel inverter topology works well and shows hope to reduce the initial cost and complexity. The proposed circuit generates a high-quality output voltage waveform and harmonic components of output voltage and current are low. It can also be extended to any number of levels when compared to conventional cascaded H-bridge multilevel inverter The functionality verification of the three phase multi level inverter topology is done using MATLAB.

The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter and can be extended to any number of levels. The schematic of the three-phase cascaded H bridge inverter with proposed topology built in MATLAB-Simulink and the results are well within the results of both output voltage and FFT analysis are verified by simulating the main circuit using MATLAB.

The Matlab/Simulink model three phase cascaded multi level inverter using nine H-bridge is shown below in Figure 3.The inverter uses a standard three-leg inverter and an H-bridge with its DC source in series with each phase leg. To see how the system operates, consider simplified single phase topology, shown in Figure 4. The output voltage 1 (3v) of this first leg of the top inverter is goes to ON state. For a negative half cycle this leg is connected in series with a full H-bridge, which, in turn, is supplied by a supply voltage. If the supply is kept charged to V_{dc} /2, then the output voltage of the H-bridge can take on the values + V_{dc}/2.

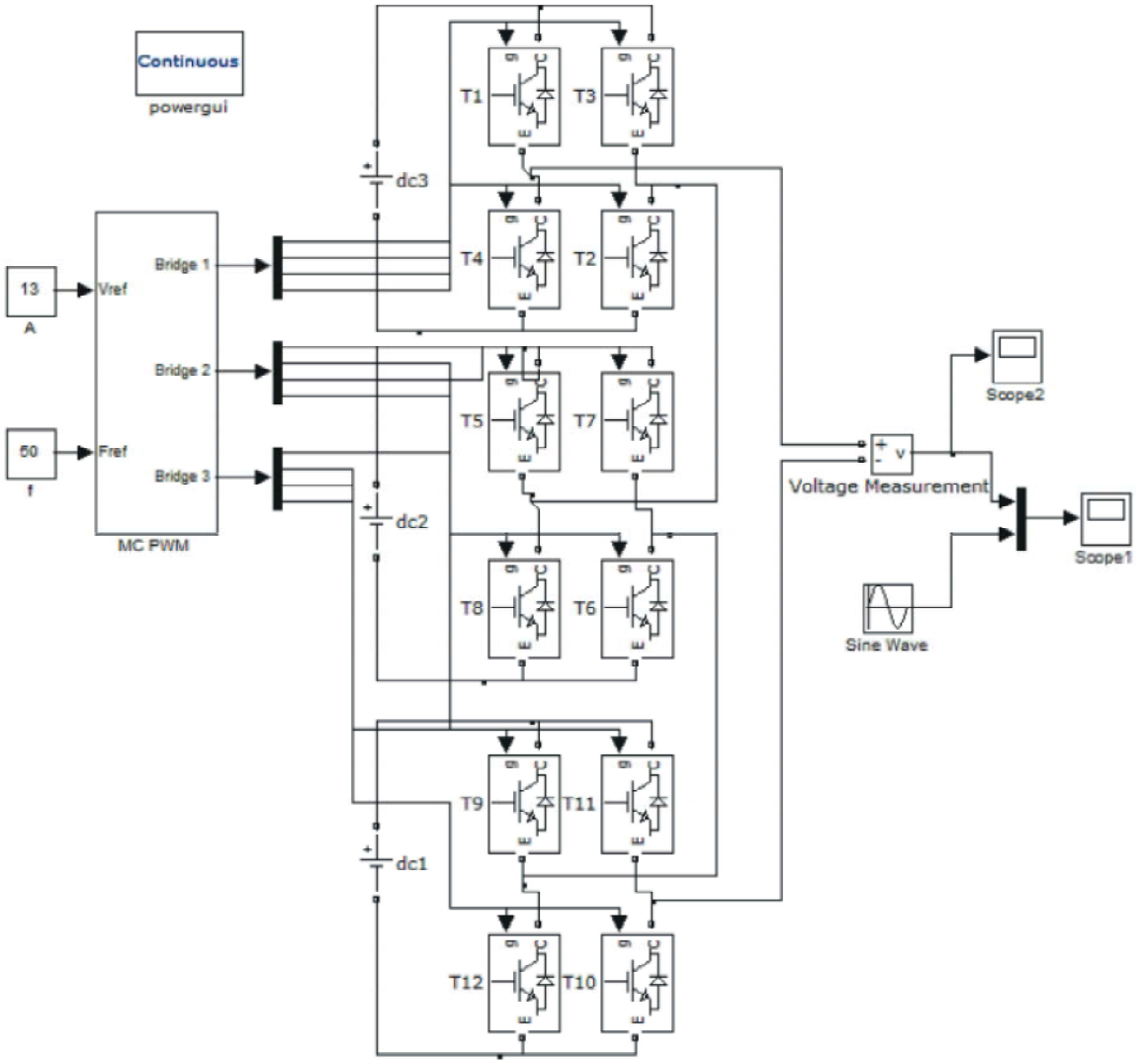

Fig. 4: Subsystem of single phase cascaded multilevel inverter

I have created subsystem for single phase cascaded H-bridge multilevel inverter and used the subsystems to avoid clutter in the workspace. The Matlab/Simulink model for single phase cascaded multilevel inverter using three H-bridges is shown below in Figure 4.

In this cascaded H-bridge inverter, it has three voltage sources as an input to the three H-Bridges are connected in series like in the proposed method of the inverter. Each H-bridge has Semiconductor switches like IGBT or MOSFET or any other semiconductor devices. In this proposed model four MOSFET switches are used for each H-bridge. In this H-bridge the two semiconductors are switched for one half cycles either positive or negative. The traditional two or three levels inverter does not completely eliminate the unwanted harmonics in the output waveform. When the number of levels increases, the total harmonic distortion decreases significantly.

This proposed method produce the pulses using Matlab/Simulink multi controller pulse width modulation for twenty seven level asymmetrical cascaded multilevel inverter. Each H-bridge inverter can produce 27 different voltages, the output levels are $13V_{dc}$,$12V_{dc}$, $11V_{dc}$, $10V_{dc}$, $9V_{dc}$, $8V_{dc}$, $7V_{dc}$, $6V_{dc}$, $5V_{dc}$, $4V_{dc}$, $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$, $-4V_{dc}$, $-5V_{dc}$, $-6V_{dc}$, $-7V_{dc}$, -8Vdc, $-9V_{dc}$, $-10V_{dc}$, $-11V_{dc}$,$-12V_{dc}$, $-13V_{dc}$. The switching for one positive cycle is as s_1, S4 and S5, S8 and S9, S12 this method is adopted to protect the increase the level of the inverter to obtain sinusoidal waveform.

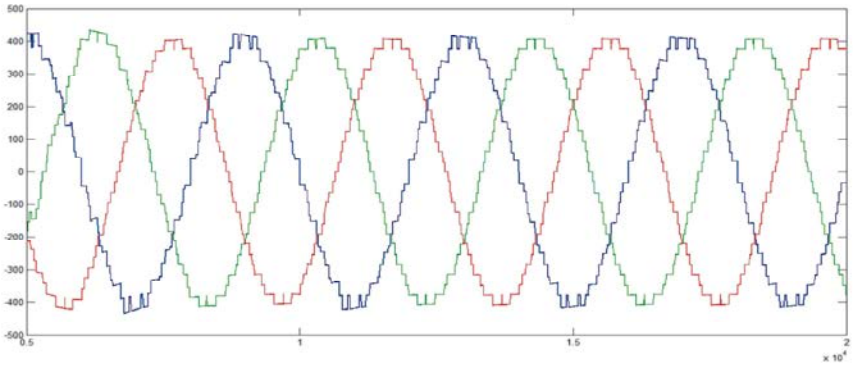

Fig. 5: Output voltage of 27-level inverter

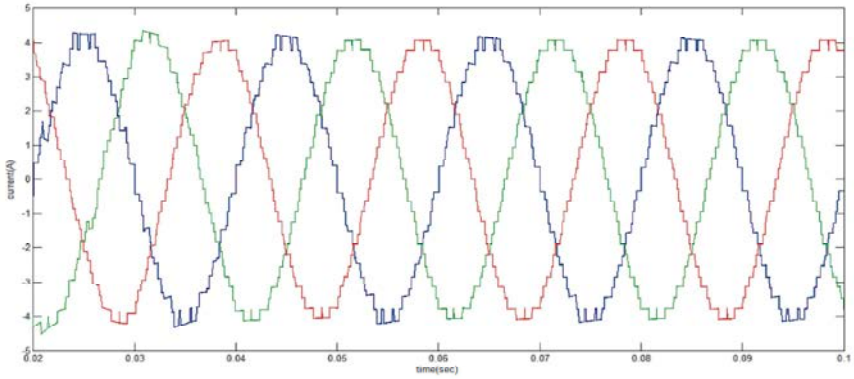

Fig. 6: Output current of 27-level inverter

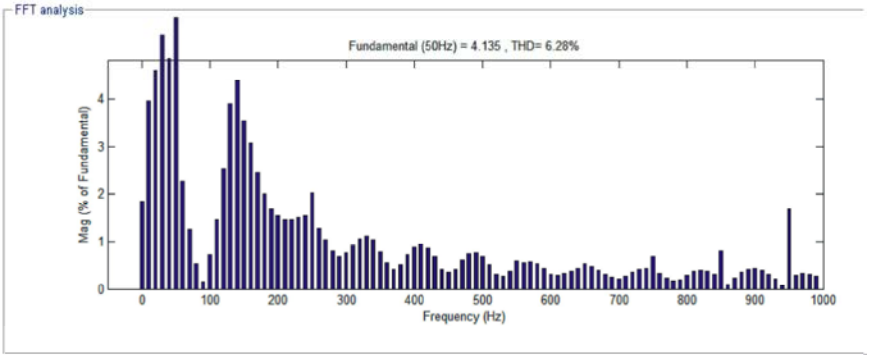

Fig. 7: FFT spectrum of three phase 27-level inverter for R-phase voltage

The Phase Shifted PWM all the triangular carriers have the same frequency and same peak-peak amplitude. But there is a phase shift between any two adjacent carrier waves. For m Voltage levels (m-1) carrier signals are required and they are phase shifted with an angle of θ = (360°/m- 1). The gate signals are generated with proper comparison of carrier wave and modulating signal. In general, a multilevel inverter with m voltage levels requires (m-1) triangular carriers In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by PhCR = 360°/(m-1).Simulation results of proposed 27 Level cascaded h-bridge multi level inverter output voltage is shown in Figure 5.

Simulation results of three phase cascaded h-bridge twenty seven level inverter output current is shown in Figure 6.

The Total Harmonic Distortion of a three phase cascaded twenty seven multilevel inverter was analyzed by Fast Fourier Transformation method (FFT).

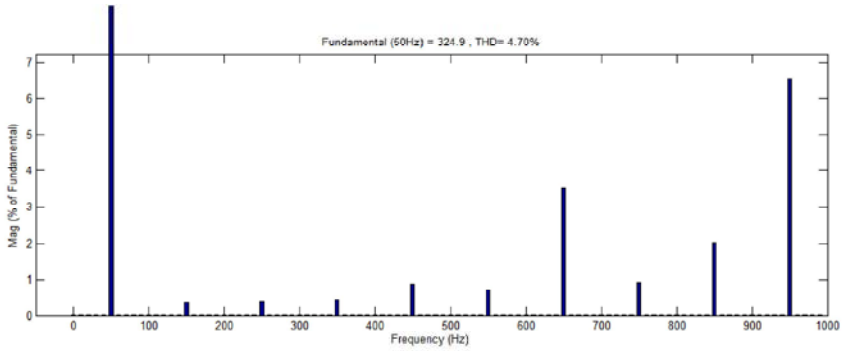

Fig. 8: FFT spectrum of three phase 27-level inverter for R-phase current

The R-phase FFT analysis is carried out for output voltage to study the reduction in harmonics and corresponding spectrum is shown above in Figure 7. THD of output voltage of the proposed three phase cascaded H-bridge multilevel inverter is 6.28%. The corresponding output current is measured to study the harmonics and the corresponding spectrum is shown in figure 8.THD of the output current of the proposed three phase cascaded H-bridge multilevel inverter is 4.70%.

CONCLUSION

This paper presents a three-phase cascaded multilevel inverter using less number of switches. The proposed system used the topology of Asymmetrical cascade H-Bridge Multilevel inverter with separate unequal dc sources for the switching circuit. As the number of step level and voltage increases in the output waveform has more steps, which produces a desired output waveform with low harmonic distortion. It is designed to generate ac output of twenty seven levels three phase and nine h-bridges are used with three unequal distributed dc sources. The simulations of twenty seven level inverters are carried out in MATLAB/SIMILINK. The three phase cascaded H-bridge gives output voltage THD of 6.28%. The above results clearly indicate that as the output Voltage levels are increased, the THD of the system decreases. The simulation results and FFT analysis results verified the three phase H-bridge multilevel inverter.

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