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Design of a Novel 16-Bit Compact Carry Save Adder by using GDI Logic for Low Power and Low Area Applications

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Abstract: Design of a digital circuit with small chip size and low power is achieved by using Complementary Metal Oxide Semiconductor (CMOS) technology. This technique is divided into Dynamic CMOS technique and Static CMOS technique. Equal number of NMOS (Pull down) and PMOS (Pull up) transistor are used to design the circuits in the static CMOS technique. So area and power is high. But in the GDI (Gate diffusion input) logic, VDD (supply voltage) and ground can be used as one of the input terminal to reduce the number of transistors. Digital Adder design is the major step in the field of Communication, DIP, DSP, Micro controllers and Microprocessors to perform the ALU(arithmetic and logical) operation. In this work, the design of compact carry save adder (CCSA) using CMOS GDI logic is presented for FIR filter. The design of MUX, XOR and, OR gates in a way that each gate 5 transistors instead of 6 transistors and hence reduced Half adder with 11 transistors are integrated into carry save adder to reduce the power dissipation and area than the existing carry save adder. This carry save adder is designed using Tanner14.11 to examine the power consumption, area and to check this adder functionality.

Key words: Static CMOS logic · CMOS GDI logic · Reduced logic gates · Compact carry save adder and tanner tool

INTRODUCTION

CMOS technology is important in very large scale integration (VLSI) for integrating huge number of circuit into single silicon chip. Nowadays, the compact product is designed to reduce the area and power consumption. The transistor size reduces in every year based on Moore law to design the compact product. If the transistor size is decreased, we can include more number of transistors into only one chip. Different kind of CMOS technologies is applied from 250nm to 45nm so as to reduce the transistor length and width based on lamda rule. The transistor size is reduced by using nano meter technology. In day today life, the Systems on Chip (SoC) product are essential. Millions of chip integrated into one single platform is called as SoC. These millions of chips are incorporated into single chip by reducing the transistor size in each and every chip. Consequently this CMOS technique may apply in SoC product [1].

Carry Select Adder (CSLA) is mostly used to diminish the chip size and for sinking the propagation delay. This kind of carry select adder provides small delay and low area when compared to Ripple carry adder, carry save adder, carry look ahead adder and carry skip adder, [2]. Different types of carry select adder constructions are presented in the existing techniques. The reduction of delay, area and power in digital adder circuits is very important for ALU. The sum of each and every bit location in digital adder is created serially only behind the previous bit location has been summed and a carry output pass into the next position [3].

The existing carry-save adder is a kind of digitaladder, used in computer micro architecture to calculate the sum of three or more *n*-bit numbers in binary [4]. It differs from other digital adders in a way that it outputs two numbers of the same dimensions as the inputs, one which is a sequence of carry bits and another which is a sequence of partial sum bits.The proposed carry save adder is designed with optimized half adder, full adder and, OR, XOR gates and BEC(Binary to excess1 code) converter to achieve the low area and low power. This type of adder has been designed in this paper in two ways.

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The Gate Diffusion Input (GDI) method is proposed in 2002 to reduce the power consumption and chip size of VLSI digital circuits [5]. The GDI logic was originally proposed for fabrication in Silicon on Insulator (SOI) and twin-well CMOS methods [6]. It allowed the implementation of a broad range of difficult logic functions using simply two transistors. This scheme was appropriate for the design of regular digital circuits, with a much lower area than existing PTL (pass transistor logic) and Static CMOS methods, whereas offering improved power characteristics. Equally to PTL implementations, the GDI circuits suffered from a decreased swing since of threshold drops. Equally, a considerably shriveled the logic flexibility and transistor count of the basic GDI cell, provides major power reduction, in spite of the need for swing restoration circuits [7].

The GDI cell consists of P (input to the source/drain of PMOS transistor), N (input to the source/drain of NMOS transistor) andG (common gate input of NMOS and PMOS transistors) [8]. The GDI method was very efficient for both combinational and sequential logic implementation in comparatively ancient CMOS methods. A variety of combinatorial circuits, for example comparators, multipliers, adders and counters, were executed in methods from 250nm down to 45nm, illustrating a power reduction of up to 40%. The main goal of the paper is to design the compact carry save adder based on GDI logic to reduce the power consumption and number of transistors than the all other existing carry adder circuits.

This article is scheduled as follows: Section 2 deals with the design of existing carry save adder by using static CMOS. Design of compact carry save adder with reduced logic gates, reduced full adder and half adder structure by using GDI logic is presented in section 3. Section 4 demonstrates the results and discussion. Section 5 describes the information about conclusion of this research work.

Existing Carry Save Adder: The existing carry save adder is designed using ripple carry adder (combination of half adder and full adder) in the first stage, binary to excess1 code converter and 2:1 multiplexer in the second stage. Structure of existing carry save is shown in Fig. 1. Static CMOS logic is used in the existing carry save adder. This AND gates are designed using 6 transistors: 3 NMOS transistors and 3 PMOS transistors. Similarly OR gate is constructed using 6 transistors. The existing XOR gate is designed by using 12 transistors [9].

Regular carry save adder utilize large propagation delay. To overcome this problem, the existing carry save adder c4-c13 and x14-x17 are given in parallel to achieve high speed and reducing the clock cycles. Binary to excess1 code converter is used to generate the given input into incremented by one as shown in fig.2. Tanner tool 14.11 is used to design the carry save adder. Static CMOS logic is applied for all the gates and adders in the existing CCSA [10].

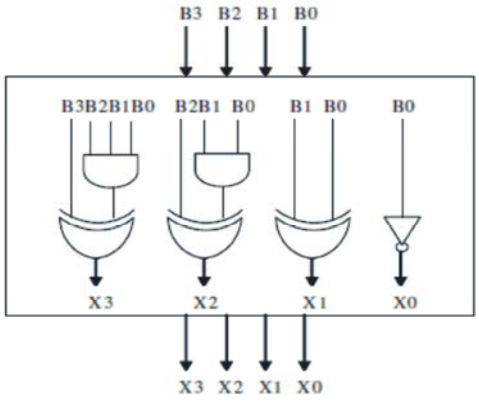

Fig. 1: Circuit diagram of existing carry save adder

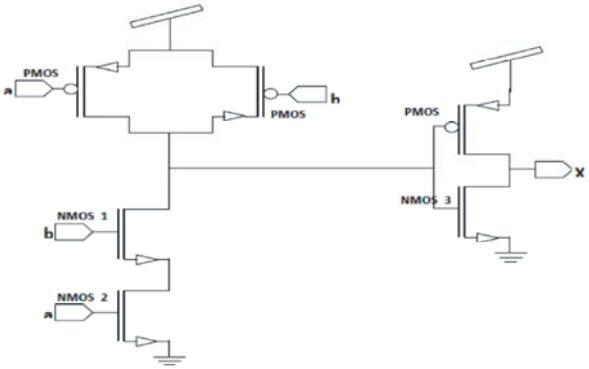

Fig. 2: Circuit diagram of BEC

In the existing AND gate, NMOS_1 and NMOS_2 are connected in serious andPMOS_1 and PMOS-2 (inputs a & b) are connected in parallel. This last output are inverted for AND operation as shown in Fig. 3. Entirely it needs 6 transistors. X is the final output of existing AND gate. If the inputs a & b inputs are zero, PMOS_1 and 2 are on (one or high) and NMOS_1 and 2 is off. Hence the PMOS output is connected to the inverter. Hence the AND gate output is 0. If the inputs a and b values are one, only NMOS_1 and 2 is on. It is joined to the ground Zero value. The Zero output is given into inverter to generate the final output of AND gate as 1. Likewise all other inputs are passed to generate the final output.

Similarly, OR and XOR gate inputs is given and produced the corresponding output by using static CMOS logic as shown in Fig. 4 [11].

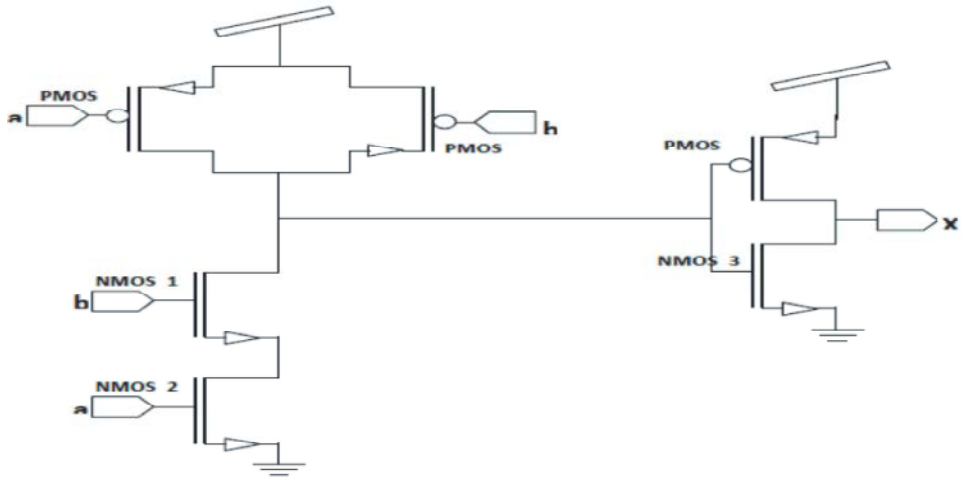

Fig. 3: Circuit diagram of existing AND gate using static CMOS logic

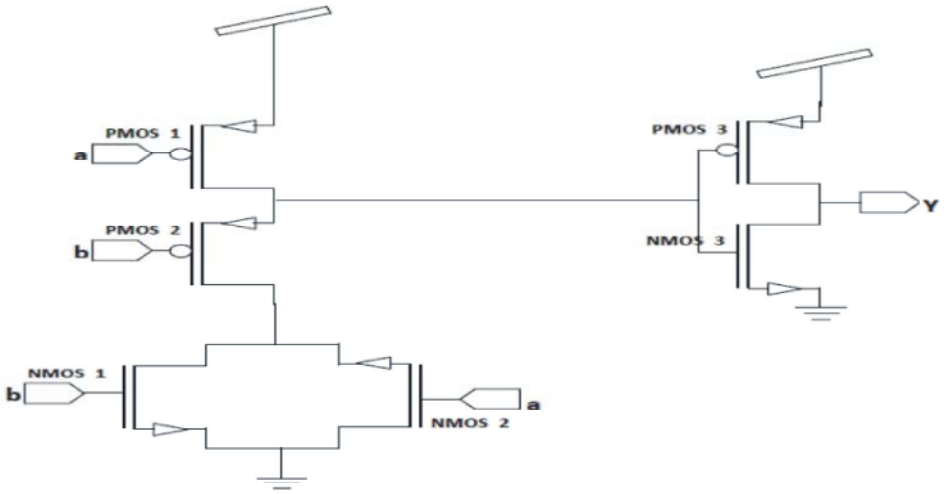

Fig. 4: Circuit diagram of existing OR gate using static CMOS logic

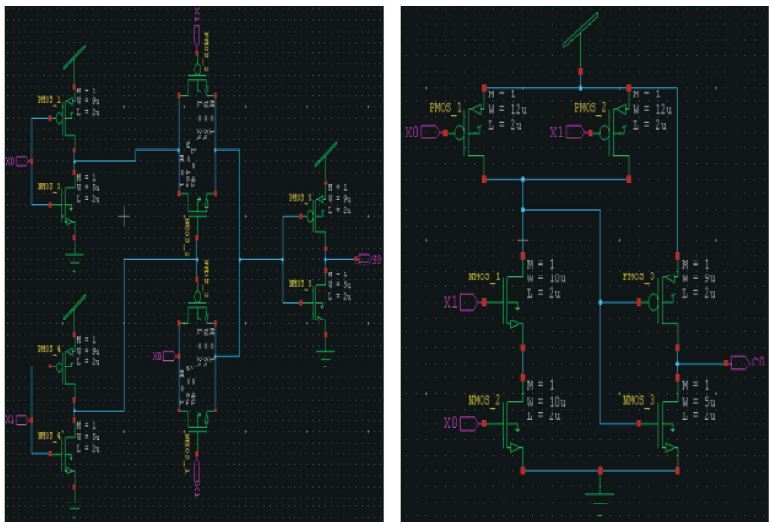

Fig. 5: Schematic diagram of existing half adder using Static CMOS technique

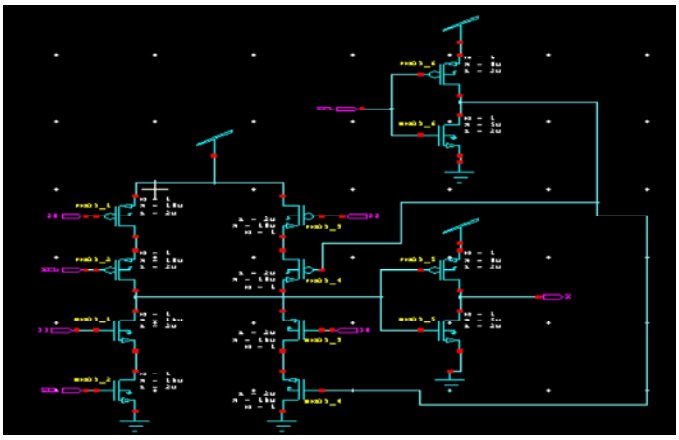

Fig. 6: Schematic diagram of existing MUX using Static CMOS technique

Compact Carry Save Adder: In the proposed compact carry save adder (CCSA) is designed by using GDI logic. Reduced AND, OR, XOR gates, half adder and full adder is designed by using GDI (gate diffusion input) logic to reduce the transistors when compared to the static CMOS and existing GDI logic. The proposed AND, OR and XOR gates is designed using 5 transistors for each gate instead of 6 transistors [12]. This reduced structure is applied in the Fig. 1 and the outcomes are examined.

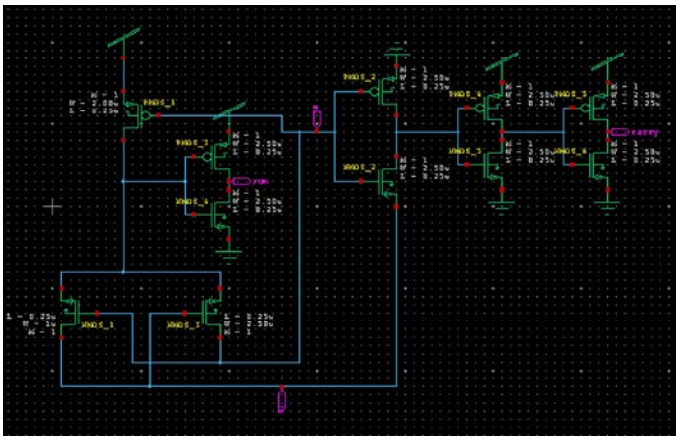

Fig. 7: Schematic of reduced half adder using GDI logic

Fig. 5 and Fig. 7 are compared. From the comparison proposed half adder need only 11 transistors instead of 16 transistors.

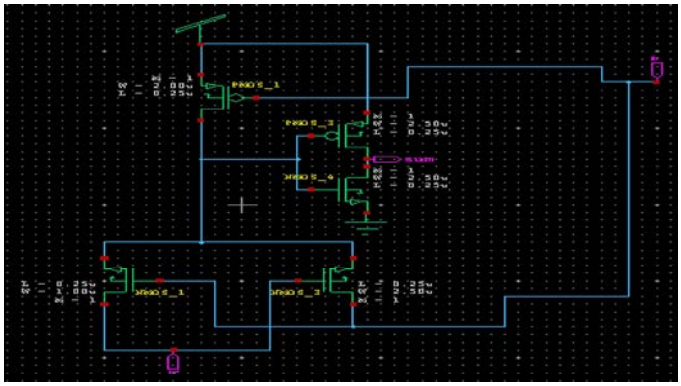

Fig. 8: Schematic of reduced XOR gate using GDI logic

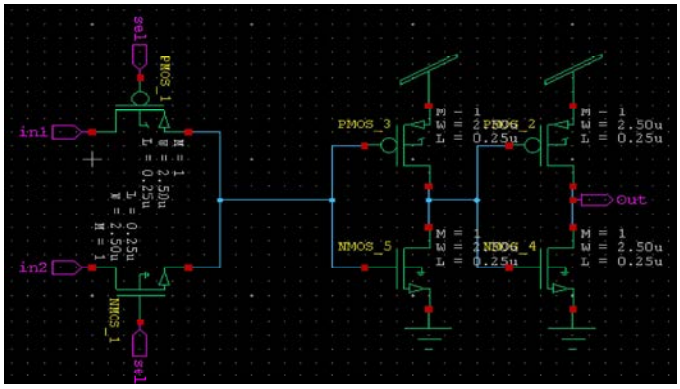

Fig. 9: Schematic of reduced MUX using GDI logic

The proposed Multiplexer as shown in Fig. 9 is compared with existing multiplexer as shown in Fig. 6. From the analysis, the proposed MUX need only 6 transistors instead of 12 transistors [13].

RESULTS AND DISCUSSION

In this paper, the design of compact carry save adder with optimized AND, OR, XOR gate, Multiplexer and half adder is presented for low area and low power applications. The compact carry save adder and conventional carry save adder are designed and implemented using Tanner14.11 to examine the power, area and this adder functionality. The Table.1 illustrates the Maximum Power of compact carry save adder over conventional carry save adder using different CMOS technology.

Table 1: Comparison of existing and compact carry save adder

	Existing CSA	Proposed CCSA
Nano technology	Max power	Max power
250nm	128 mw	82.4 mw
45nm	621 uw	371 uw

The proposed 16-bit CCSA provides 35.6% maximum power reduction when compared to the existing carry save adder. Similarly, the proposed CCSA offers 40.25 % power reduction than the existing CSA.

Table 2: Comparison between existing and proposed CSA for area utilization

	Existing CSA	Proposed CCSA
Adder Types	Number of transistors	Number of transistors
16-bit	1387	804
Half adder	16	11
Multiplexer	12	6
XOR	12	5
AND	6	5
OR	6	5

The table.2 describes the area utilization of different type of adder; the proposed compact carry save adder offers 42% area reduction for 16bit than the existing carry save adder. To reduce the number of transistor, GDI logic is used in the proposed CCSA in the transistor level. Also logic level simplification is achieved to reduce the number of gate.

CONCLUSION

In this paper, the design of reduced multiplexer, full adder and half adder is proposed using Gate diffusion Input (GDI) logic. The proposed half adder needs only 11 transistors instead of 16 transistors. multiplexer needs 6 transistors instead of 12 transistors. This gate, mux and half adder have been integrated in the proposed compact carry save adder CCSA(CCSA) with GDI logic with buffer in the end of the half adder. In the proposed CCSA, voltage drop is reduced in the modified GDI logic adder than the ordinary GDI logic. The simulation result shows that the proposed CCSA consumes low power and requires less number of transistors than the conventional CSA. In future, this CCSA structure has been used to design a parallel FIR filter.

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