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Performance Analysis of Square Cross Section Based Junctionless Silicon Nanotube FET

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Abstract: In this paper, Square cross section based n-type Junctionless silicon nanotube field effect transistor (SQ-JLSiNT) device's performance are studied using 3D TCAD simulations. The device is operated in three modes namely gate inside, gate outside and gate inside-outside. The parameters, OFF current (I_{OFF}), ON current (I_{ON}), transconductance (g_m), subthreshold swing (SS), output resistance (R_{OUT}), gate capacitance (c_{gg}), unity gain frequency (f_T), input impedance (Z_{in}) and noise figure (NF) are extracted and compared for gate inside (GI), gate outside (GO), gate inside & outside (GIO) based SQ-JLSiNT devices.

Key words: Junctionless FET · GO · GIO

INTRODUCTION

To achieve a high drive current at low leakage, scaling of conventional planar transistors has been used by main stream semiconductor industry. 3D device structures such as Tri-Gate (TG), Double-Gate (DG) and Gate-All-Around (GAA) are appeared in the continuous desire for higher performance at lower leakages. GAA is considered to provide ultimate electrostatic controllability as the gate completely surrounds the channel [1-5]. However, the search for the better device structure has continued which has led to the invention of novel device, Silicon Nanotube-FET (SiNT). The SiNT has the two gates namely inner and outer gates which control the tubular channel for better control hence SiNT exhibits the best of TG, DG and GAA [6]. Nowadays junctionless transistors are popularly known for its lesser fabrication complexity and its good immunity to short channel effects (SCE) [7, 8]. Junctionless based gate inside or gate outside device with square cross section is already explored in reference [9, 10]. Junctionless based SiNT contains both inner and outer gates with circular cross section are also explored in [11]. Square cross section based Junctionless SiNT-FET with gate inside & outside is not yet explored.

In this paper, we present the device performance of square cross section based junctionless SiNT (SQ-JLSiNT) using TCAD 3D simulations with gate inside (GI), gate outside (GO), Gate inside-outside (GIO) structures. The rest of the paper is organized as follows: Device structure and the simulator models used for simulations have been discussed in Section 2. Electrical characteristics of GI, GO, GIO SQ-JLSiNT devices with comparisons are presented in Section 3. Finally, conclusions are given in Section 4.

Device Structure and Simulation Methodology: Unlike in conventional MOSFETs, SQ-JLSiNT is comprised of the components source, drain, channel of same doping profile of $1.5xe^{19}$ atoms/cm^3 and gate, gate oxide thickness of various dimensions depends on inner and outer gate. The device details of GI, GO, GIO JLSiNT devices are given in Table 1. Sentaurus TCAD simulator from Synopsys is used for this study. The simulator has many facilities and the following modules are used in this study.

- Sentaurus Structure Editor (SDE): To create the device structure, to define doping, to define contacts and to generate mesh for device simulation.
- Sentaurus Device Simulator (SDEVICE): To perform all DC, AC and noise simulations.
- SVisual and Inspect: To view the results.

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Table 1: Device details of GI, GO, GIO mode SQ-JLSiNT

Parameters	GI SQ-JLSiNT	GO SQ-JLSiNT	GIO SQ-JLSiNT
Gate Length	18 nm	18 nm	18nm
Oxide thickness	1 nm	1 nm	1 nm
Tube thickness	2 nm	2 nm	2 nm
Gate thickness	7 nm	2 nm	7 nm (GI)
2 nm (GO)			
N_S,N_D,N_{CH} (atoms/cm^3)	1.5 e^{19}	1.5 e^{19}	1.5 e^{19}
$N_{polygate}$ (atoms/cm^3)	1.44 e^{13}	1.44 e^{13}	1.44 e^{13}

The physics section of SDEVICE includes the appropriate models for band to band tunneling, quantization of inversion layer charge, doping dependency of mobility, effect of high and normal electric fields on mobility and velocity saturation. Transport properties are modeled using Drift-Diffusion, Density-Gradient, Philips Unified Mobility, Lombardi Mobility Degradation [12].

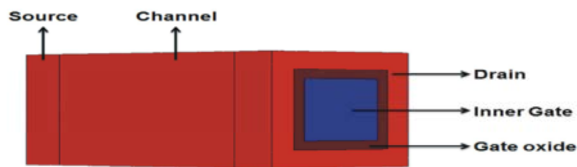

Fig. 1: Device structure of GI mode SQ-JLSiNT

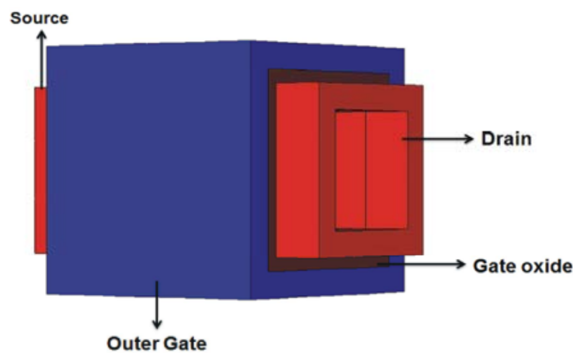

Fig. 2: Device structure of GO mode SQ-JLSiNT

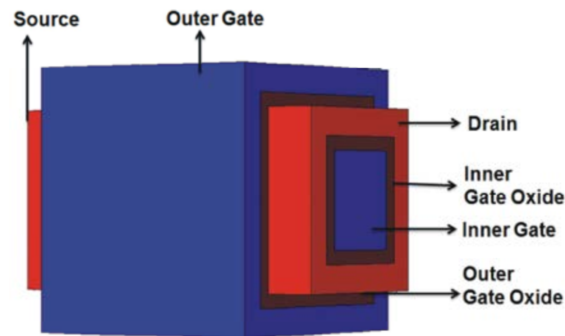

Fig. 3: Device structure of GIO mode SQ-JLSiNT

Figure 1 shows 3D device structure of GI SQ-JLSiNT device generated from Synopsys TCAD, corresponding to a gate thickness of 7 nm. Fig.2 shows 3D device structure of GO SQ-JLSiNT structure corresponding to a gate thickness of 2 nm. Fig.3 show 3D view device structure of GIO SQ-JLSiNT device corresponding to an outer gate thickness of 7nm and inner gate thickness of 2 nm.

RESULTS AND DISCUSSION

The simulator is calibrated against the published results on n-type gate inside Junctionless transistors I_D–V_{GS} data from Ref [9]. The calibrated I_D-V_G characteristics are shown in Fig.4.

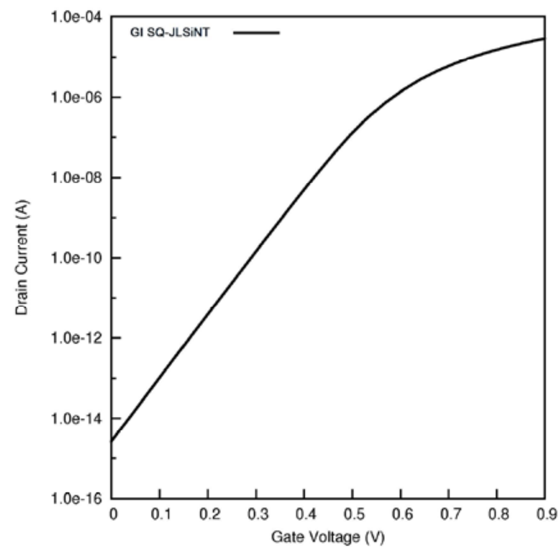

Fig. 4: I_D–V_G characteristics of GI mode SQ-JLSiNT

Using the calibrated models we have studied electrical performance of GI, GO, GIO mode SQ-JLSiNT devices. The supply voltage (V_{DD}) used in this study is 0.9 V. Figures 5 and 6 show the simulated I_D–V_G and I_D–V_D characteristics of GI, GO, GIO mode devices respectively. The device parameters, OFF current (I_{OFF}), ON current (I_{ON}), threshold voltage (V_{TH}), transconductance (g_m), are extracted from the saturated I_D–V_G characteristics from Fig.5 and are shown in Table 2.

It is observed from Fig.5 that GI SQ-JLSiNT device shows the OFF current (I_{OFF}) of 0.12 pA/µm and ON current (I_{ON}) of 1.31 mA/µm and for GO SQ-JLSiNT shows I_{OFF} of 1.22 pA/µm and I_{ON} of 1.08 mA/µm, GIO-SQJLSiNT device shows I_{OFF} of 0.2 aA/µm and I_{ON} of 0.36 µA/µm.

Table 2: Parameter values of GI, GO, GIO SQ-JLSiNT

Parameters	GI SQ-JLSiNT	GO SQ-JLSiNT	GIO SQ-JLSiNT
I_{ON} (A/µm)	1.318 e^{-3}	1.080 e^{-3}	3.682 e^{-5}
I_{OFF} (A/µm)	1.209 e^{-13}	1.220 e^{-12}	2.0486 e^{-17}
g_m (µ Siemens)	157.8	83.4	247.7
R_{OUT} _V_{GS}=0.5 v	484 K?	1041 K?	387.53 K?
A_V	76.37	86.81	95.99
SS (mV/decade)	63.03	66.92	60.89
f_T (GHz)	634	854	607
NF (dB)	67.09	60.79	82.80
Z_{in} _10GHz	156-j68	60-j112	1027-j186
C_{gg} (F/µm)	3.12e^{-17}	8.08e^{-18}	4.9e^{-17}

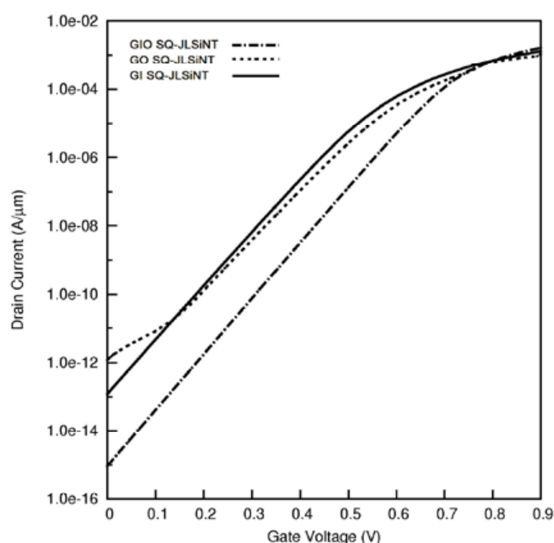

Fig. 5: I_D–V_G characteristics of GI, GO, GIO mode SQ-JLSiNT

Input impedance (at 10GHz) and Noise figure (NF) and gate capacitance are calculated for all three structures and given in Table 2. It is observed from the Table2 that c_{gg} is higher in GIO hence Z_{in} is higher in GIO device comparatively. Noise Factor = 1+ (T_e/T_o), where T_e is the noise equivalent temperature contributed by the sources. T_o is standard temperature (290K). Noise Figure shows the Noise Factor value in dB. Since the GIO is controlled by two simultaneously driven supply sources, the T_e is high comparatively and shows the higher NF. GO shows the better NF and is shown in Table 2.

For RF applications unity gain cut-off frequency (f_T) is one of the important metric and in terms of device parameters, f_T is given by,

$$f_T = \frac{gm}{2\pi Cgg}$$

where, g_m is the trans-conductance, C_{gg} is the combination of gate-source capacitance (C_{gs}), gate-drain capacitance (C_{gd}) and overlap capacitance (C_{ov}). From the standard AC simulations, transit frequency (f_T) is extracted when Y_{21}/Y_{11} equals one. Since the c_{gg} is higher in GIO device, it expected that f_T will be lower for GIO device comparatively and the result shown in Table 2 confirms the same.

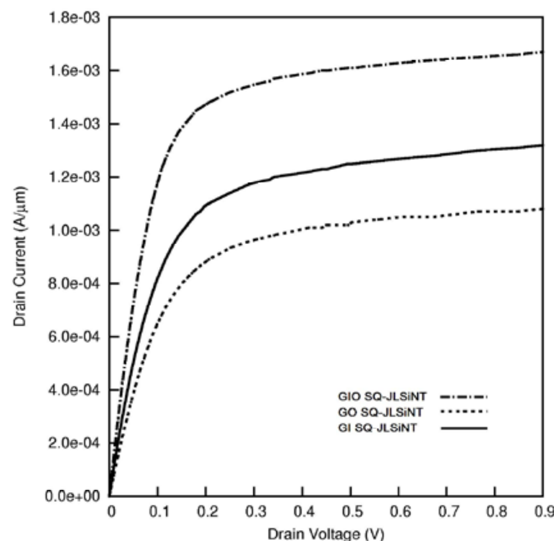

Fig. 6: I_D–V_D characteristics of GI, GO, GIO mode SQ-JLSiNT

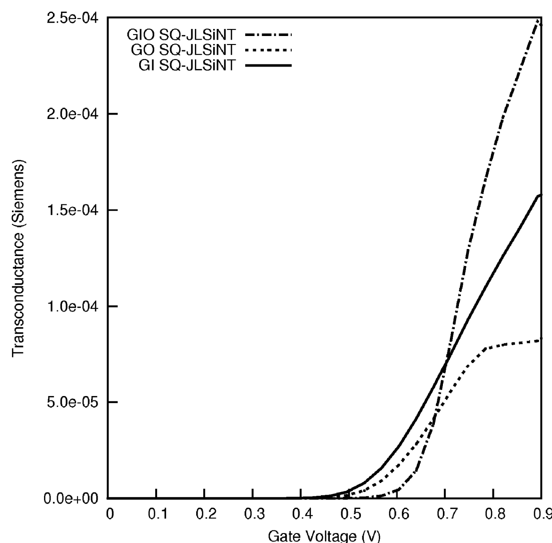

Fig. 7: g_m versus Gate voltage of GI, GO, GIO mode SQ-JLSiNT

R_{OUT} is extracted at saturated region from Fig.6 with the V_{GS} just above the threshold voltage to obtain maximum AC swing. Figure 7 shows the transconductance

versus gate voltage for all three devices. It is observed that peak transconductance is occurred for GIO and GI mode SQ-JLSiNT at 0.9V whereas for GO mode SQ-JLSiNT at 0.8V.

CONCLUSION

We investigated the Square cross section based n-type Junctionless silicon nanotube field effect transistor in GI, GO and GIO mode with basic DC and AC simulations using TCAD simulations. We extracted the parameters, OFF current (I_{OFF}), ON current (I_{ON}), transconductance (g_m), subthreshold swing (SS), output resistance (R_{OUT}), gate capacitance (c_{gg}), unity gain frequency (f_T), input impedance (Z_{in}) and noise figure (NF) for all three modes. The GIO device shows the better in DC, Z_{in} and lesser f_T since the c_{gg} is more due to larger gate area.

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