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Harmonic Reduction and Power Quality Enrichment in Three Phase Asymmetric Multilevel Inverter Fed Pmbldc Drive System

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Abstract: This paper presents the ternary voltage progression for asymmetric cascaded multilevel inverter (ACMLI) fed Permanent magnet brushless DC motor drive. Objective of this work is to propose an alternative topology that can reduce the number of power switches and complexity in design compared to the conventional multilevel inverter. With the presented topology, quality of the inverter output voltage is improved with lesser number of power switches. A structure of 27 level inverter is built and presented to investigate the performance of this topology. With the use of presented inverter, resolution is increased and the harmonic content is highly reduced. This system is an effective replacement for the conventional method. The complete model of the proposed drive system is developed and simulated using the MATLAB/Simulink. A prototype is developed, using ARM® Cortex™-M0 Core (NUC140XXCN) controller to verify the theoretical and simulation results. The number of utilized switches, installation area and cost are considerably reduced compared to conventional inverter.

Key words: Asymmetric cascaded multilevel inverter · Permanent magnet brushless DC motor (PMBLDC) · Total harmonic Distortion (THD) · ARM controller

INTRODUCTION

Recently, Multilevel inverter finds applications mainly in industries such as Brushless DC motor, AC power supplies, renewable energy sources, drive systems, etc. The multilevel inverter has introduced the solution to increase the converter output voltage above the voltage limits of classical semiconductors. A new hybrid asymmetric multilevel inverter is introduced with minimum number of switches. This achieves a better sinusoidal output. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [1, 2].

The recent proliferation of motor drives in the automobile industry has generated a serious demand for highly efficient PM motor drives and this is the beginning of the interest in BLDC motors. In the literature, there are several simulation models available for BLDC motor drives. Even though these models have made a great contribution to BLDC motor drives, there is no comprehensive model for the analysis of a motor using a multilevel inverter. In the BLDC motor, torque pulsations produce noise and vibrations in the system [3-5]. Therefore, the minimization or elimination of noise and vibration is a serious issue in BLDC drives. Because of their high reliability, efficiency, maintenance free nature and silent operation, permanent magnet (PM) motors have been widely used in a variety of applications like enclosures for computers, aerospace, medical equipment, household products and value addition in air conditioner applications. Novel optimal current excitation scheme to minimize ripple torque based on the d–q–0 reference frame are used [3]. A new torque control method to reduce the torque ripple of BLDC motors, with un-ideal back EMF waveforms [4]. A different control strategy for BLDC machines [5]. The conventional methods proposed in the above literature use a six step inverter as an electronic commutator. The Previous literature does not use multicarrier multilevel inverter as an electronic commutator for PMBLDC motor drive. To solve the aforementioned problem, this study emphasizes to improve the performance by using a multilevel inverter as an electronic commutator fed to a PMBLDC motor.

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This paper investigates a control technique applied to the ternary asymmetric cascaded multi-level inverter fed PMBLDC motor drive to ensure an efficient voltage utilization and better harmonic spectrum [6-9].

It provides a cost effective solution in low and medium voltage applications. By proper control, the number of output voltage increases that yields nearly sinusoidal waveform. The advantage enhances, as the level increases to maximum. Furthermore, asymmetric cascaded multilevel inverters use unequal DC sources [10-12], which increase the modularity of the circuit. The researchers have strived in to introduce a new topology for multilevel converters with a reduced number of components compared to conventional multilevel converters.

This topology consists of series connected sub multilevel converter blocks. The major disadvantage associated with reduced number of switches is their circuit complexity due to the bulky capacitor. Additional design complications might be imposed, especially regarding the design of device heat sinks. Unfortunately, modulation technique is not serving the purpose if more auxiliary bridges increased. Moreover, a large number of auxiliary bridges have to be employed and large capacitor banks need to be included. Compare to the conventional topology ternary progression [13] provides a higher number of output levels, lower number of components, high modularity and reduction of output harmonics due to sinusoidal output voltages. The vast majority of electric power transmissions were three-phase and multilevel inverter is the common topology widespread.

The significant problem of cascaded multilevel inverter design is overcome by using this proposed method. In addition, the power component is minimized with increased output levels. However, the proposed method uses only three bridges instead of five bridges compared to the conventional hybrid cascaded multilevel inverter. Complexity of the system and the harmonic contents at the output waveform are reduced.

Ternary Asymmetric Cascaded Multilevel Inverter: A cascaded multilevel inverter consists of a series of H bridges in each phase. For three level output, H-Bridge topology requires one DC source along with four MOSFET switches [14-17]. Output voltage can have three values V_{dc}, $-V_{dc}$ and zero depending on the trigger pulses given to the switches. To provide a large number of output levels without increasing the number of inverters, asymmetric multilevel inverters can be used. It is proposed to choose the DC-voltage sources according to a geometric progression with a factor of 2 or 3. Using the proposed technique ternary DC voltage progression on ACMLI is generated. Ternary progressions, also called order-3 have DC voltages V_{dc1} =1V then V_{dc2} =3V …. $V_{dc\ min}$= $V_{dc\ N}$ =3^N V and the ternary progression have amplitude of DC voltages in the ratio 1: 3: 9:27. . : 3^N. Advantage of this topology is that the control and protection requirements of each bridge are modular. Increasing the number of levels provides more steps; hence, the output voltage has enhanced resolution and the better sinusoidal output voltage can be achieved. For modeling the presented inverter topology each full bridge inverter, the output voltage is given by

$$V_{0i} = V_{dc} (S_{1i}-S_{3i}) \quad (1)$$

input DC current is

$$I_{dci} = I_a (S_{1i}-S_{3i}) \quad (2)$$

i =1, 2, 3… (Number of full bridge inverters employed). I_a is the output current of the new hybrid inverter. S_{1i} and S_{3i} is the upper switch of each full bridge inverter. Now the output voltage of each phase of the multilevel hybrid inverter is given by

$$V_{on} = \Sigma_{i=1}^{n} V_{oi} \quad (3)$$

The structure introduced in this work is an Asymmetric cascaded multilevel inverter that uses unequal DC Sources. The general function of this multilevel inverter is the same as that of the other two inverters. ACMLI provides a large number of output voltage levels without increasing the number of full bridge units. In the proposed model, ternary DC voltage progressions of unequal DC sources of ACMLI are used. This is the most popular unequal voltage progression with an amplitude of DC voltage having a ratio of 1:3:9:27;81....3^N and the maximum output voltage reaches ((3^N-1)/2) V_{dc}. The ACHB consists of 3-bridges, to generate 27 level output for the DC Sources of 9:3:1 ratio. The output waveform has 27 levels as $+13V_{dc}$ ……$+1V_{dc}$ and zero. By different combinations of the 12 switches, S1-S12, each inverter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero. Let the output of H bridge-1 be denoted as V_1 (t), that of the H bridge-2 as V_2 (t) and that of the H bridge-3 as V_3 (t).Hence the output voltage is given by

$$V(t) = V_1(t) + V_2(t) + V_3(t) \quad (4)$$

Table 1: Mode of operation of the three-phase temary multi level inverter during positive cycle

Angle of interval in degrees	Voltage level
0-6.9	V_{dc}
6.9-13.8	$2V_{dc}$
13.8-20.7	$3V_{dc}$
20.7-27.6	$4V_{dc}$
27.6-34.5	$5V_{dc}$
34.5-41.4	$6V_{dc}$
41.4-48.3	$7V_{dc}$
48.3-55.2	$8V_{dc}$
55.2-62.1	$9V_{dc}$
62.1-69	$10V_{dc}$
69-75.9	$11V_{dc}$
75.9-82.8	$12V_{dc}$
82.8-89.7	$13V_{dc}$

As per the patterns given in the switching Table 1, driving pulses for the H-bridges are developed. The generated gate pulses are given to each switch in accordance with the developed pattern for the positive half cycle. Similarly the negative half will be generated to obtain 27 level output voltage. For N such cascade inverters, one can achieve the following distinct voltage levels

$$n = 3^N, \text{ if } V_{dc,j} = 3^{j-1} V_{dc}, j = 1, 2, \ldots, N. \quad (5)$$

The maximum output voltage of these N cascaded multilevel inverter is

$$V_{o,MAX} = \Sigma_{j=1}^{N} V_{do,j} \quad (6)$$

$$V_{o,MAX} = \left(\frac{3^{N}-1}{2}\right) V_{do} \quad (7)$$

if $V_{dc}j = 3^{j-1} V_{dc}$, $_j = 1, 2, \ldots, N.$

Simulation diagram of three phase ternary voltage progression topology is shown in Fig. 1. The simulation results of three phase voltage,FFTvoltage spectrum, stator current and electromagnetic torque waveform is presented in Fig. 2(a), (b), (c) and (d) respectively. Comparison of conventional topology with premeditated Ternary topology are given in Table 2. From the table it clearly state that the presented topology has greater reduction when compared with the conventional topology. Due to the higher voltage capability provided by MLI; quality of the output voltage is enhanced, which provides sinusoidal current without undulation. It leads to the reduction in torque ripple.

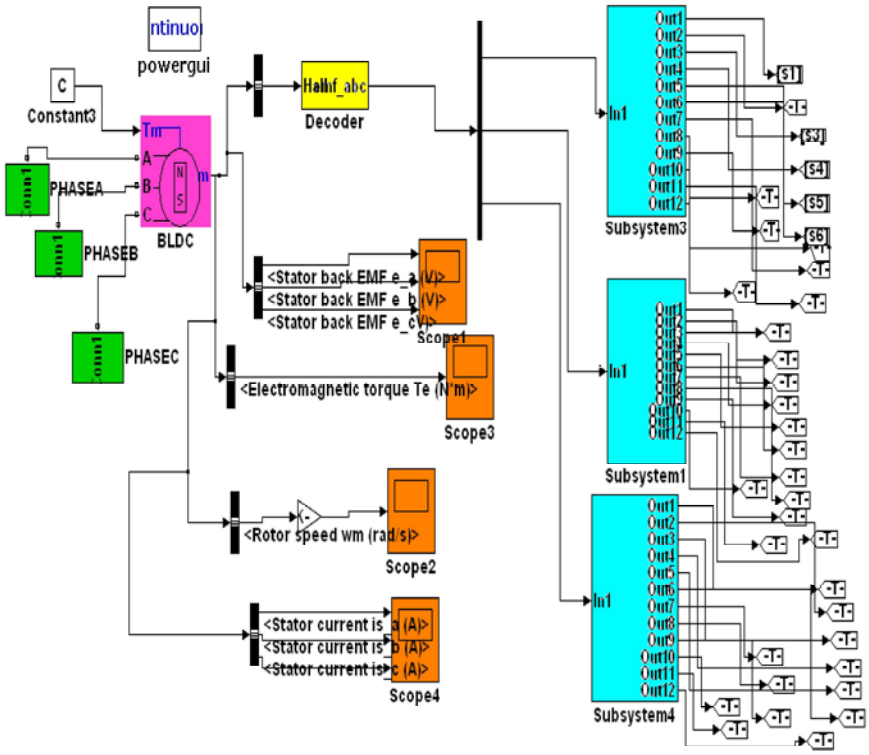

Fig 1: Simulation diagram of three phase ternary voltage progression topology

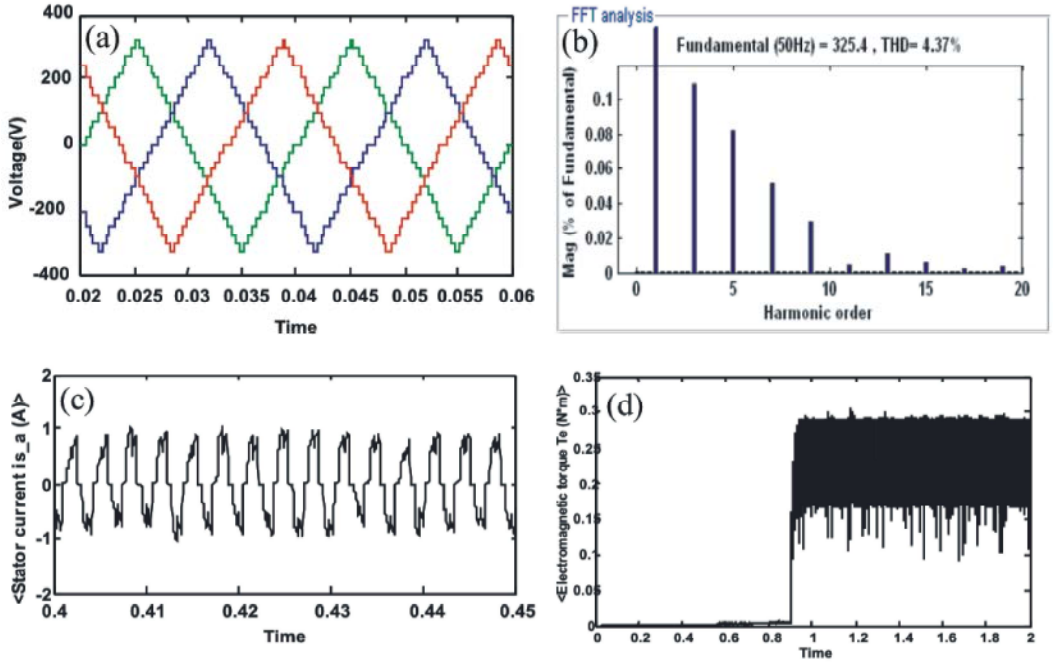

Fig. 2: (a) Three phase voltage waveform (b) FFT voltage spectrum (c) Stator current waveform (d) Electromagnetic torque

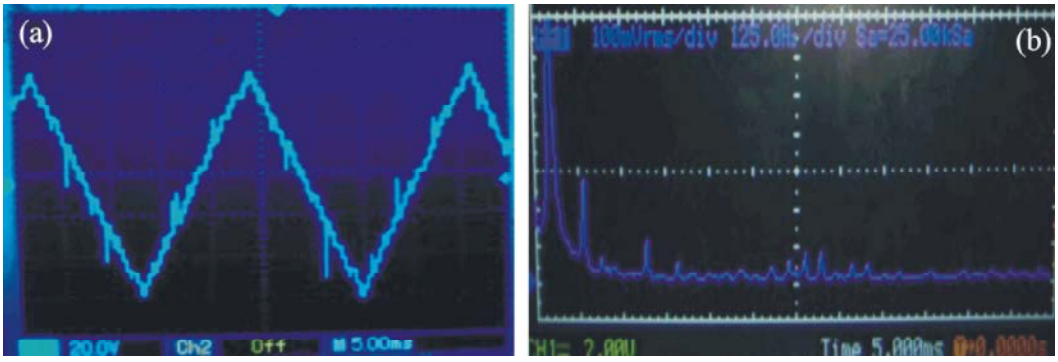

Fig. 3: (a) Output voltage waveform (X-axis 1CM=5mSec, Y-axis 1CM=20 Volts) (b) FFT Spectrum of output voltage.

Table 2: Comparison of conventional topology with premeditated Ternary topology

Parameter	Conventional	Proposed	% of Reduction
No.of Bridges	12	3	75%
No.of Switches	48	12	75%
TH.D%	13.66%	4.37%	9.29%

12 MOSFETs with 3 DC sources are required for the proposed topology. With lesser number of components, the proposed topology provides higher number of levels. Also, the voltage and current rating of the switches play an effective role in the cost of the system. Here the asymmetric topology employs unequal DC sources with Ternary progression. Proposed topology requires only 12 switches instead of 48 switches of the conventional topology. This attainment reduces installation cost and the area of the proposed topology compared to the conventional inverter. In addition to it, the complexity involved in the control circuit is also minimized.

RESULTS AND DISCUSSION

To validate the proposed concept, the inverter is implemented and its prototype has been manufactured. The NuMicro™ NUC100 Series is 32-bit microcontrollers with embedded ARM® Cortex™-M0 core, the cost is equivalent to traditional 8-bit microcontroller, Wide availability and reliable sources. The control circuit decides the sequence of pulses to be given to the switches in the power circuit. The driver circuit amplifies the pulses to the required level. The driver circuit is used

for an isolation of the negative current to the micro-controller, amplification of voltage and to create a constant voltage source. The square pulse should have a constant voltage of 5V. Isolation refers to the separation of the power circuit from the control circuit. A power circuit is fabricated using 12 MOSFETs (IRF540) and it requires three individual DC sources of an asymmetric ternary ratio. As per the switching sequence presented in Table 1, the pulse signals generated by taking competition and applied to the MOSFET switches, using the micro-controller. MOSFET with anti-parallel diodes are employed as switching devices. The opto coupler used for high side switch is 6N137and for low side switch MCT2E is used. During the hardware implementation, the inverter is tested for 52V. Each inverter leg takes different voltages**.** During the implementation, the inverter input sources are taken as V_{dc1} = 4 V, V_{dc2} = 12V and V_{dc3} = 36V with switching frequency f = 50 Hz. As illustrated, the experimental setup is built for the generation of desired output voltage waveform. The modulated output voltages with twenty seven-level waveform can be clearly appreciated; with low distortion. The hardware result obtained using arm processor is found to be in agreement with the simulation results.

CONCLUSION

Ternary voltage progression based Asymmetric cascaded Multilevel Inverter topology has been developed. To verify the performance, a three phase 27-level asymmetric cascaded multilevel inverter has been simulated, fabricated and tested experimentally by using ARM cortex controller. Experimental results are in line with the simulation results. With an asymmetric cascaded multilevel inverter fed PMBLDC drive, excellent voltage waveforms with reduced harmonic contents, improved fundamental component and efficiency has been obtained. In addition to this, THD content is also significantly reduced. Hence, the minimal current ripple leads to reduced torque ripple content of 0.12 Nm. These leads to reduced noise level and vibration to the system, which is the major requisite for PMBLDC drive applications. It is being realized in industries such as aerospace (fuel control), a robust Air conditioner and medical field (medical analyzer). Reduction in the components, size, complexity and cost makes it as an ideal solution for these industrial needs. Improving the harmonic profile, leads BLDC motor being maintenance free to certain extent to adhere the compact design without compromising robustness and reliability. The asymmetric multilevel inverter fed PMBLDC drive system can be used for industries where the faster, dynamics with minimal ripple content, enhanced speed and feedback control (speed) are required. Significant amount of energy can also be saved as the system has lesser harmonic losses.

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