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PI Control for Voltage Regulation in Positive Output Elementary Parallel Connected Boost Converter

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Abstract: The necessity of higher current and providing a back-up when one unit fail, demands the parallel operation of dc-dc converters. One of the problems of the parallel operating power converters is to regulate the output voltage and equalize the output currents of modules. This paper provides the design of PI Controller for parallel operated DC-DC boost converter. The output voltage regulation and load sharing behaviors are studied for the designed PI controller for disturbances viz. line voltage variations of converters, load variation and other circuit components changes. The performance evaluation is done in MATLAB-Simulink tool.

Key words: Parallel Connected Boost Converter · PI Controller · Voltage Regulation

INTRODUCTION

DC-DC step-up converters are widely used in computer hardware and industrial applications, such as computer peripheral power supplies, car auxiliary power supplies, servo-motors drives and medical equipment by Wood Peter [1] and Wang Kunrong *et al.* [2]. In recent years, the DC-DC conversion technique has been greatly developed. The main objective is to reach a high efficiency, high power density and cheap topology in a simple structure. Generally in power supply applications DC-DC converter modules are operated in parallel due to the reasons like higher power demand, improving the power system reliability and the operational redundancy (N+1 redundancy - N is the number of units needed to power the load, plus 1 as the back-up) Rajagopalan *et al.* [3]. There is also a trend in manufacturing the standard power converter modules which can be connected in parallel to cover a wide power range. This significantly reduces the costs of development and existing systems can be extended easily. The parallel operation offers the advantages such as expandability of output power, reliability and ease of maintenance. The main challenges in the parallel operations are output voltage regulation and load current sharing at different disturbances.

The average generalized PI output feedback regulator as a steer for defining the switched implementation of the average sliding mode features through a sigma-delta modulation strategy has been addressed by Sira-Ramirez *et al.* [4]. The control loop of a parallel connection of two nonidentical paralleled positive output elementary super lift luo converters using the SMC theory for current distribution control in continuous conduction mode Kuppan Ramash Kumar and Seenithangam Jeevananthan [5]. A droop method has been proposed for the converter parallel operation, which adaptively controls the reference voltage of each module. The scheme improves the output voltage regulation and the current sharing of the conventional droop method Jung-Won Kim *et al.* [6]. A robust controller for parallel dc–dc buck converters has been coined by combining the concepts of integral-variable-structure and multiple-sliding-surface control Mazumder *et al.* [7]. Grid connected solar PV system with SEPIC converter compared with parallel boost converter based MPPT Bosco Raj *et al.* [8]. Nonlinear back-stepping adaptive controller has been proposed for the design of parallel DC-DC buck converters with uncertainties of load and power disturbance. The relationship between the control elements and circuit parameters has been determined by simulation analysis. The relationship between current sharing difference and circulating current for two parallel connected dc-dc converters has been investigated Augustine *et al.* [9]. Although there may exist a trade-off between current sharing difference and voltage regulation, the proposed droop index algorithm gives

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better performance and low voltage regulation. The detailed analysis and design procedure are explained for two dc-dc boost converters connected in parallel. The effectiveness of proposed method is verified using MATLAB simulation.

The uncertainties in the source, load and other circuit parameters make the parallel operation of DC-DC converters challenging. This paper provides the design of PI Controller for parallel operated DC-DC boost converter. The output voltage regulation and load sharing behaviours are studied for the designed PI Controller for disturbances viz. line voltage variations of converters, load variation and other circuit components' changes. The performance of the developed controller in parallel boost converter is validated at the different working conditions through the simulation in the comparison with PI controller.

Principle and Operation of PI Controller: Variable structure control (VSC) is one of the effective nonlinear robust control approaches since it provides system dynamics with an invariance property to uncertainties once the system dynamics are controlled in the sliding mode DeCarlo [10]. For the non-linear system like positive output elementary cascade boost converter, the sliding mode controller is a more suitable approach. Sliding mode control has been presented as a good alternative to the control of switching power converters Tan Siw-Chong *et al.* [11] and Yiwen He *et al.* [12]. The main advantage over the classical control schemes is its insusceptibility to plant parameter variations that leads to invariant dynamics and steady-state response in the ideal case. In this paper, a sliding mode controller for the positive output elementary cascade boost converter is proposed.

System Description: The Positive Output Elementary Parallel Connected Boost Converter (POEPCBC) is shown in Figure 1. It includes dc supply voltage V_{in}, capacitor C, input inductor L, power switch (n-channel) S, freewheeling diode D, load resistance R. The principle of the sliding mode controller is to make the capacitor voltage V_C follows as faithfully as possible a capacitor voltage reference.

In the description of the converter operation, it is assumed that all the components are ideal and that the proposed converter operates in a continuous conduction mode. Figure 2 shows equivalent circuit while Figure 3 and Figure 4 represent two topological modes for a one cycle period of operation. When the switch S is closed in Figure 3, inductor current i_L rises quite linearly, diode current D is reverse polarized and capacitor C supplies the energy to output stage. Once the switch S is open in Figure 4, inductor current i_L is forced to flow through the diode D, capacitor C and load. The current i_L decrease while capacitor is recharged.

The ripple inductor current is;

$$\Delta i_L = \frac{V_{in}}{L} dT = \frac{V_o - V_{in}}{L}(1-d)T \tag{1}$$

Voltage transfer gain,

$$G = \frac{V_o}{V_{in}} = \frac{1}{1-d} \tag{2}$$

$$G = \frac{V_c}{V_{in}} = \frac{1}{1-d}$$

Inductor average current

$$I_L = (1-d)\frac{V_o}{R} \tag{3}$$

The state-space modelling of the equivalent circuit with state variables i_L and V_C is given by;

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} -\frac{V_C}{L} \\ 0 \end{bmatrix} \gamma + \begin{bmatrix} \frac{V_{in}}{L} \\ 0 \end{bmatrix} \tag{4}$$

$$\dot{v} = Av + B\gamma + C$$

where γ is the status of the switches, v and $\dot{v}$ are the vectors of the state variables (i_L, V_C) and their derivatives, respectively,

$$v = \begin{cases} 1 \rightarrow S \rightarrow ON \\ 0 \rightarrow S \rightarrow OFF \end{cases} \tag{5}$$

Design of PI Controller: A PI controller is chosen for providing the better output voltage regulation in POEPCBCs. The DC output voltage is sensed and compared with reference output voltage and error signal is obtained. This error signal is processed by the PI controller to maintain the output voltage constant.

The PI parameters, Proportional gain (Kp) and Integral times (Ti) are obtained by using Zeigler-Nichols tuning method [11]. The transfer function (TF) model of equation is obtained from the state space average model of the following equation using Matlab. Then

$$TF = \frac{-7.958e^{-12}s^2 + 1.667e^{8}s + 1.389e^{12}}{s^3 + 666.7s^2 + 8.333e^{7}s}$$

For simplifying the design aspect, the term -7.958e-12s2 in the numerator of the TF model is very small and hence it can be neglected. Therefore, the new TF becomes.

$$\mathrm{TF} = \frac{1.667\mathrm{e}^{8}\mathrm{s} + 1.389\mathrm{e}^{12}}{\mathrm{s}^3 + 666.7\mathrm{s}^2 + 8.333\mathrm{e}^{7}\mathrm{s}}$$

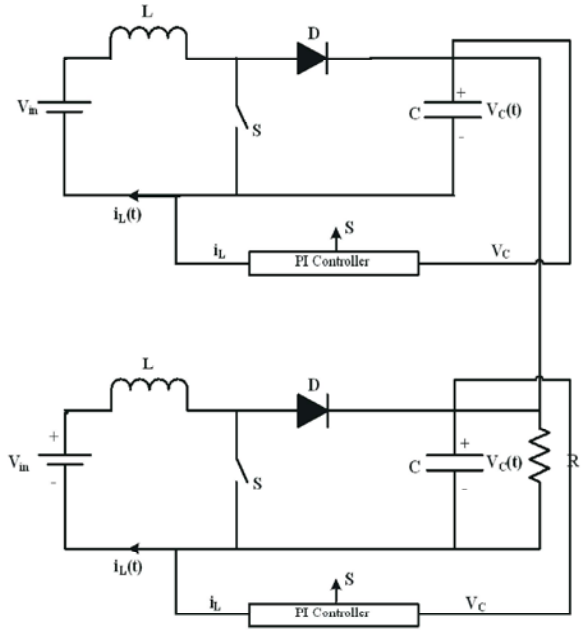

Fig. 1: The positive output elementary parallel connected boost converter controlled by PI

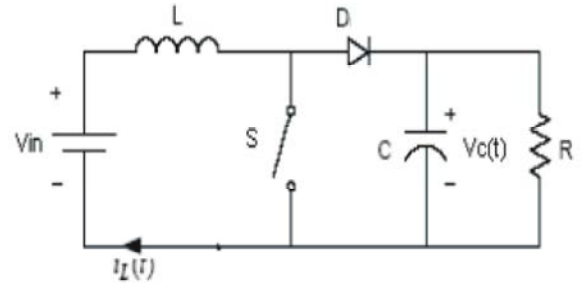

Fig. 2: Equivalent circuit for the positive output elementary cascade boost converter

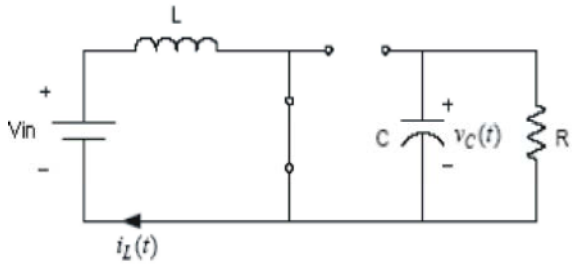

Fig. 3: Mode 1 operation

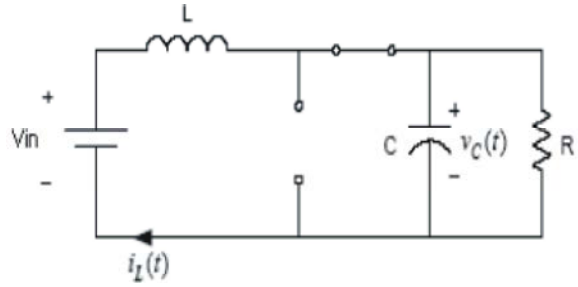

Fig. 4: Mode 2 operation

The characteristics equation with proportional control is expressed by;

$$s^3 + 666.7s^2 + s(8.333e^7 + K^* 1.667e^8) + K * 1.389e^{12} = 0$$

The routh array of above equation is;

s3:1 (8.8333e7+K*1.1667e8)
s2: 666.7 (K*1.389e12)
s1: (-8.333e7+2247116969*K)
s0: K*1.389e12

from this routh array, the range of K for stability (-8.333e7+2247116969*K) > 0, K>0.037, 0<K<0.037. So, the ultimate critical gain Kcr=0.037 and their corresponding wn=210447 rad/sec and Pcr=2*piwn=2.9856e-5. After the turning the controller using this method, the POEPBCs is providing a sustained oscillation with ultimate gain for stability can be found by Kcr=0.02 and their corresponding ultimate period Pcr=0.0012s. Using this method the value of Kp=Kcr/2=0.01205 and integral time Ti=Pcr/.2=0.0133s are determined.

RESULTS AND DISCUSSIONS

Here the PI controller is used for comparison with the designed controller. The validation of the system performance is done for different conditions viz. the start-up transient, line variation, steady state and

Table I: Parameters of Chosen POEPCBC

Parameters Name	Symbol	Value
Input Voltage	Vin	12V
Output Voltage	Vo =Vc	36V
Inductor	L	100 µH
Capacitor	C	30 µF
Nominal switching frequency	Fs	100 kHz
Load resistance	R	50
Output power	Po	25.92 W
Input power	Pin	38.952 W
Input current	Iin	3.246 A
Efficiency		88.277 %
Range of duty ratio	D	0.3 to 0.7

Table II: Performance of POEPCBC without controllers

Change inVin1 & Vin2 (V)	V01 (V)	V02 (V)	VO (V)	I1 (A)	I2 (A)	IO (A)
9 V -12 V	33.92	33.92	33.92	0.040	0.645	0.685
12 V-15 V	47.04	47.04	47.04	0.063	0.802	0.865
Resistance (Ω)	V01 (V)	V02 (V)	VO (V)	I1 (A)	I2 (A)	IO (A)
40 Ω	34.42	34.42	34.42	2.414	1.041	3.455
50 Ω	36.85	36.85	36.85	0.308	0.428	0.736
60 Ω	36.92	36.92	36.92	0.315	0.300	0.615

component variations. Simulations are performed on the POEPCBC circuits with the specifications are listed in Table 1.

Figure 6 and Figure 7 shows the average output currents and the gate pulse of paralleled modules without a controller for different input voltages (V_{in1}=12V and V_{in2}=15V). It can be seen that the current share of the modules are unequal. Table 2 lists the simulated results of the average output current/voltage for each of the modules and the POEPCBC without controllers for various input voltages and load resistances. From Table 2, it can be clearly seen that the output voltage regulation and the output current distributions of each of the modules and the POEPCBC are unequal.

Start-Up Transients: Figure 8 shows the dynamic behavior at start-up for the output voltage of paralleled modules for different input voltages viz. 9V, 12V and 15V. It can be seen that the output voltage of the paralleled modules has a little overshoot and a settling time of 0.008s for V_{in}=15V whereas for 12V and 9V there are negligible overshoots and a settling time of 0.01s and 0.012s for designed PI Controller, respectively. Figure 9 shows the dynamic behavior at start-up for the output voltage of paralleled module-1 for different input voltages viz. 9V, 12V and 15V. It can be seen that the output voltage of the paralleled modules has a little overshoot and a settling time of 0.022s for V_{in}=15V

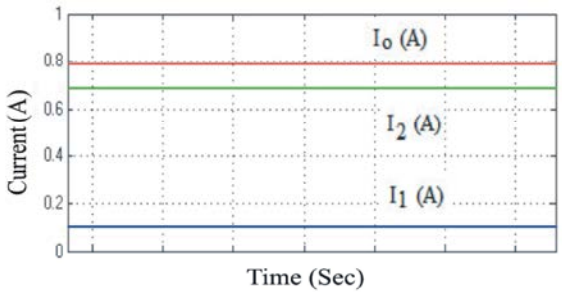

Fig. 6: Average output currents without a controller

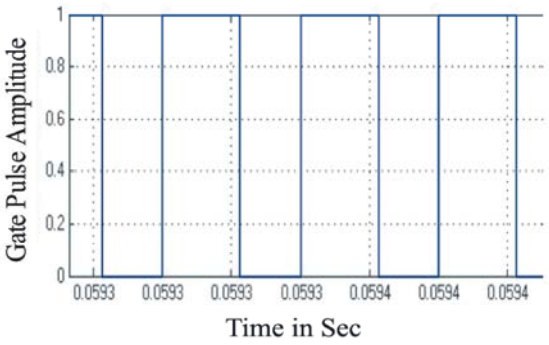

Fig. 7: Gate pulse of paralleled modules without a controller

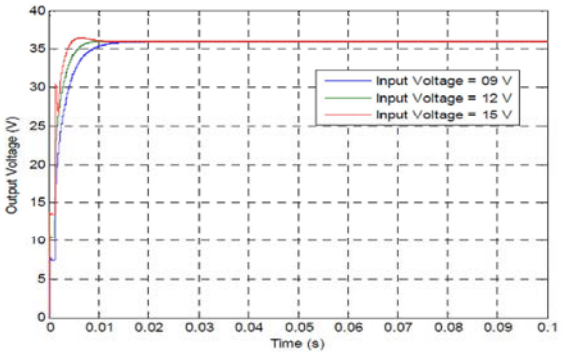

Fig. 8: Response at start-up for average output voltage of POEPCBC

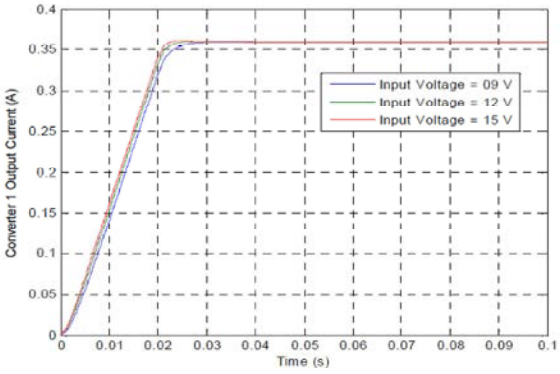

Fig. 9: Response at start-up for average output current of POEPCBC 1

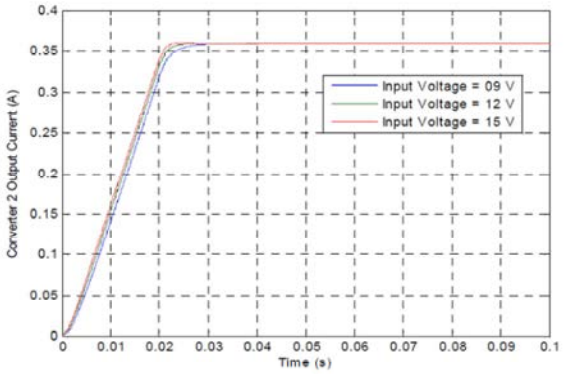

Fig. 10: Response at start-up for average output current of POEPCBC 2

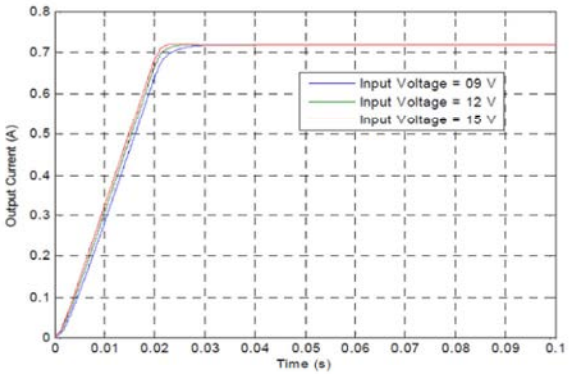

Fig. 11: Response at start-up for average output current of POEPCBC

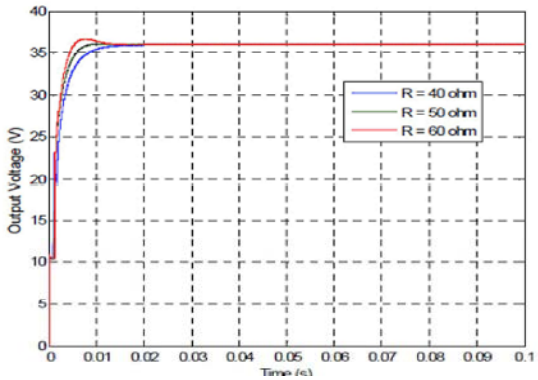

Fig. 12: Response at start-up for output voltage of paralleled modules

whereas for 12V and 9V there are negligible overshoots and a settling time of 0.025s and 0.028s respectively. Figure 10 shows the dynamic behavior at start-up for the output voltage of paralleled modules for different input voltages viz. 9V, 12V and 15V. It can be seen that the output voltage of the paralleled module-2 has a little overshoot and a settling time of 0.022s for V_{in}=15V

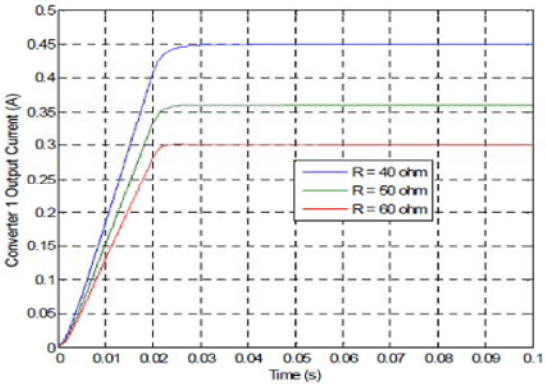

Fig. 13: Response at start-up for average output current of POEPCBC 1

whereas for 12V and 9V there are negligible overshoots and a settling time of 0.025s and 0.028s respectively. The overshoot behavior imitates the conclusions of the previous cases. Figure 11 shows the dynamic behavior at start-up for the average output current of paralleled modules.

Figure 12 shows the dynamic behavior at start-up for the output voltage of paralleled modules for different load resistances like 40Ω, 50Ω and 60Ω. It can be seen that the output voltage of the paralleled modules has a slight overshoot and settling time of 0.012s for R=60Ω, whereas the output voltage of the paralleled modules for R=50Ω and R=40Ω has a negligible overshoot and settling times of 0.013s and 0.014s with the designed PI Controller. Figure 13 shows the dynamic behavior at start-up for the average output current of paralleled module-1 for different load resistances like 40Ω, 50Ω and 60Ω. It can be seen that the output voltage of the paralleled module-1 for R=40Ω, R=50Ω and R=60Ω has a negligible overshoot and settling times of 0.03s, 0.025s and 0.021s with the designed controller.

Figure 14 shows the dynamic behavior at start-up for the average output current of paralleled module-2 for different load resistances like 40Ω, 50Ω and 60Ω. It can be seen that the output current of the module-2 for R=40Ω, R=50Ω and R=60Ω has a negligible overshoot and settling times of 0.03s, 0.025s and 0.021s with the designed PI Controller. Figure 15 shows the dynamic behavior at start-up for the average output current of paralleled module-2 for different load resistances like 40Ω, 50Ω and 60Ω. It can be seen that the output current of the modules for R=40Ω, R=50Ω and R=60Ω has a negligible overshoot and settling times of 0.03s, 0.025 and 0.021s with the designed PI Controller.

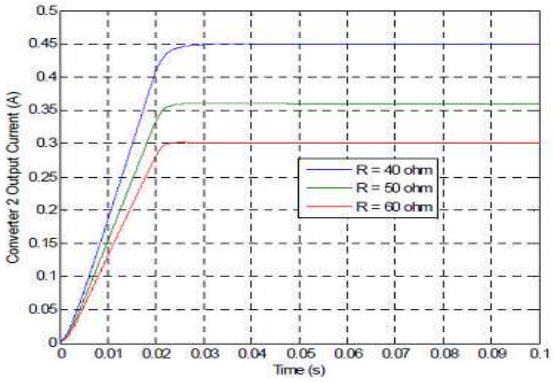

Fig. 14: Response at start-up for average output current of POEPCBC 2

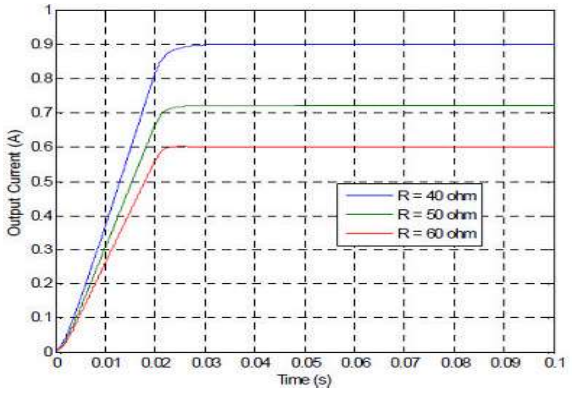

Fig. 15: Response at start up for average output current of POEPCBC

Table III: Voltage/Current profiles of POEPCBC for input voltages/load resistances with nominal input voltage/load in start-up region

	Voltage Profile		
	PI Controller		
Line Variation 9V - 15 V(Start-up region)	Vo1 (V)	Vo2 (V)	VO (V)
	36.05	36.05	36.05
	Current Profile		
	PI Controller		
Load Variation 40Ω - 60Ω (Start-up region)	I1 (A)	I2 (A)	IO (A)
40Ω	0.441	0.441	0.882
50 Ω	0.358	0.358	0.716
60Ω	0.291	0.291	0.582

Table 3 lists the simulated results of the average output current and voltage of each of the modules and the POEPCBC with controllers for various input voltage and load resistances in the start-up region. From Table 3, it can be seen that the voltage regulation and the current distributions of each of the modules and

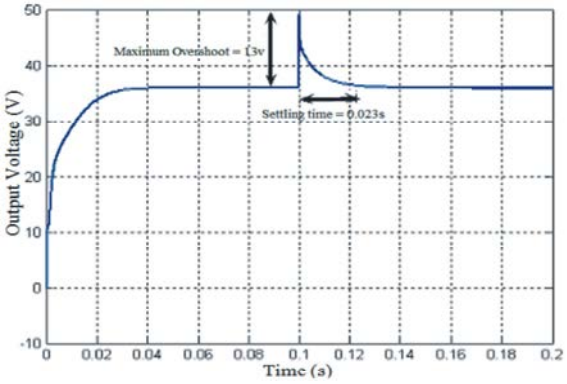

Fig. 16: Response of output voltage of paralleled modules (12V to 15V)

the POEPCBC using the designed PI Controller show excellent performance in comparison with a conventional PI controller.

Line Variations: In the Figure 16, the response of average output voltage of POEPCBC using PI controller for input voltage step change from 12V to 15V (+30% line variations) at time 0.05s. It is found that the output voltage of POEPCBC using PI controller exhibits the overshoot of 13V and has a long settling time of 0.023s, respectively. The simulated result of the designed controller gives better performance in comparison with the PI controller under the line variation.

Load Variations: Figure 12 Simulated response of output voltage of POEPCBC using PI controller for load change of 50Ω to 60Ω.

Figure 12 shows the response of the output voltage of paralleled modules using both a PI controller for load step change from 50Ω to 60Ω (+20% load variations) at time=0.1s. Here the output voltage of the paralleled modules using PI controller has a overshoot of 1.2V and a settling time of 0.018s respectively.

Steady State Regions: The Figure 13 gives the simulated instantaneous output voltage and the inductor current of POEPCBC in the steady state region using the PI controller. From the figure that the output voltage ripple is about 0.15 and peak to peak inductor ripple current is 0.51A for the average switching frequency of 100kHz closer to the theoretical designed. Figure 21 shows the instantaneous output voltage of paralleled modules in the steady state using PI controller. It is evident from the figure that the output voltage ripple is about 0.025V.

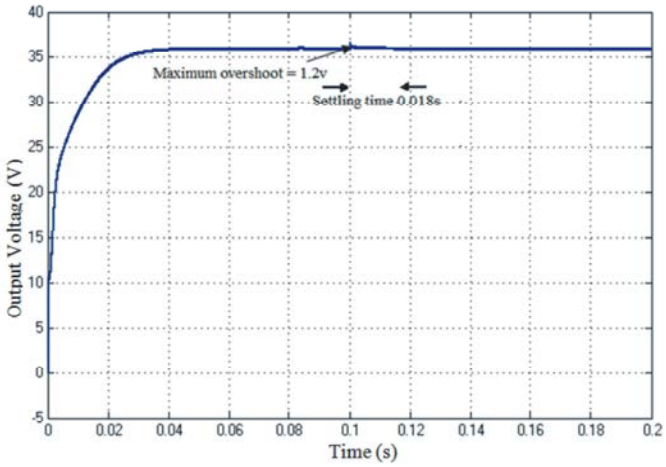

Fig. 17: Simulated response of output voltage of POEPCBC using PI controller for load change of 50Ω to 60Ω.

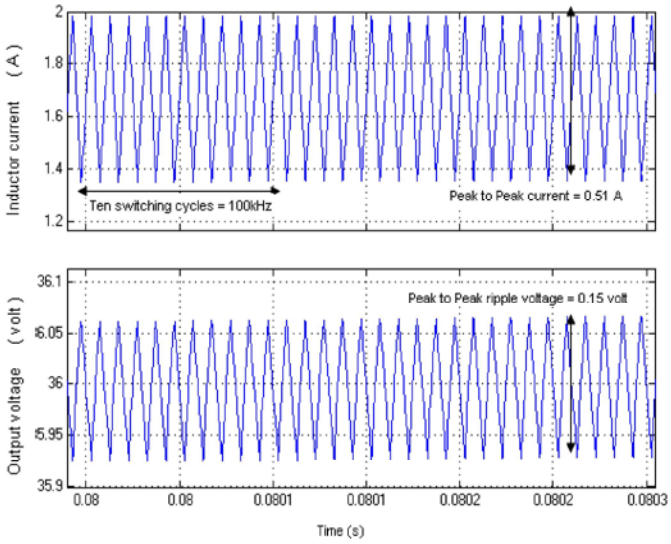

Fig. 18: Inductor current iL1 and output voltage in steady state region using PI Con-troller

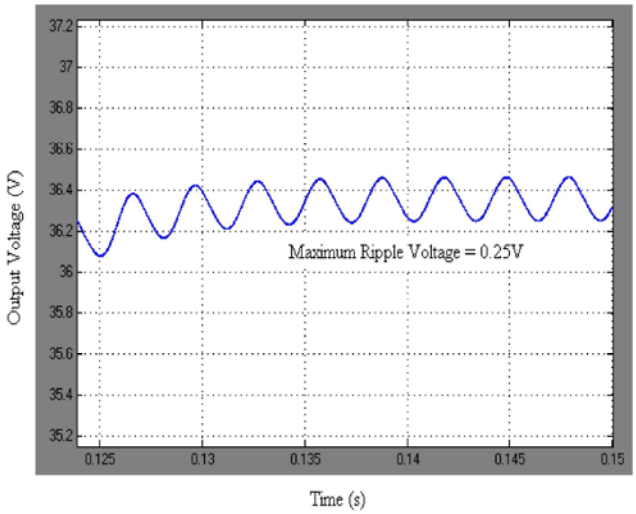

Fig. 19: Output voltage in steady state region using PI controller

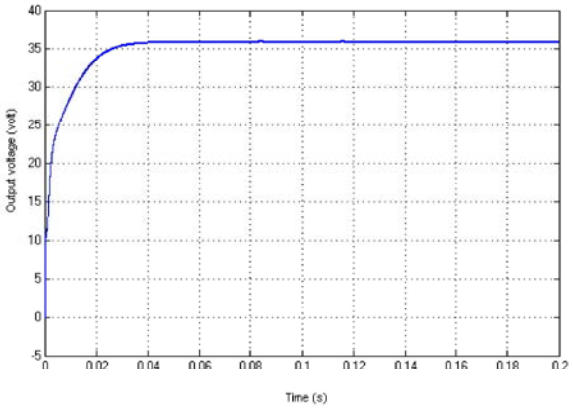

Fig. 20: Performance of POEPCBC output voltage (100µH to 500µH)

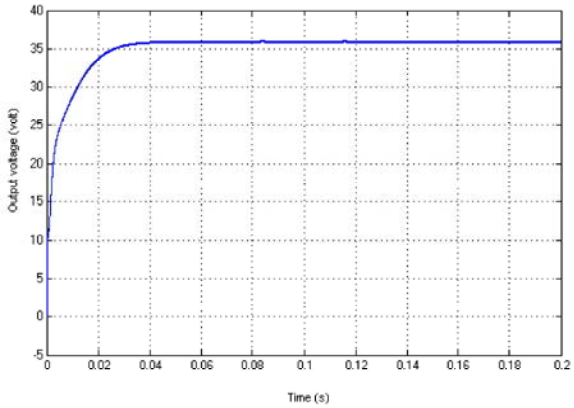

Fig. 21: Performance of POEPCBC output voltage (30µF to 100µF)

Circuit Components Variations: Figure 22 represents the response of the output voltage and current of paralleled modules using a PI controller for the variation of inductor L from 100µH to500µH. It can be seen that the change does not influence the paralleled converters behavior due to the proficient design of the designed controller in comparison with a conventional PI controller.

An interesting result is illustrated in above Figure 24. It shows the response of the output voltage and the current of the paralleled modules with both a PI controller and the proposed controller scheme for a variation in the capacitors values from 30µF to 100µF. It can be seen that the PI Controller is very successful in suppressing the effect of the capacitive variation except that a negligible output voltage ripple with a quick settling time and a proper current distribution in comparison with a conventional PI controller. In summary from Figure 24, it is obviously specified that the simulated graphs of developed PI has better performance of during circuit component variation.

CONCLUSION

This paper has successfully demonstrated the design and suitability of the sliding mode controlled based positive output elementary parallel connected boost converter. The simulation based performance analysis of a sliding mode controlled positive output elementary parallel connected boost converter circuit has been presented along with its state averaged model. The proposed control scheme has proved to be robust and its triumph has been validated with load and line regulations and also with circuit components variations. Therefore the system achieves a robust output voltage against load disturbances and input voltage variations to guarantee the output voltage to feed the load without instability. The approach thus has several advantages for it credits: stability even for large supply, load variations and circuit components variations, robustness, good dynamic behavior and simple implementation. The proposed configuration, thus claims its use in applications such as computer peripheral equipment and industrial applications, especially for high output voltage projects.

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