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Analysis of Reduced Switch Seven Level Inverter for Fuel Cell System

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Abstract: This paper presents a single-phase modified H-bridge seven-level multilevel VSI topology with reduced number of switching devices. The main objective of these kinds of topologies is that the number of gate driving circuits is reduced, which reduces the switching loss, size and power consumption making the inverter circuit less complex. Improved characteristics of robustness and efficiency can be achieved using multilevel inverter topologies with this reduced number of switch count. This Multilevel Inverter (MLI) type enhances the reduction of Total harmonic content of the output waveform and switching losses of the inverter. The seven-level output voltage levels are generated, namely +3Vdc, +2Vdc, +Vdc, 0, -Vdc, -2Vdc and –3Vdc.Six carrier triangular signals that are identical to each other with an offset that is equivalent to the amplitude of the single sine reference signal were used to generate the switching signals. PD, POD and APOD multi-carrier PWM techniques with low/high carrier frequency are implemented in this seven level MLI. Among which of PWM technique the least output-voltage Total Harmonic Distortion (THD) is checked. The single-phase seven-level MLI is simulated using MATLAB Simulink.

Key words: *Multi-carrier PWM* · Multilevel inverter · Reduced Switch Count · Switching losses · Total Harmonic Distortion

INTRODUCTION

Since the invention of the multilevel inverters they have been receiving more popularity and attention in the alternate energy resource sectors because of its attractive features. The multilevel inverters reduced the total harmonic content of the output waveforms and also proved easier way in design or implementation [1-4]. The conventional single phase multilevel inverter topologies used are diode-clamped, flying capacitor and cascaded H-bridge multilevel inverters [5, 6]. Lot of research works are carried out in the field of multilevel inverter topologies. Thereby to overcome the demerits of the conventional multilevel inverter topologies there aroused many different types of multilevel inverter topologies. Some topologies came up with reduced number of switching device [7-11]. MLI with reduced number of DC sources having symmetrical or asymmetrical arrangements and some incorporating both these factors into it. Now the study is based on further reducing the number of the switch count and maximizing the total number output levels of the multilevel inverter [12, 13].

The harmonic reduction is one of the key factors of the multilevel inverter features. As the number of levels in the output voltage waveform is replicates the shape of the sinusoidal waveform hence reducing the harmonics contents in the output. This is one way to reduce the harmonic content of the output waveform and the other way is by using PWM techniques for switching signal generation. The Multiple Carrier Sinusoidal Pulse Width Modulation (SPWM) is the common and an efficient PWM technique used [14].

This paper investigates on one such multilevel inverter topologies with reduced number of switches. The power switches of the MLI topology is triggered by

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implementing multi-carrier PWM technique. The operational principle and comparative analyses are illustrated in depth with appropriate simulation results and its validation.

Circuit Configuration: The seven-level inverter topology is shown in Figure 1. The inverter uses totally only five switching devices to give an output voltage with seven steps unlike 12 are required in the conventional MLI topologies. The total number of input DC sources is four and they all are symmetrically arranged. Each level is obtained by the additive and subtractive value of the DC sources.

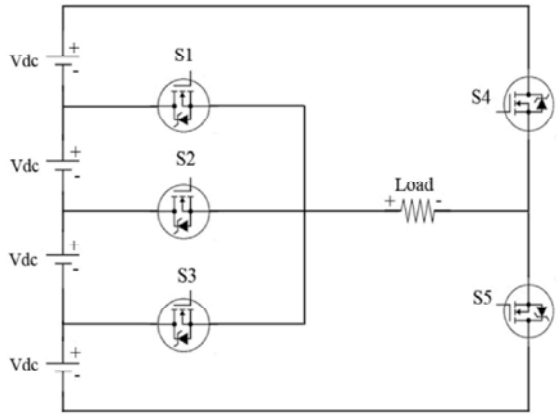

Fig. 1: Seven level inverter topology

For the ease of analysis purposes, the power electronic switches are considered to be ideal. The single-phase modified H-bridge seven-level MLI topology is significantly advantageous over other H-bridge topologies, i.e., less power switches and no power diodes or balancing capacitors required for inverters of the same levels.

Table 1: Comparative Table - 7 Level Inverter

Topology	Diode Clamped	Flying Capacitor	Cascaded H-bridge	Proposed System
Level	7	7	7	7
Switches	12	12	12	5
DC source	6	6	3	4
Clamping diodes	30	--	--	--
DC capacitors	--	15	--	--

Proper switching sequence for the multilevel inverter will produce seven output voltage levels, namely +3Vdc, +2Vdc, +Vdc, 0, -Vdc, -2Vdc and –3Vdcfrom the dc supply voltages. For every level only two switches are in the ON state and remaining three switches are in the OFF state. A resistive load is connected so as the output current is in phase with output voltage.

It is significant that every switch produces a relative loss during the ON and OFF operations so reduced switch count proves efficient. Besides that, this topology does not require any of the clamping diodes or clamping capacitors in the circuit.

Principle of Operation: Fig. 1 is the seven-level multilevel inverter topology with a resistive load connected to it. The multilevel inverter's operation can be divided into seven switching states: see figures 2(a-g) of which three are positive cycle states, three are negative cycle states and zero state.

The seven output voltage levels are generated as follows:

Table 2: Switching State Table - 7 Level Inverter

S.No	OutputLevels	S1	S2	S3	S4	S5
1	+3Vdc	1	0	0	0	1
2	+2Vdc	0	1	0	0	1
3	+Vdc	0	0	1	0	1
4	0	0	0	0	1	1
5	- Vdc	1	0	0	1	0
6	-2Vdc	0	1	0	1	0
7	-3Vdc	0	0	1	1	0

Mode 1 is Maximum positive output (+3Vdc) mode, in that mode of operation S1, S5 controlled switches are in ON state and the remaining switches will be in OFF condition. Figure 2(a) shows the conduction paths that are active in this state.

Mode 2 is Two-third positive output (+2Vdc) stage, in that state S2, S5 controlled switches are in ON state and the remaining is in OFF condition. Figure 2(b) shows the conduction paths that are active in this state.

Mode 3 is One-third positive output (+Vdc) state, in this stage S3, S5 controlled switches are in ON state and the remaining will be in OFF condition. Figure 2(c) shows the conduction paths that are active in this state.

Mode 4 is a Zero state output (0V), in this state S4 and S5 controlled switches are in ON state. The S4 connects the positive terminal to the positive of first dc voltage source and S5 connects the negative terminal of the fourth dc voltage source forming a loop. The loop current path disconnects the load from the voltage sources thus giving out 0V at to load terminal. Figure 2(d) shows the conduction paths that are active at this state.

Mode 5 is a One-third negative output (-Vdc) state, in this mode S1, S4 controlled switches are in ON state. Remaining all switches is in OFF state. Figure 2(e) shows the conduction paths that are active at this state.

Mode 6 is a Two-third negative output (-2Vdc) state, in this mode S2, S4 controlled switches are in ON state and the remaining switches is in OFF condition. Figure 2(f) shows the conduction paths that are active at this state.

Mode 7 is a Maximum negative output (-3Vdc) state, in this mode S3, S4 controlled switches are in ON state and the remaining will be in OFF condition. Figure 2(g)shows the conduction paths that are active at this state.

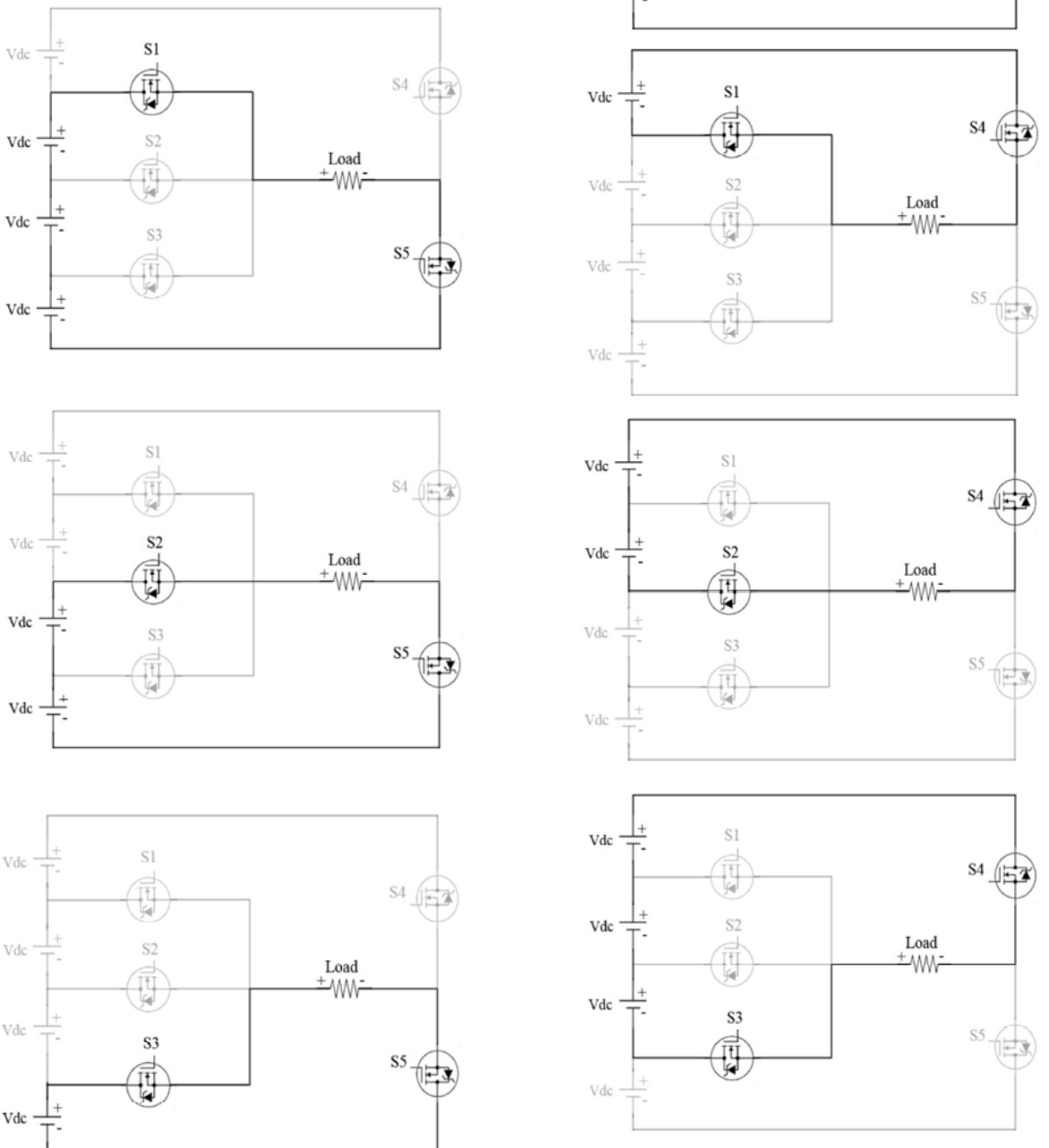

Fig. 2(a-g): Current paths that are active in mode 1-7

Multi-Carrier PWM: In the PWM methodologies the carrier wave frequency is set around 3 KHz to 11 KHz. The reason for moving onto high frequency switching is that the lower order harmonics are eradicated from the output waveform. Conventionally the PWM signals are generated using a single reference and single carrier waves. But when we require more number of PWM signals to be generated we move on to multi-carrier PWM technique.

But the usage of high switching frequency causes various undesired effects like heating effect in the MOSFETs furthermore enhancing the switching losses. Hence to overcome these ill-effects, Low Carrier Switching Frequency method is considered. The switching frequency selected is 100 Hz almost near to the fundamental frequency at which the reference wave frequency is set.

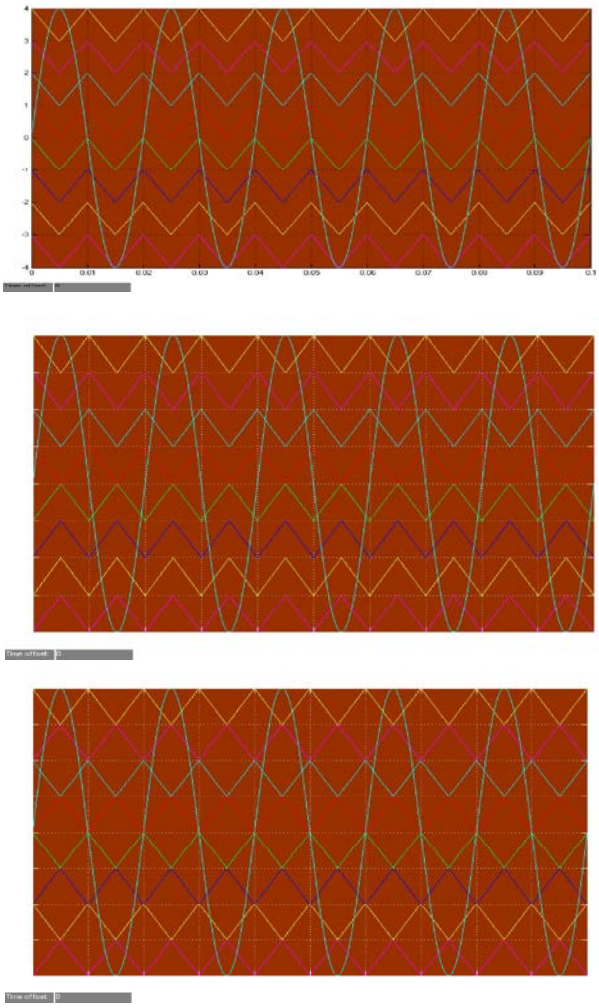

Fig. 3(a,b,c): Multi-carrier Switching Frequency PD, POD and APOD waveform

For this seven-level multilevel inverter topology, a single sine reference wave and six triangular carrier waves are compared. Six carrier triangular signals that are identical to each other with an offset that is equivalent to the amplitude of the single sine reference signal were used to generate the PWM signals.

The switching signals are generated using Multiple Carrier Sinusoidal Pulse Width Modulation (SPWM). The commonly used three multi-carrier PWM techniques are Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD). The multi-carrier switching PWM signal generation of PD, POD and APOD is shown in the figures 3(a, b, c).

Simulation Results: The simulation modeling is done for the single-phase modified H-bridge seven-level MLI topology with reduced number of switching devices in MATLAB Simulink. The PWM switching signals for the switching devices are generated by implementing appropriate multi-carrier PWM methodology.

The simulation model is experimented with Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD) multi-carrier PWM techniques. The carrier wave frequency is tested with low frequency value 100Hz and high frequency value 15KHz. The Total harmonic distortion of the output voltage is measured.

Table 3: THD Calculation for Low Carrier Frequency

Low Carrier Wave Frequency (100 Hz)			
Parameter	PDPWM	PODPWM	APODPWM
2nd Harmonics	8.15	0.15	0.15
3rd Harmonics	1.25	5.67	0.45
4th Harmonics	4.94	0.13	0.12
5th Harmonics	1.84	6.61	3.65
THD%	17.88	14.39	13.92

The carrier wave frequency is tested for low frequency at 100 Hz. The Total Harmonic Distortion of the multilevel VSI is tabulated for Phase disposition (PD PWM), Phase opposite disposition (POD PWM) and Alternate Phase opposite disposition (APOD PWM).

Table 4: THD Calculation for High Carrier Frequency

High Carrier Wave Frequency (15KHz)			
Parameter	PD PWM	POD PWM	APOD PWM
2nd Harmonics	0.54	0.41	0.28
3rd Harmonics	1.27	1.35	1.49
4th Harmonics	0.59	0.59	0.64
5th Harmonics	1.76	0.76	0.84
THD%	21.61	19.98	19.84

The carrier wave frequency is tested for low frequency at 15 Khz. The Total Harmonic Distortion of the multilevel VSI is tabulated for Phase disposition (PD PWM), Phase opposite disposition (POD PWM) and Alternate Phase opposite disposition (APOD PWM).

Among the THD results between low carrier wave frequency and high carrier wave frequency the THD value is less for the Lowcarrier wave frequency PWM technique. Thereby proving Lowcarrier wave frequency PWM technique reduces THD content and also enhances the switching loss reduction in the system.

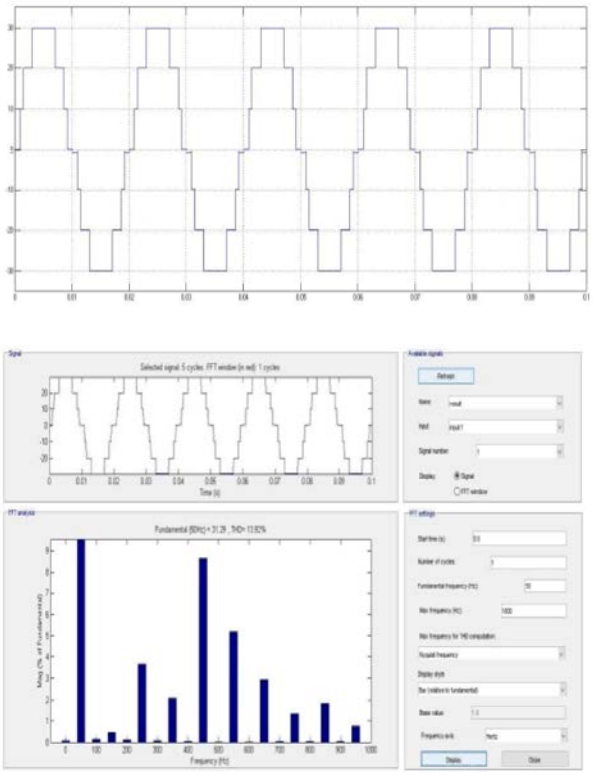

Fig. 4(a,b): Low carrier frequency APOD PWM based output voltage waveform and FFT window

The Alternative Phase Opposition Disposition (APOD) multi-carrier PWM technique show lower THD value while compared with the rest of the two methods.The output seven-level voltage waveform and the FFT window for THD calculation of Alternative Phase Opposition Disposition (APOD) multi-carrier PWM technique is shown in the figure 4(a,b) and 5(a,b)

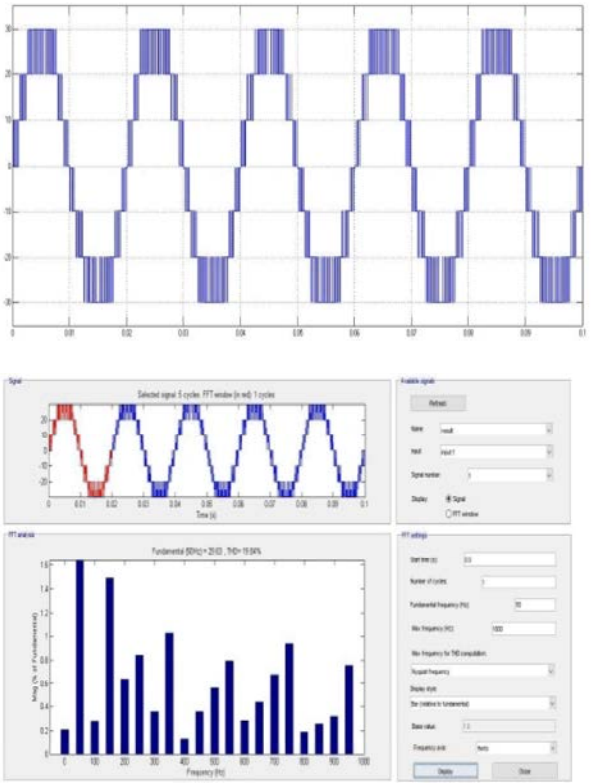

Fig. 5(a,b): High carrier frequency APOD PWM based output voltage waveform and FFT window

CONCLUSION

The simulation of the single-phase modified H-bridge seven-level MLI topology with reduced number of switching devices triggered with multicarrier PWM switching is simulated in MATLAB R2013a. The seven-level multilevel VSI with reduced number of switches, reduced number of DC sources and maximum number of output levels is modeled and simulated. The three types of multi carrier sinusoidal PWM techniques as PD, POD and APOD are implemented with low carrier wave frequency (100 Hz) and high carrier wave frequency (15 KHz).

From the results it is obvious that the Alternative Phase Opposition Disposition Multi-Carrier Sinusoidal Pulse Width Modulation (APOD SPWM) show relatively lesser THD content in the output voltage waveform. Hence it is recommended that for this seven-level multilevel inverter topology Low carrier wave frequency Alternative Phase Opposition Disposition Multi-Carrier Sinusoidal Pulse Width Modulation (APOD SPWM) is the best choice for implementation.

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