Middle-East Journal of Scientific Research 23 (Sensing, Signal Processing and Security): 319-328, 2015
ISSN 1990-9233

DOI: 10.5829/idosi.mejsr.2015.23.ssps.116

Multi-Level Grid-Connected Converter Topology for Transformer less PV Systems

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Abstract: This paper presents a single-phase transformerless grid-connected photovoltaic converter with a single cascaded full bridge with common source dc voltage. The converter can synthesize up to fifteen voltage levels with a single dc bus, since one of the full bridges is supplied by a flying capacitor. The multilevel output reduces harmonic distortion and electromagnetic interference. A suitable switching strategy is employed to regulate the flying-capacitor voltage, improve the efficiency (most devices switch at the grid frequency) and minimize the common-mode leakage current with the help of a novel dedicated circuit (transient circuit). Simulations and experiments confirm the feasibility and good performance of the proposed converter.

Key words: Component · Formatting · Style · Styling · Insert (key words)

INTRODUCTION

The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the Output waveform without increasing switching frequency or decreasing the inverter Power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multilevel starts from three levels. As the number of levels reach infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout and packaging constraints.

Multilevel Inverter

Transformerless Multilevele Inverter: Transformer less multilevel inverters is uniquely suited for this application because of the high volt-ampere ratings possible with these inverters. For EVs a cascaded H-bridges inverter can be used to drive the traction motor from a set of batteries or fuel cells. Where generated ac voltage is available such as from an alternator or generator aback-to-back diode clamped converter can convert this source to variable frequency ac voltage for the driven motor.

Multilevel inverters also solve problems with some present two level pulse width modulation (PWM) adjustable speed drives (ASD). ASDs usually employ affront end diode rectifier to convert utility ac voltage to dc voltage and an inverter with PWM controlled switching devices to convert the dc voltage to variable frequency and variable voltage of the motor speed control.

Motor damage and failure have been reported by industries as a result of some ASD inverters HIGH VOLTAGE CHANGE RATINGS (dv/dt), which produced a common mode voltage cross the motor windings. The main problems reported have been “motor bearing failure” and “motor winding insulation breakdown” because of circulating currents, dielectric stress, voltage surge and converter discharge.

Only recently have motor insulation failures becomes problem with some ASDs because the increased switching speed of contemporary power semiconductor Devices caused steep voltage waveforms to appear at the motor terminals. The voltage change rate (dv/dt) sometimes can be high enough to induce corona discharge between the winding layers. These high-speed semiconductor switches allow faster PWM carrier frequencies. Although the high frequency switching can increase the motor running efficiency and is well above the acoustic noise level, the dv/dt associated dielectric stresses between insulated winding turns also greatly

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Table 1: 5-level diode clamped inverter

V	S1	S2	S3	S4	S5	S6	S7	S8
0V	1	1	0	0	0	0	1	1
-Vdc/4	1	0	0	0	0	1	1	1
-Vdc/2	0	0	0	0	1	1	1	1
-Vdc/4	1	0	0	0	0	1	1	1
0V	1	1	0	0	0	0	1	1
0V	1	1	0	0	0	0	1	1
Vdc/4V	1	1	1	0	0	0	0	1
Vdc/2V	1	1	1	1	0	0	0	0
Vdc/4V	1	1	1	0	0	0	0	1
0V	1	1	0	0	0	0	1	1

increased. Multilevel inverters overcome these problems because the individual devices have a much lower dv/dt per switching and they operate at high efficiency because they can switch at a much lower frequency than PWM-controlled inverters

Fifteen Level Converter Strategy:

- This paper gives the explanation about the transformer less multilevel converters.
- The main objective of this project is it will give the harmonic less stepped waveform to the input of the motor.
- A multilevel converter gives multilevel outputs.
- Here AC is converted into AC because the first AC is direct voltage it consists of more harmonics and fluctuations.
- The AC is converted into DC by using rectifier and then converted into AC by using multilevel converters.
- The main advantage of this project is filter less constant output voltage.
- Initially it has higher torque.
- The controller program is implemented using micro controller.
- Using diode clamped converter to get the correct stepped waveform, suppose we are using capacitor clamped we are getting pulsated stepped waveform.

Diode Clamped Inverters: To produce a staircase-output voltage, let us consider only one leg of the five level inverter as shown. A single-phase bridge with two legs is shown. The dc rail 0 is the reference point of the output phase voltage. The steps to synthesize the five level voltages are as follows,

- For an output voltage level Vao=Vdc turn on upper half switches Sa1 through Sa4.
- For an output voltage level Vao=3Vdc/4, turn on three upper switches Sa2 throughSa4 and one lower switch Sa1'.
- For an output voltage level Vao=Vdc/2, turn on two upper switches Sa3 through Sa4 and two lower switches Sa1'and Sa2'.
- For an output voltage level Vao=Vdc/4 turn on one upper switch Sa4 and three lower switches Sa1' through Sa3'.
- For an output level Vao=0,turn on all lower half switches Sa1' through Sa4'.

Table shows the voltage levels and their corresponding switch states. State condition 1 means the switch is on and state 0 means the switches off. It should be noticed that each switch is turned on only once per cycle and there are four complementary switch pair in each phase. These pairs for one leg of the inverter are (Sa1, Sa1'), (Sa2, Sa2'), (Sa3, Sa3') and (Sa4, Sa4'). Thus if one of the complementary switch pairs is turned on, the other of the same pair must pairs is turned on, the other of the same pair must be off. Four switches are always turned on at the same time.

Flying-Capacitor Multilevel Inverteter: It shows a single phase, full bridge five level converter based on a flying capacitors multilevel inverter. The numbering order of the switches is Sa1, Sa2, Sa3, Sa4, Sa1', Sa2', Sa3', Sa4', note that the order is numbered differently from that of the diode-clamped inverter. The numbering is immaterial as long as the switches are turned on and off in the right sequence to produce the desired output waveform. Each phase leg has an identical structure. Assuming that each capacitor has the same voltage rating, the series connection of the capacitors indicates the voltage level between the clamping points. Three inner loop-balancing capacitors for phase leg- a are independent from those for phase leg b. All phase legs share the same dc-link capacitors, c1 through c4.

The voltage level for the flying capacitors converter is similar to that of the diode-clamped type of converter. That is the phase voltage Vao of an m-level converter has m-levels and if the line voltage Vab has (2m-1) levels.

Table 2: Level capacitor clamped inverter

Vao	Sa1	Sa2	Sa3	Sa4	Sa1'	Sa2'	Sa3'	Sa4'
V5=Vdc	1	1	1	1	0	0	0	0
V4=3Vdc/4	1	1	1	0	1	0	0	0
V3=Vdc/2	1	1	0	0	1	1	0	0
V2=Vdc/4	1	0	0	0	1	1	1	0
V1=0	0	0	0	0	1	1	1	1

Assuming that each capacitor has the same voltage rating as the switching device, the dc bus needs (m-1) capacitors for an m-level converter. The number of capacitors required for each phase is m,

$$Nc=\Sigma j=1\ (m-j),\ \text{Thus for } m=5,\ Nc=10.$$

Principle Of Operation: To produce a staircase output voltage, let us consider the one leg of the five level inverter shown. The dc rail '0' is the reference point of the output phase voltage. The steps to synthesize the five level voltages are as follows:

- For an output voltage level Vao=Vdc, turn on all upper half switches Sa1 through Sa4.
- For an output voltage level Vao=3Vdc/4, there are four combinations:

- Vao=Vdc-Vdc/4 by turning on devices Sa1, Sa2, Sa3, Sa4'
- Vao=3Vdc/4 by turning on devices Sa2, Sa3, Sa4, Sa1'.
- Vao=vdc-3Vdc/4+Vdc/2 by turning on devices Sa1, Sa3, Sa4, Sa2'.
- Vao=Vdc-Vdc/2+Vdc/4 by turning on devices Sa1, Sa2, Sa4, Sa3'.

- For an output voltage level Vao=Vdc/2 there are six combinations:

- Vao=Vdc-Vdc/2 by turning on devices Sa1, Sa2, Sa3', Sa4'
- Vao=Vdc/2 by turning on devices Sa3, Sa4, Sa1', Sa2'.
- Vao=Vdc-3Vdc/4+vdc/2-Vdc/4 by turning on devices Sa1, Sa3, Sa2', Sa4'.
- Vao=Vdc-3Vdc/4+vdc/4 by turning on devices
- Vao=3Vdc/4-vdc/2+vdc/4 by turning on devices
- Vao=3Vdc/4-Vdc2 by turning on devices Sa2, Sa3,

- For an output voltage level Vao=Vdc/4, there are four combinations
  - Vao=Vdc-3Vdc/4 by turning on devices Sa1, Sa2', Sa3', Sa4'.
  - Vao=Vdc/4 by turning on devices Sa4, Sa1', Sa2', Sa3'.
  - Vao=Vdc/2-Vdc/4 by turning on devices Sa3, Sa1', Sa2', Sa4'.
  - Vao=3Vdc/4-Vdc/2 by turning on devices Sa2, Sa1', Sa3', Sa4'.
  - For an output voltage level Vao=0, turn on all lower half switches Sa1' through Sa4'.

There are many possible switch combinations to generate the five –level output voltage. However lists a possible combination of the voltage levels and their corresponding switch states. Using such a switch combination requires each device to be switched only once per cycle. It can be noticed from table that the switching devices have unequal turn on time. Like the diode clamped inverter, the line voltage consists of the positive phase leg voltage of one terminal to the negative phase leg voltage of other terminal. The resulting line voltage is a nine-level staircase wave. This implies an m-level output phase leg voltage and a (2m-1) level output line voltage.

Proposed Fifteen-Level Inverter Topology: To prove the reduction in component numbers achieved by this simplified H-bridge multilevel inverter configuration, the number of component required to implement a 13 level inverter using simplified H- bridge multilevel inverter and three previously defined ones: the two that considered as the standard multi level stages, the diode clamped and the capacitor clamped configuration and a new and highly improved multi level stage with reduced switches

Main Power Switches: The new topology achieves a around 40% reduction in the number of main switches required, using only nine controlled power switches instead of twelve required in any of the other three configurations. The auxiliary switch voltage and current rating are lower than the once required by the main controlled switches.

Auxiliary Devices (Diodes and Capacitors): The new configuration reduces the number of diodes and capacitors, when compared with diode clamped

configuration. The new configuration reduces the number of capacitors, when compared with the capacitor clamped configuration. The new configuration uses no more diodes or capacitors.

Additionally, since three capacitors are connected in parallel with the main dc power supply, no significant capacitor voltage swing is produced during normal operation, avoiding a problem that can limit operating range in some other multi level configuration

Modes Of Operation

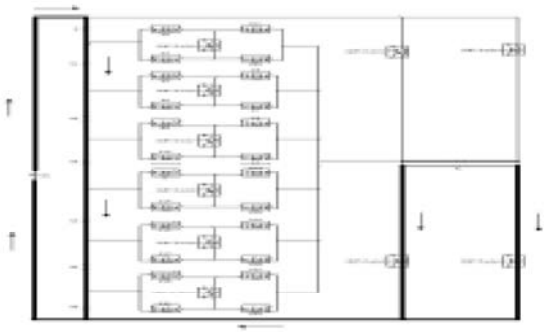

Fig. 1: MODE 0 S2 and S4 SWITCHES S2 and S4 ON CAPACITORS C1-C7 CHARGING

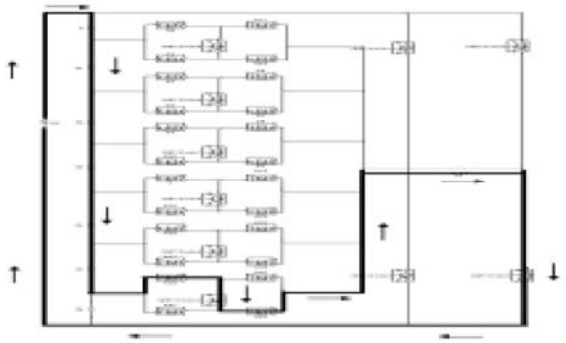

Fig. 2: MODE 1(VDC/7) CONDUCTION DEVICES (S10 and S4) SWITCHES S10 and S4 ON CAPACITORS C1-C6 CHARGING

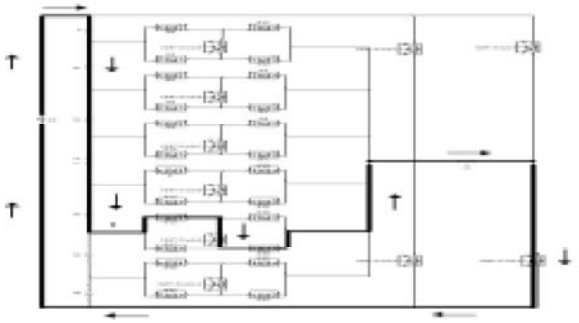

Fig. 3: MODE 2(2VDC/7) SWITCHES S9 and S4 ON CAPACITORS C1-C5 CHARGING

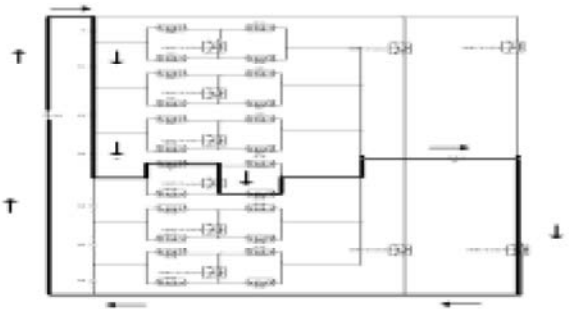

Fig. 4: MODE 3(3VD/7) SWITCHES S8 and S4 ON CAPACITORS C1-C4 CHARGING

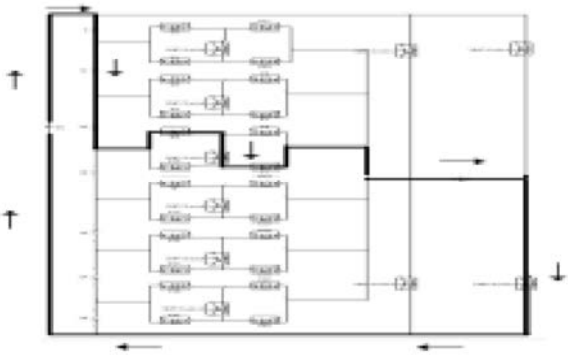

Fig. 5: MODE 4(4VDC/7) SWITCHES S7 and S4 ON CAPACITORS C1,C2,C3 CHARGING

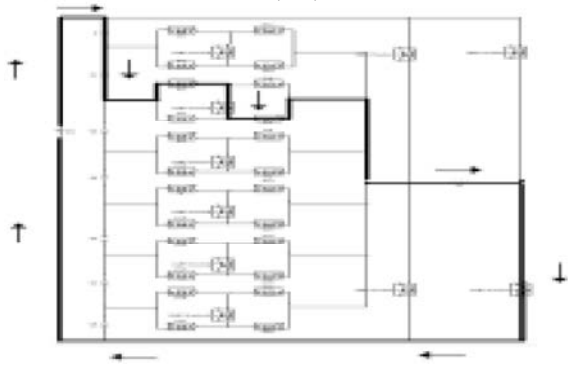

Fig. 6: MODE 5(5VDC/7) SWITCHES S6 and S4 ON CAPACITORS C1,C2 CHARGING

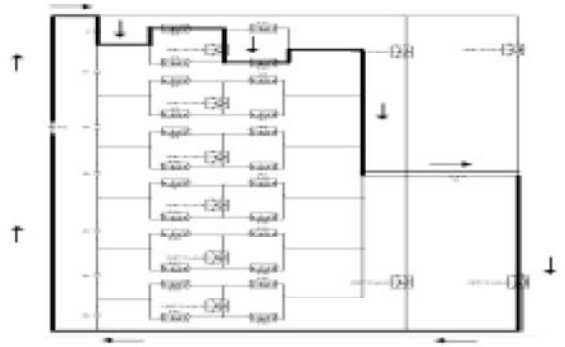

Fig. 7: MODE 6(6VD/7) SWITCHES S5 and S4 ON CAPACITORS C1 CHARGING

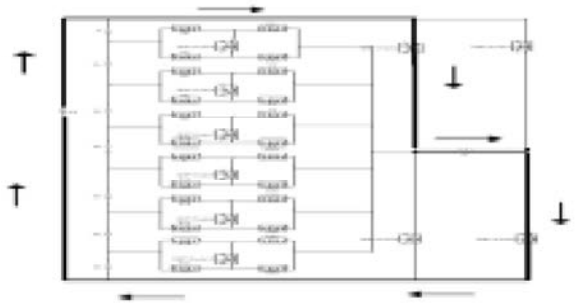

Fig. 8: MODE 7(VDC) SWITCHES S1 and S4 ON

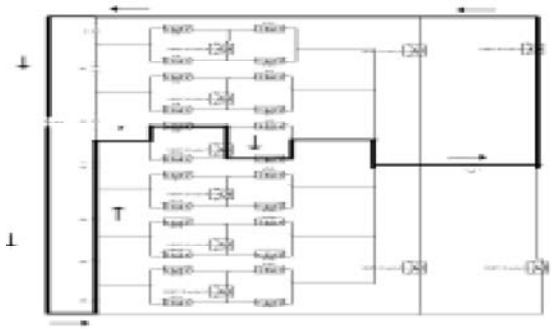

Fig. 12: MODE 11(-3VDC/7) SWITCHES S7 and S3 ON CAPACITORS C7, C6, C5, C4 CHARGING

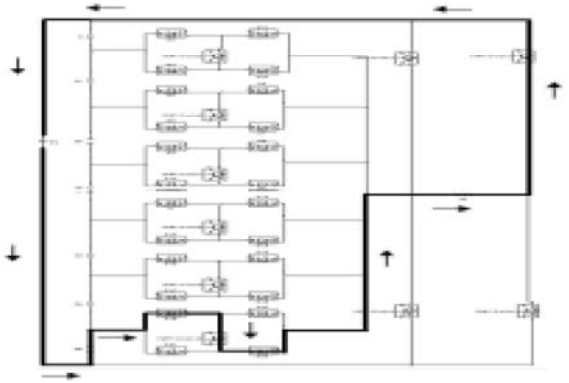

Fig. 9: MODE 8(-6VDC/7) SWITCHES S10 and S3 ON CAPACITORS C7 CHARGING

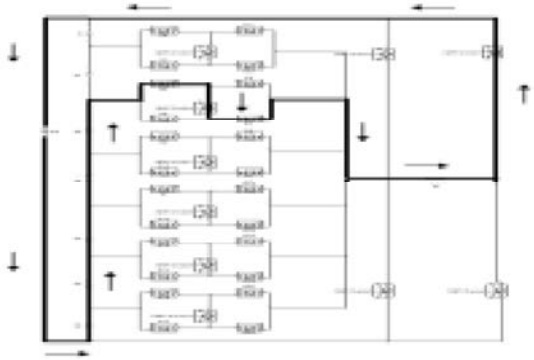

Fig. 13: MODE 12(-2VDC/7) SWITCHES S6 and S3 ON CAPACITORS C7-C3 CHARGING

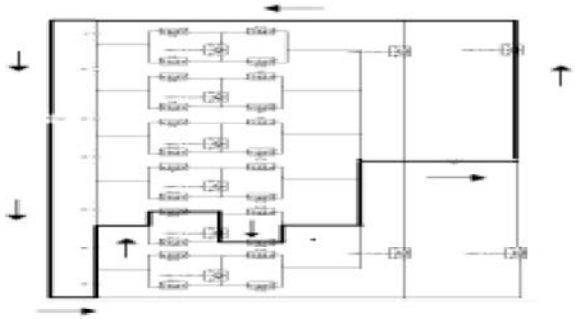

Fig. 10: MODE 9(-5VDC/7) SWITCHES S9 and S3 ON CAPACITORS C7, C6 CHARGING

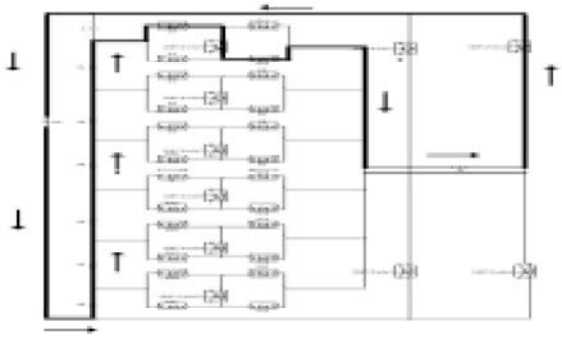

Fig. 14: MODE 13(-VDC/7) SWITCHES S5 and S3 ON CAPACITORS C7-C2 CHARGING

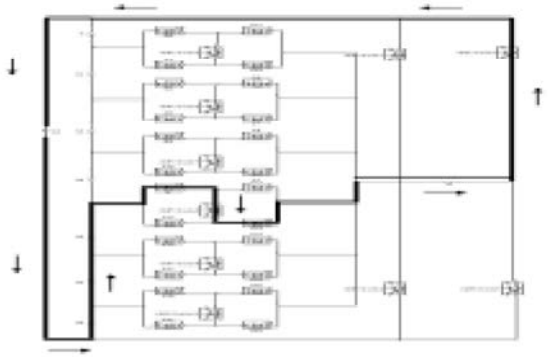

Fig. 11: MODE 10(-4VDC/7) SWITCHES S8 and S3ON CAPACITORS C7, C6,C5 CHARGING

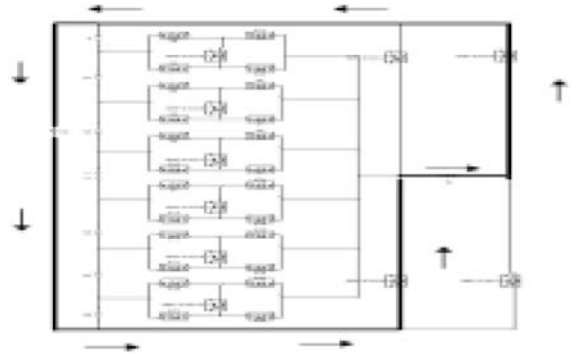

Fig. 15: MODE 14(-VDC) SWITCHES S2 and S3 ON

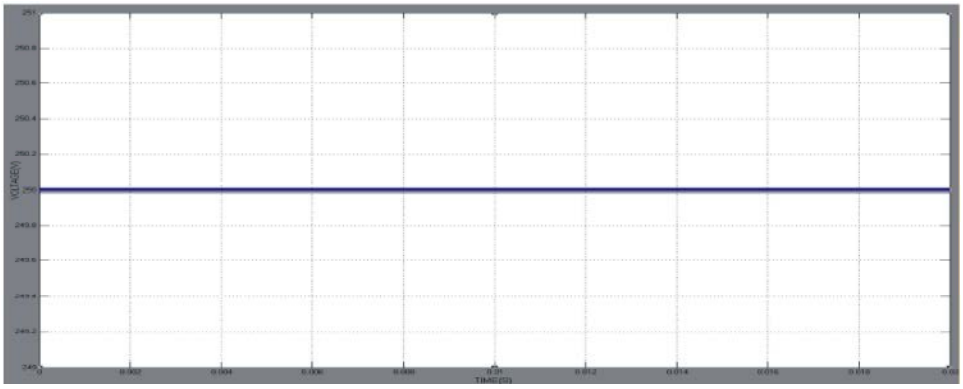

Fig. 16: Input Current

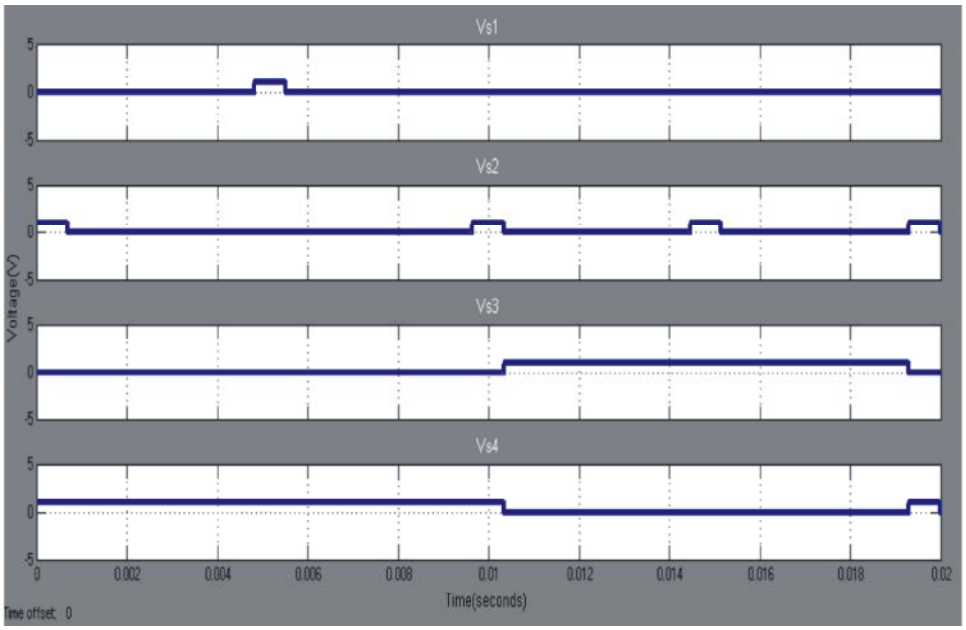

Fig. 17: Triggering Pulses 1

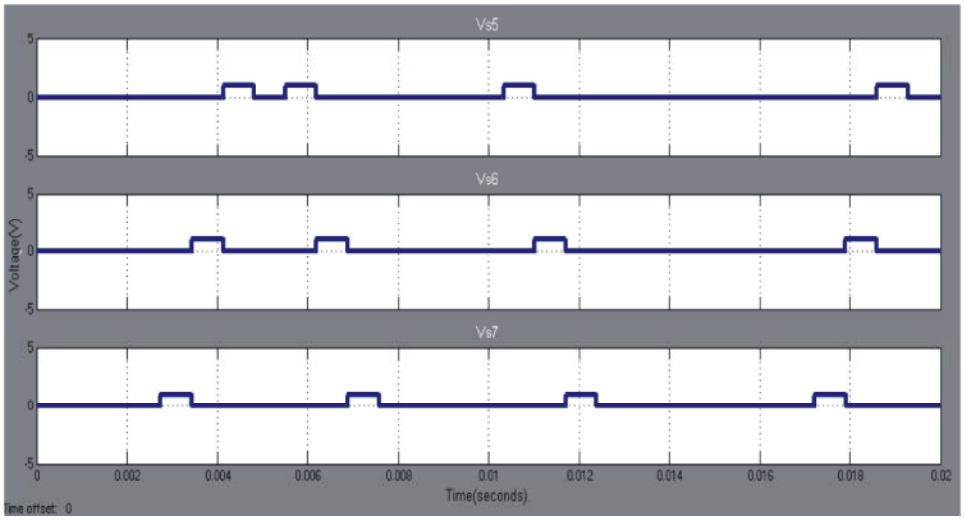

Fig. 18: Triggering Pulses 2

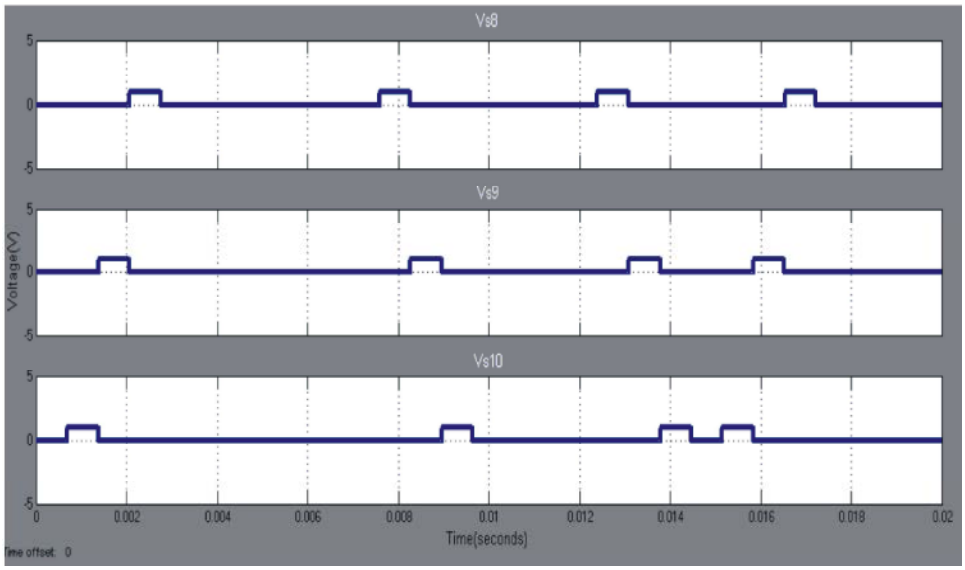

Fig. 19: Triggering Pulses 3

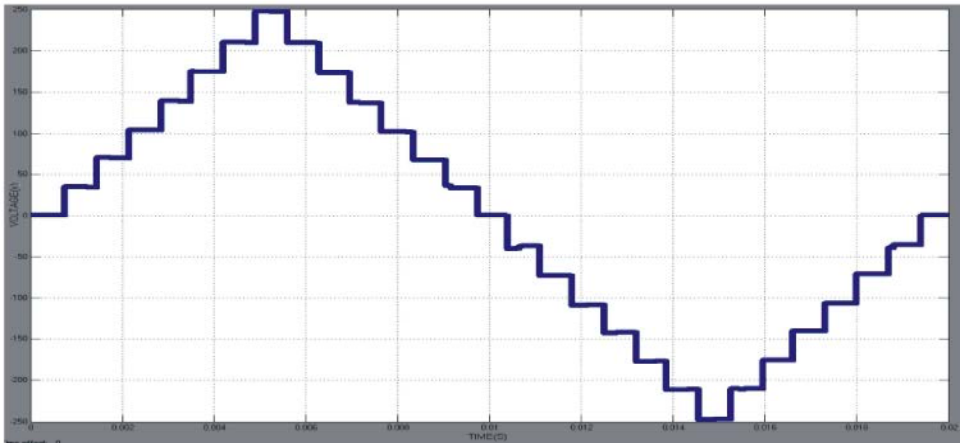

Fig. 20: Output Current

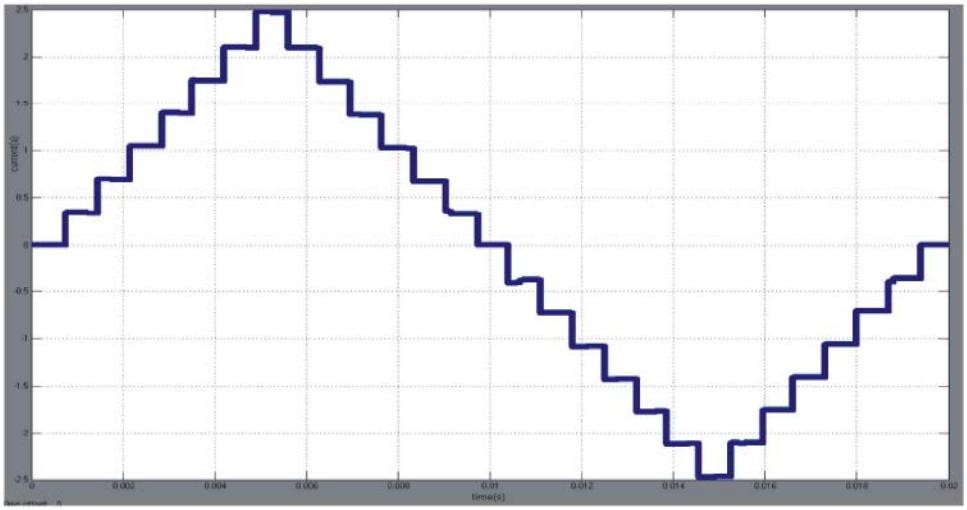

Fig. 21: Output Voltage

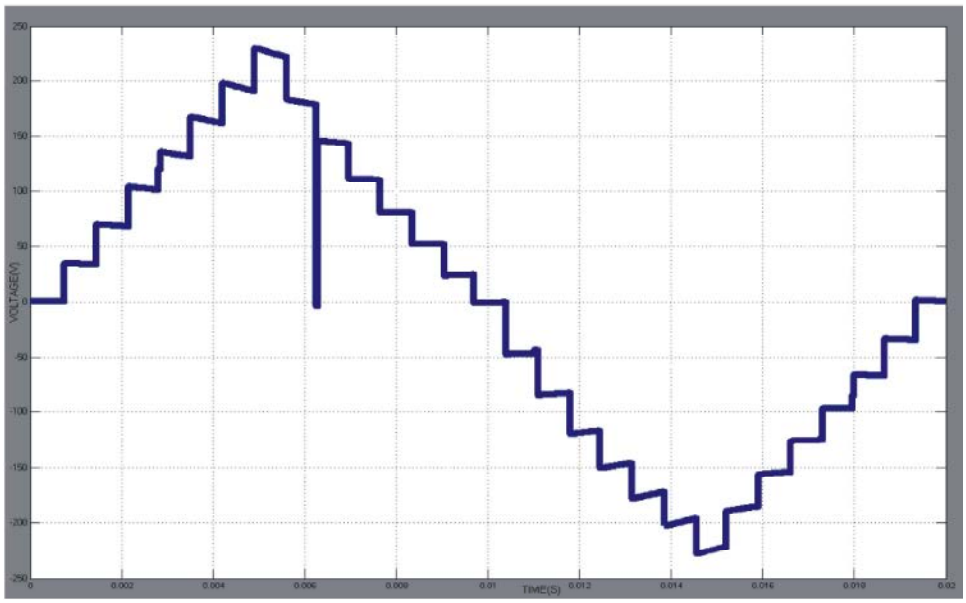

Fig. 22: R-Load Output Voltage

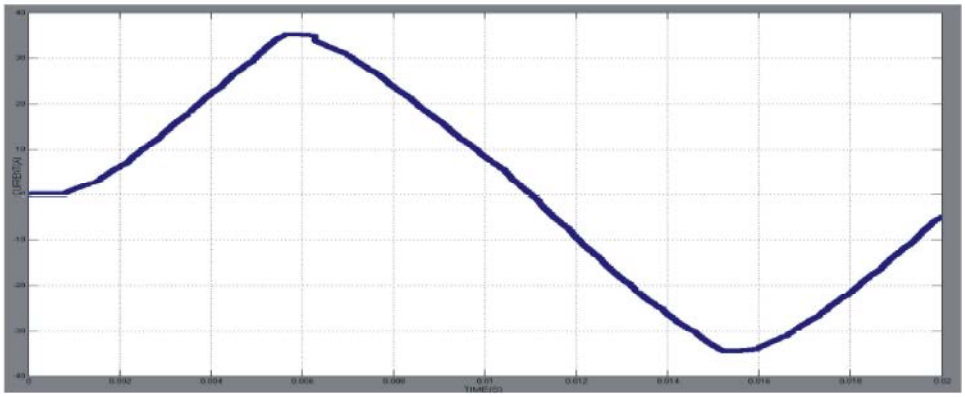

Fig. 23: Output current

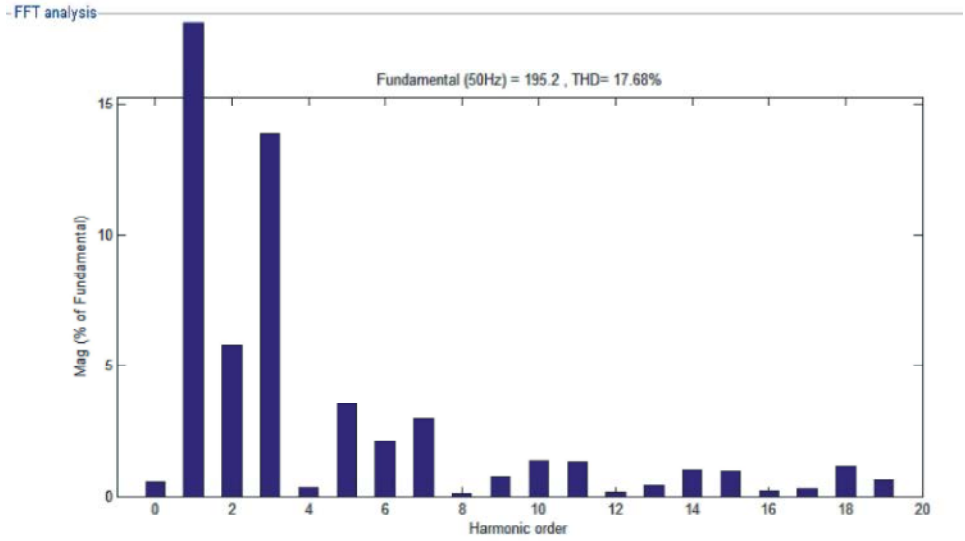

Fig. 24: Total Harmonic Distortion THD

Table 3: (buffer Measurements)

	Features		
No.	Measurements	Quantity	Unit
1	Typical IOL (sink current)	74LS 64	mA
2,	Typical IOH (source current)	74LSb15	mA
3,a)	Typical propagation delay times.Inverting	10.5	ns
3.b)	Typical propagation delay times.Non-Inverting	16	ns
4.	Typical enable/disable time	18	ns
5.	Inverting	130	mW
6.	Non inverting	135	mW

Voltage And Current Measurements: Floating channel designed for bootstrap operation Fully operational to +500V or +600V Tolerant to negative transient voltage dV/dt immune. Gate drive supply range from 10 to 20V.Under voltage lockout for both channels 3.3V logic compatible Separate logic supply range from 3.3V to 20V Logic and power ground ±5V offset.CMOS Schmitt-triggered inputs with pull-down. Cycle by cycle edge-triggered shutdown logic. Matched propagation delay for both channels. Outputs in phase with inputs, also available LEAD-FREE.

These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address Drivers, clock drivers and bus-oriented transmitters/receivers. Featuring 400 Mv of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fan out outputs and can be used to drive terminated lines down to 133X.

- TRI-STATE outputs drive bus lines directly.
- PNP inputs reduce DC loading on bus lines.
- Hysteresis at data inputs improves noise margins.

Figure Labels: Use 8 point Times New Roman for Figure labels. Use words rather than symbols or abbreviations when writing Figure axis labels to avoid confusing the reader. As an example, write the quantity "Magnetization," or "Magnetization, M," not just "M." If including units in the label, present them within parentheses. Do not label axes only with units. In the example, write "Magnetization (A/m)" or "Magnetization (A (m(1)," not just "A/m." Do not label axes with a ratio of quantities and units. For example, write "Temperature (K)," not "Temperature/K."

CONCLUSION

A multilevel inverter with single dc sources has been proposed. Simulation and experimental results have shown that with a control strategy operates the switches at the fundamental frequency, these converters have low output voltage THD and high efficiency and power factor.

In summery the main advantages of using multilevel converters for large electric drives include the following,

- They are suitable for large volt-ampere rated and /or high voltage motor drives.
- These multilevel converters systems have higher efficiency because the devices can be switched at minimum frequency.
- Power factor is close to unity for multilevel inverters used as a rectifier to convert generated ac to dc.
- No EMI problem or common mode voltage/current problem exists.
- No charge unbalance problem results when the converters are in higher charge mode or drive mode.

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