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Highly Compressed and Errorless Reconfigurable DAB/DAB+ Architecture

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Abstract: Digital audio broadcasting technology (DAB) is one of the far-reaching electronic mass media. The upgraded version of DAB is DAB+ which provides coding efficiency even in bandwidth-limited applications. In this paper, highly compressed and errorless reconfigurable DAB/DAB+ architecture is designed. Maximum likelihood path decoding along with convolutional encoding is used here for providing reliable communication and integration of the embedded transition inversion (ETI) technique in the extended frequency directed run-length encoding is to increase the compression ratio of the test vectors. The proposed design is implemented in Cyclone II EP2C15AF484C6 of FPGA family using Modelsim and Quartus II of Altera 6.4a. The low power dissipation and high compression ratio is achieved here.

Key words: Digital audio broadcasting (DAB) · Maximum likelihood path decoding · Embedded transition inversion · Extended frequency directed run-length encoding

INTRODUCTION

Over the last few years, Digital Audio Broadcasting (radio broadcasting technology) has evolved rapidly in many countries due to its ever increasing demands. DAB+ is the advanced standard of DAB and hence receivers are required to be compatible with both standards. In this paper, a highly compressed and errorless reconfigurable DAB/DAB+ architecture is designed.

To achieve the superior audio quality, the DAB system adopted MPEG1- Layer II (MP2) as its audio standard whereas the DAB+ system adopted high-efficiency advanced audio coding version 2 (HE-AAC V2) as its audio coding standard. HE-AAC V2 includes advanced audio coding (AAC) low complexity (LC) profile, parametric stereo (PS) and spectrum band replication (SBR) technologies which provide the coding efficiency.

Generally in digital communication systems, two types of coding are used. They are source coding and channel coding. In source coding redundant bits are removed in order to promote the transmission capacity and conserve the channel resource whereas in channel coding redundant bits are added in order to provide reliable communication.

Finite state transition convolution encoder and embedded transition inversion technique in the extended frequency directed run-length encoding is our proposed design in reconfigurable DAB/DAB+ architecture. The channel is more prone to errors and hence to provide reliable communication channel coding is used. Finite state transition convolution encoder and maximum likelihood path decoding is used to obtain errorless data at the receiver side. In modern electronic systems, by compressing the audio data, the audio information can be transferred efficiently. For data compression transition inversion technique in the extended frequency directed run-length encoding is used.

The rest of the paper is designed as follows. In section II, some of the audio coding techniques have been discussed briefly. In Section III, a highly compressed and errorless DAB/DAB+ multimedia processor is proposed and reconfigurable transmitter and receiver architecture is described. The analysis of the parameters and simulation results are shown in Section IV. In Section V, the inference of the paper is stated.

Related Works: Some of the audio coding techniques are briefly discussed in this section. In low bit-rate encoders, the perceptual audio coding (PAC) [1] removes the redundant information which leads to compression. To achieve the superior audio quality, the DAB system adopted MPEG1- Layer II (MP2) as its audio standard. By using HE-AAC [2] i.e., AAC-LC profile and SBR technology, the superior audio quality has been achieved even at low bit rates. In bandwidth limited applications, the coding efficiency is further optimized by designing

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HE-AAC V2 [3]. The high stereo quality is obtained in [4] where the MP2 and AAC-LC are used for designing DAB/DAB+ audio decoder.

The ½ code rate [5] convolutional encoder and Viterbi decoder is designed and hence reliable communication is achieved. The power dissipation is reduced by optimizing the switching activity. In [6], the encoding technique is utilized which minimizes transitions while transferring the data blocks. The power dissipation is reduced by optimizing the switching activity. In [6], the encoding technique is utilized which minimizes transitions while transferring the data blocks. In the transition inversion coding (TIC), the extra word is used to indicate when the bit inversion occurs. But in ETI [7], the phase difference indicates the bit inversion.

Compression is done with the help of input compression and output compaction. Data compression involves lossless and lossy compression methods. The data compression technique is used to store or to send a smaller number of bits. Lossless compression is the RLE method. In the run length encoding, five different approaches [8] are there for the filling of "don't care" bit. The method used to increase the frequency of runs of 0s is the Simple run length code. In this method, the careful ordering of test cubes increases the number of 0s, which helps to enhance the run-length coding efficiently. The next method is the Golomb code which helps to overcome the disadvantages of the simple run-length coding method. In this, the code words are divided into groups and each group has a separate prefix and tail in the end. The use of this approach is for the longer runs. To control the problems in this approach, the frequency directed run-length encoding is generated. From this method, the encoding is based on the runs of 0's. The frequency directed run-length code [9] consist of the prefix and tail with equal sized code words. In this method, predicts only the runs of 0's so called as an extended frequency directed run-length Is used and this helps in both runs of 1's followed by 0's and 0's followed by 1's. The main disadvantage in this method is we cannot generate the random numbers so we use transition inversion technique to integrate with the extended frequency directed run-length encoding.

Proposed System: The highly compressed and errorless reconfigurable DAB/DAB+ is described here. The channel is more prone to errors and hence to obtain reliable communication maximum likelihood path decoding is used. Data compression involves many methods; Run Length Encoding (RLE) is one of them. RLE is a simple form of data compression technique, which runs the data are stored as a single-valued data, rather than the original run. Embedded transition inversion (ETI) increases the bit transition. This ETI is able to increase the 0's transitions. Integration of the embedded transition inversion technique in the extended frequency directed run-length (EFDR) encoding is to increase the compression ratio of the test vectors. This paper focuses on transmitter and receiver architecture for achieving high compression and error-free data respectively.

The reconfigurable DAB/DAB+ transmitter architecture, Fig. 1, is designed using convolutional encoder and EFDR based embedded transition inversion encoder. Using the convolutional encoder, the ½ code rate is obtained which is one of the forward error correction techniques. In this proposed work, we use a technique known as the ETI. This helps in reduction of power and very efficient in reducing the number of 0s while inverting the data. The test patterns are generated using the automatic test equipment then the don't care bits are filled by 1s and 0s. Then the number of 1s and 0s are calculated for inversion, the inversion occurs depending upon the values of 1s and 0s. After inverting the number of 0s is reduced, this helps in further compression of the data. Then the codes are given on the inverted data using EFDR technique.

The reconfigurable DAB/DAB+ receiver architecture is depicted in Fig. 2. The encoded data is transmitted through the channel where there is a chance of manipulating the data. Hence to avoid it maximum likelihood path Viterbi decoding is used at the receiver side to combat from errors. The de-interleaver is used to overcome from burst errors. Finally the decoded DAB and DAB+ data (original input data) are stored in their respective memory banks and come out through the speaker as audio.

Convolutional Encoder and Viterbi Decoder: The Convolutional Encoder along with maximum likelihood path decoder is one of the forward error correcting codes. It helps to combat from errors which occur during transmission of data through the channel.

The shift registers are the principle components of Convolutional encoder, which encodes the input data of code rate ½. The implementation of a Convolutional encoder is shown in Fig. 3, here C1 and C2 are the encoded data. The operation of an encoder is represented in the form of trellis diagram and is depicted in the Fig. 4. Here the solid edges represent 'input 0' and dashed edges represent 'input 1'.

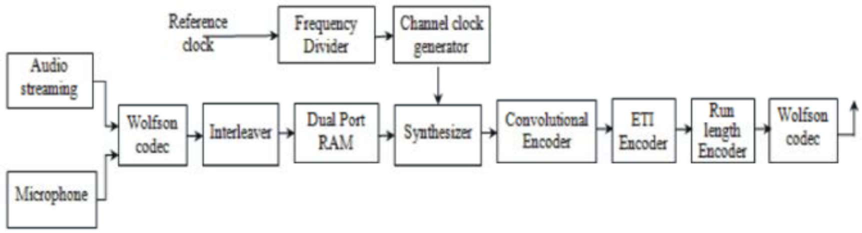

Fig. 1: Transmitter Architecture

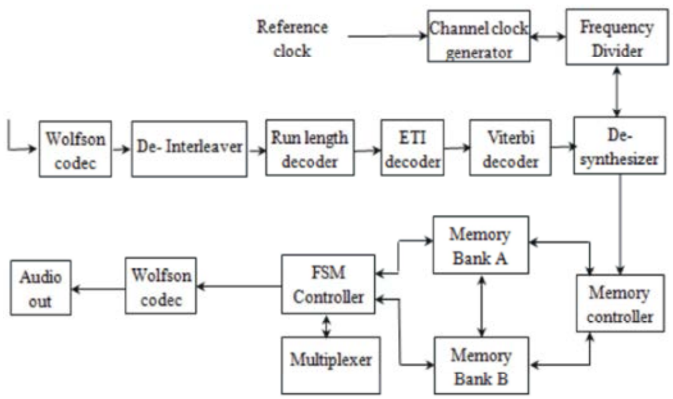

Fig. 2: Receiver architecture

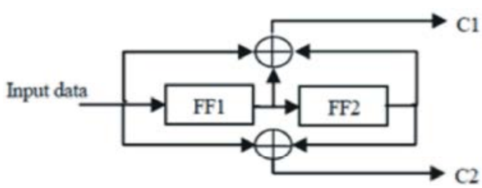

Fig. 3: Convolutional Encoder

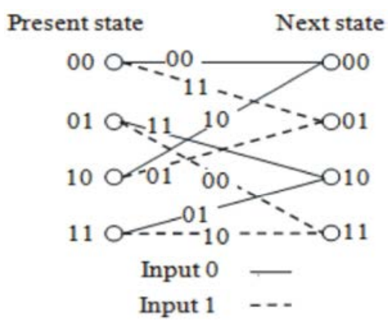

Fig. 4: Part of Trellis diagram

The maximum likelihood path Viterbi decoder is used to estimate the original transmitted data. When the stream of data is transmitted through the channel there may be a chance of getting errors in the data and hence using trellis diagram the data can be recovered from errors. The branch metric unit (BMU), add compare and select unit (ACS), survivor memory unit (SMU) and traceback unit (TBU) are the functional units (Fig. 5) which is used to compute the original message sequence.

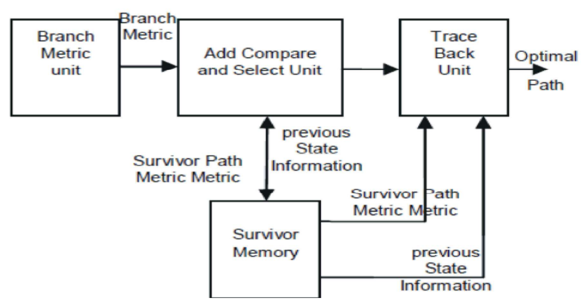

Fig. 5: Block diagram of Viterbi decoder

The steps to recover data from errors are mentioned below.

Step 1: The received two binary bits are given as input to the decoder and then BMU calculates the hamming distance of each node. Each node has two values i.e., each current state has two possible paths.

Step 2: The ACS module is used to find the cumulative hamming distance of each node. It then compares and the smaller is chosen as survivor, which is used for further computations.

Step 3: Those survivor paths are stored in SMU. Finally at the last stage, using minimum path metric the survivor paths are traced back by TBU. Thus, the original input data is recovered from errors.

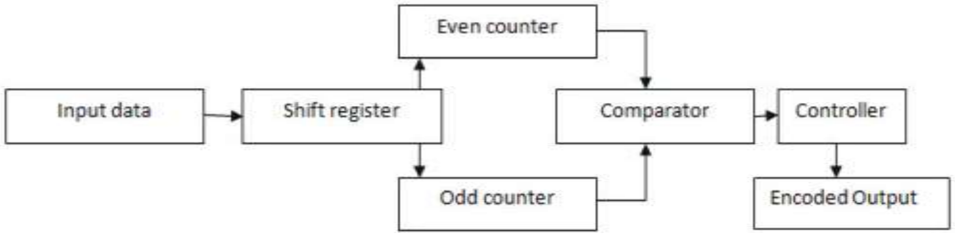

Fig. 6: ETI encoder for proposed system

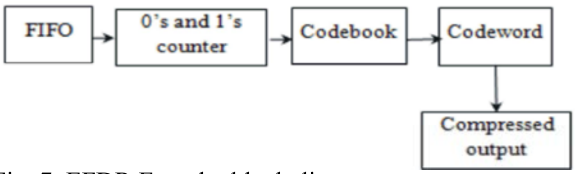

Fig. 7: EFDR Encoder block diagram

ETI Encoder and Decoder: Embedded transition inversion is a technique used to invert the data that is present on the tester. The switching activity is reduced in transition inversion coding (TIC) [6], but when inversion occurs extra bit is required to indicate bit inversion. Hence to avoid overhead ETI is used, which uses phase difference to indicate inversion. ETI increases the bit transition. This ETI [10] is able to increase the 0's transitions by 50% when compared to the existing method [6]. The block diagram of ETI encoder is shown in the Fig. 6.

This ETI encoding involves odd inversion, even inversion, no inversion, full inversion and is done based on the 1's and 0's. If the number of 1's is greater than 0's then full inversion takes place. If the number of 1's is equal to 0's, then half inversion occurs depending upon the positions of 1's. If the number of 0 is greater than 1, then will be no inversion. Embedded transition inversion helps to increase the compression ratio and helps in increasing the runs of 0's. Based on the inversion the decoding process takes place i.e., odd invert, even invert, full invert and on invert.

Extended Frequency Directed Run Length Encoder: Run-length encoding is a method used to compress data and this method is very efficient when the data's are represented as 1's and 0's.This method is used to replace the consecutive repeating occurrences of a symbol. There are different types of run-length used to compress data; one among them is that frequency directed run-length (FDR) encoding. This FDR encoding helps to compress data depending on the frequency of runs of 0s. The codeword is given for both prefix and suffix. They are splitted into groups depending upon the size of the test data. The extension to the FDR is that EFDR encoding.

TABLE I

EFDR CODE

Group	Run Length	Group Prefix	Tail	Code Word Runs of 0's	Code Word Runs of 1's
A_1	1	0	0	000	100
	2		1	001	101
A_2	3	10	00	01000	11000
	4		01	01001	11001
	5		10	01010	11010
	6		11	01011	11011
A_3	7	110	000	0110000	1110000
	8		001	0110001	1110001
	9		010	0110010	1110010
	10		011	0110011	1110011
	11		100	0110100	1110100
	12		101	0110101	1110101
	13		110	0110110	1110110
	14		111	0110111	1110111

In this, it further compress the test data present on the tester since it works on both the runs of 0s as well as the runs of 1s. Compared to all the methods in the run-length EFDR coding is more efficient.

EFDR coding is used in an efficient way that is this involves both the runs of 0's as well as the runs of 1's. This approach is an extension of the frequency directed run-length coding [8]. The EFDR encoder diagram and EFDR code is shown in the Fig. 7 and Table 1 respectively. This helps to obtain more number of 0's since this involves both the number of 0's, as well as 1's. This is more efficient when compared with all the approaches used in the run-length encoding. This is integrated along with the transition inversion technique to overcome all the drawbacks that are present in these approaches.

Result and Analysis: From the Fig. 8, it clearly shows that the high compression is achieved using embedded transition based EFDR technique. It is analyzed using Cyclone II EP2C15AF484C6 of FPGA family. Here the input data is represented as data_in and the encoded data is represented as cw. The data is encoded using Table 1. The input data is given and based on the number of 1's and 0's, the encoded data i.e., compressed data is obtained.

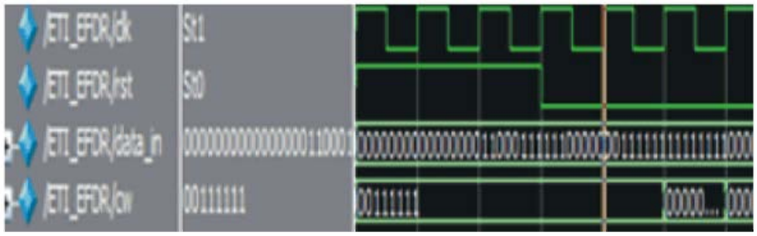

Fig. 8: Simulation result of ETI based EFDR

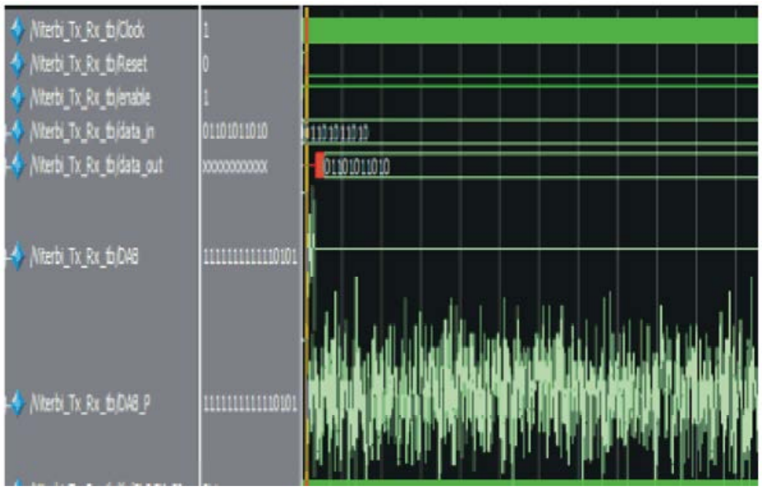

Fig. 9: Simulation result of reconfigurable DAB/DAB+ architecture

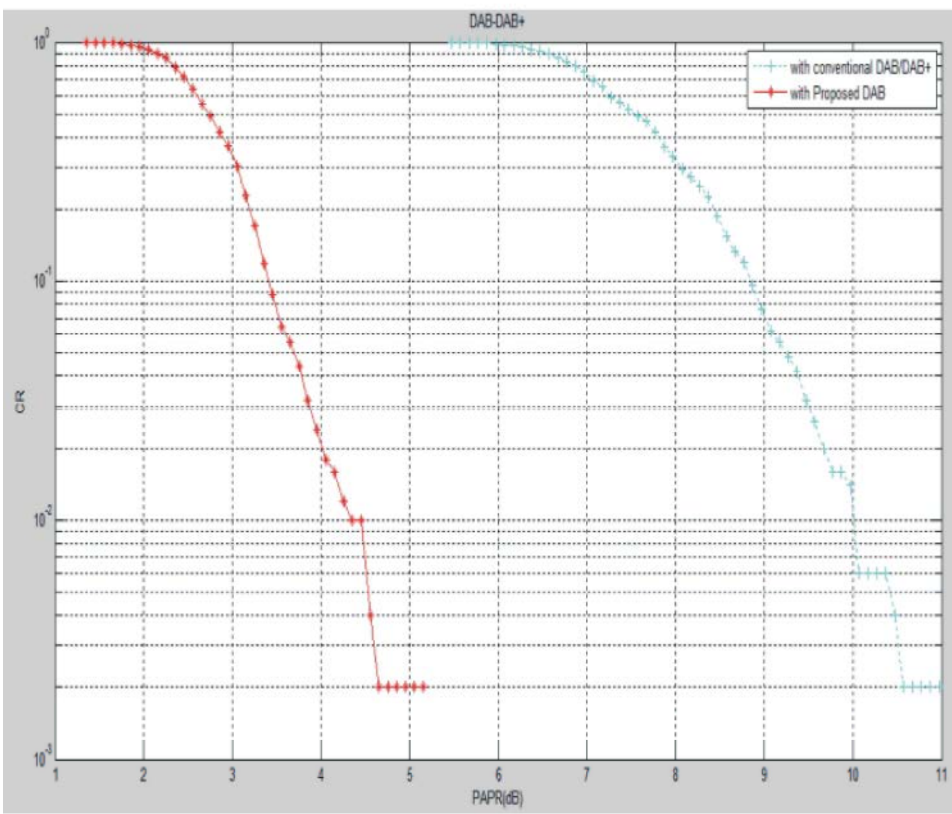

Fig. 10: Compression ratio graph for proposed architecture

TABLE II

PERFORMANCE ANALYSIS OF ETI BASED FDR AND EFDR TECHNIQUE

Parameters	ETI based FDR technique	ETI based EFDR technique
Dynamic PD (mW)	12.13	3.25
Static PD (mW)	47.46	18.04
I/O PD (mW)	68.33	24.92
Total PD (mW)	127.91	46.22

The simulation results of error free DAB/DAB+ reconfigurable architecture is shown in the Fig. 9. It is simulated in ModelSim Altera 6.4a. Here data_in and data_out are same. Thus, the reliable communication is obtained using Convolutional encoding and maximum likelihood path decoding technique.

The peak amplitude power ratio (PAPR) is the ratio of the maximum power of a sample in a DAB/DAB+ transmit symbol to the average power of that received symbol. PAPR reduction and compression ratio (CR) of the proposed approach varies according to the requirement of the system. From the graph (fig 10), it is inferred that the proposed ETI based EFDR reconfigurable DAB/DAB+ architecture, which is indicated in red color solid line, has high CR than the ETI based FDR. Table II also implies that the proposed design power dissipation is only 46.22mW. Hence, the proposed design is more efficient and used for reliable communication.

CONCLUSION

The highly compressed and errorless reconfigurable DAB/DAB+ architecture is designed. From the simulation results, it is inferred that ETI based EFDR technique is used to achieve high compression and reliable communication can be achieved by using maximum likelihood path decoding. It also implies that the proposed design power dissipation is only 46.22mW which is more efficient than the ETI based FDR technique. Hence, the proposed reconfigurable DAB/DAB+ architecture will definitely offer simplicity to the digital radio industry.

REFERENCES

1. Herre, J., 1999. "Temporal noise shaping, quantization and coding methods in perceptual audio coding: A tutorial introduction," in Proc. AES 17th Int. Conf. High Qual. Audio Coding, pp: 312-315.
2. Herre, U. and M. Dietz, 2008. "MPEG-4 high-efficiency AAC coding," IEEE Signal Process. Mag., 2(3): 137-142.
3. Meltzer, S. and G. Moser, 2006. "HE-AAC v2-Audio coding for today's digital media world," EBU, Geneva, Switzerland, Tech Rev., pp: 305.
4. Guoyu Wang, Hongsheng Zhang, Member, IEEE, Mingying Lu, Chao Zhang, Tao Jiang and Guangyu Guo, 2014. "Low-Cost, Low-Power ASIC Solution for Both DAB+ and DAB Audio Decoding," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 22(4).
5. Rohan M. Pednekar and B.M. Dayanand, 2013. "Design and Implementation of Convolution Encoder with Viterbi Decoder," Int. J. of Emerging Technologies in Comp. and Applied Sciences.
6. Abinesh, R., R. Bharghava, Suresh Purini and Govindarajulu Regeti, 2010. "Transition Inversion based Lower data coding scheme for Buffered Data Transfer," Conference Proceedings, 23rd VLSI Design-9th Embedded Systems.
7. Chennakesavulu, M. and A. Raghavi, 2014. "Design and Analysis of Effective Coding Technique for Serial Links," Int. J. of Science and Research, ISSN (online): 2319-7064, 3(4).
8. Usha S. Mehta, Kankar S. Dasgupta and Niranjan M. Devashrayee, 2010. "Run-Length-Based Test Data Compression Techniques: How Far from Entropy and Power Bounds?—A Survey," Hindawi Publishing Corporation, VLSI Design, Vol. 2010, Article ID 670476.
9. Anshuman Chandra and Krishnendu Chakrabarty, 2003. "Test data compression and test resources partitioning for system-on-a-chip using frequency directed run length (FDR) codes," IEEE Transactions on Computers, 52(8).
10. Jacob, Ebbipeni and N. Bamakumari, 2014. "Design and Implementation of Area and Power Efficient Transition Inversion Coding For Serial Links," Int. J. of Comp. Engg. Research, 04(2).