Middle-East Journal of Scientific Research 23 (Sensing, Signal Processing and Security): 97-101, 2015
ISSN 1990-9233

DOI: 10.5829/idosi.mejsr.2015.23.ssps.24

On Chip SC DC-DC Converter with Single Input Multiple Output

[1]P. Suresh and [2]S. Karunakaran

[1]Department of Electronics and Communication Engineering,
Saveetha Engineering College, Chennai, India
[2]Department of Electronics and Communication, Saveetha Engineering College, Chennai, India

Abstract: In this paper, the On-chip DC-DC converter is implemented in order to improve the performance of the Multicore processor. A single input voltage is converted using on-chip SC DC-DC Converter into variable output voltage. Switched Capacitor plays a major role in DC-DC conversion. The significance of this conversion process is to improve the overall performance of the multi-core as well as to reduce the number of pins used for the power supply. This paper is designed in Verilog HDL code and is widely used in Multicore Systems.

Key words: Switched Capacitor (SC) and Direct Current (DC)

INTRODUCTION

Different supply voltages is needed for multicore processor having many cores for parallel processing and also due to low and high power digital and analog circuits because of increased transistors count. Here no need for off chip converter which increases cost and size, we are implementing on chip converter for producing various outputs using voltage scaling technique On chip converter reduces the number of supply pins. Linear regulators have been widely used for on-chip DC-DC converters [1]. However, the most significant drawback of linear regulators is their linear efficiency drop with increasing dropout voltage. Therefore, the alternatives are required to achieve high efficiency across a broad range of output voltages. Since the on-chip capacitors have significantly higher quality factor, higher energy density and lower cost than on-chip inductors in standard CMOS process, SC based on-chip converter have been receiving increased attention from both in academia and industry [2].

Traditionally the digital arrangement and processor working alongside a steady input supply voltage. We arranging the converter for several cores/multiple digital routes that need several working voltage the reconfigurable converter utilized for multicore processor possessing three variable outputs. But multicores needs input power simultaneously [2]. So, SC DC-DC Converter is projected alongside nine variable outputs, which gives three outputs simultaneously alongside solitary input. The synchronous buck converter is a extensively utilized topology in low-voltage, high-current applications [4]. Low-power loss and exceedingly effectual synchronous buck converters are in outstanding demand for advanced microprocessors of the future. Good understanding of power defeats in a synchronous buck converter is critical for enhancing converter performance. This request report analyzes MOSFET-related power defeats in a synchronous buck converter [5].

DC-DC Converter: There are countless disparate kinds of DC-DC converter, DC-DC converters are electronic mechanisms utilized whenever we desire to change DC mechanical power effectually from one voltage level to another. Here we are employing is SC DC-DC converter lacking employing inductor that has less IR drop [4].

SC Converter: Switched capacitor (SC) converters have come to be accepted for on-chip power conversion as no inductors, that on-chip are colossal and tough to produce alongside sufficiently low defeats, are needed [6]. Employing merely switches and capacitors obtainable in the knowledge, SC converters have the possible to encounter the severe power density and efficiency necessities set by the microprocessor power specification. The operation of step down converter using switched capacitor is shown in Fig 1.

Corresponding Author: P. Suresh, Department of Electronics and Communication Engineering,
Saveetha Engineering College, Chennai, India.

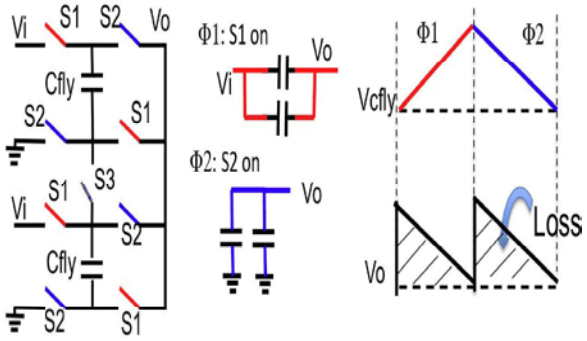

Fig. 1: Basic 2V:1V step-down switched capacitor converter and the operational waveforms

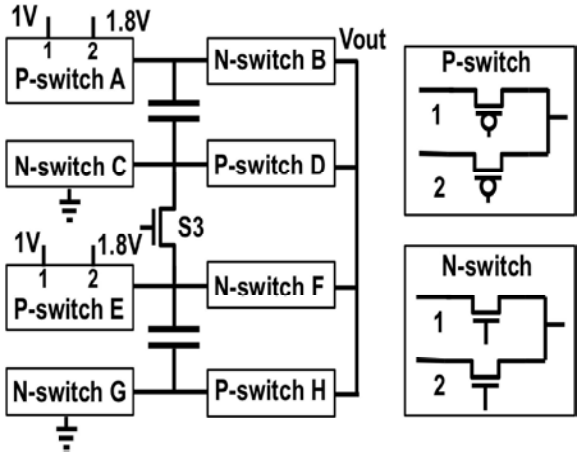

Fig. 2: Single input single output voltage reconfigurable SC DC-DC converter with threshold voltage 1V and 1.8V.

Table 1: Employed switches for each configuration

Conf	Threshold voltage	φ1	φ2
Conf1	1.8V	A2,D2,E2,H2	B2,C2,F2,G2
Conf2	1V	A1,D1,E1,H1	B1,S3,G1
Conf3	1V	A1,D1,E1,H1	B1,C1,F1,G1

DC–DC Converter Circuit Design: Our design is crafted concerning a reconfigurable SC dc–dc converter employing MOS capacitors in 28-nm FDSOI knowledge and it has three disparate configurations: 2–1 and 3–2 topologies working off a 1 V input and a 2–1 topology working off a 1.8 V input. To elucidate the key defeat mechanisms, here onset by scrutinizing the procedure of 2:1 step-down reconfigurable converter is shown in Fig. 2. The specific details of the SC route design are endowed in fig.2. For the 2:1 conversion, the switch S3 is always OFF. The converter operates in two non-overlapping periods φ1 and φ2. The equivalent waveforms on the capacitor and at the output [5] are shown in Fig 2.

Losses in Switched Capacitor Converter: The main SC converter power defeats are conduction losses from charging and emitting the hovering capacitor and switching losses from the parasitic bottom plate capacitor, the transistor parasitic gate-source and drain-source capacitances and the gate driver. As the MOSFET switches on and off, it's intrinsic parasitic capacitance stores and next dissipates power across every single switching transition. The defeats are proportional to the switching frequency and the benefits of the parasitic capacitances. As the physical size of the MOSFET increases, its capacitance additionally increases; so, rising MOSFET size additionally increases switching loss [5].

Conduction Losses: The charging and emitting of the hovering capacitor across Req is a lossy procedure that aftermath in conduction defeats, that are encompassed in the output present scutiny above by the exponential words in k. Due to present balance of the hovering capacitor [6],

The output present is

$I_{out} = 2I_{in}$

And the emerging converter efficiency becomes

$ç = P_{OUT}/P_{in} = V_{OUT}I_{OUT}/V_{IN}I_{IN} = 2V_{OUT}/V_{IN}$

Hence, equation displays that the efficiency after encompassing conduction losses is given by the input and output voltage specifications only.

Loss Optimization in Standard DC–DC Converter: In a fully consolidated SC dc–dc converter, several switching phases are utilized to cut the output ripple [5]. We are referring to this kind of converter as the standard interleaved or just standard converter. Optimizing the converter needs selecting the capacitor size Cfly, the switches size W_{sw} and the switching frequency f_{sw}. The capacitor size is normally fixed by the chosen power density. Domination density embodies the ratio amid the converter output power and its span and is a functional metric for computing converter span overhead for a given processor power. To accomplish re-configurability, we embed two identical sub converter unit cells into one, as shown in [5]. Two sets of switches are utilized for larger power efficiency: one set for the configurations working off a 1 V (set 1) and the supplementary set for the configuration working off a 1.8 V (set 2).

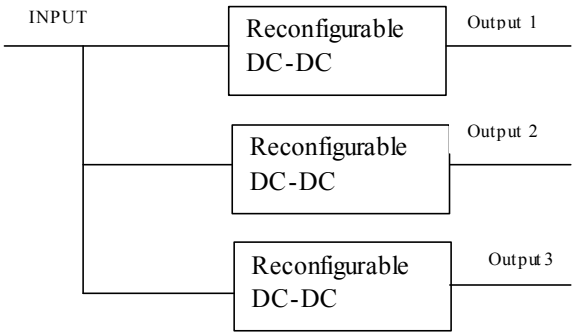

Fig. 3: Single input multiple output DC-DC Converter Block Diagram

Table 2: Configuration for single input single output DC-DC Converter

Conf	Voltage input	Voltage output	Threshold voltage	Switch condition (S3)
Conf1	2V	1V	1.8V	1
Conf2	3V	2V	1V	1
Conf3	2V	1.2V	1V	0

Single Input Multiple Output DC-DC Converter: For the present DC-DC converter using Dynamic voltage scaling gives three variable outputs, which is very efficient converter using switched capacitor with high efficiency designed for multi-core processor. But converter gives single input at a time so many converters needed to be designed with separate outputs, So the proposed design is connecting the converters in parallel, which gives single input multiple output having three configurations which gives nine variable outputs from 5V as a input by differentiating threshold voltage and varying switch conditions. Output voltages with different threshold voltages are designed using different switch conditions. Our design is single input three output is designed by connecting reconfigurable DC-DC converter in parallel is designed based on this block diagram shown in Fig. 3.

RESULTS AND DISCUSSIONS

An on-chip DC-DC Converter is designed using Verilog HDL and simulated in modelsim software power is estimated using Quartus tool.

On-chip converter with three variable outputs using three different configurations shown in Table 2. Table 2 description is given below

- In configuration1 2V-1V is converted using threshold value 1.8V with switch(S3) condition is on represented.
- In configuration2 3V-2V is converted using threshold value 1V with switch(S3) condition is on
- In configuration1 2V-1.2V is converted using threshold value 1V with switch (S3) condition is off as shown in Fig. 4.

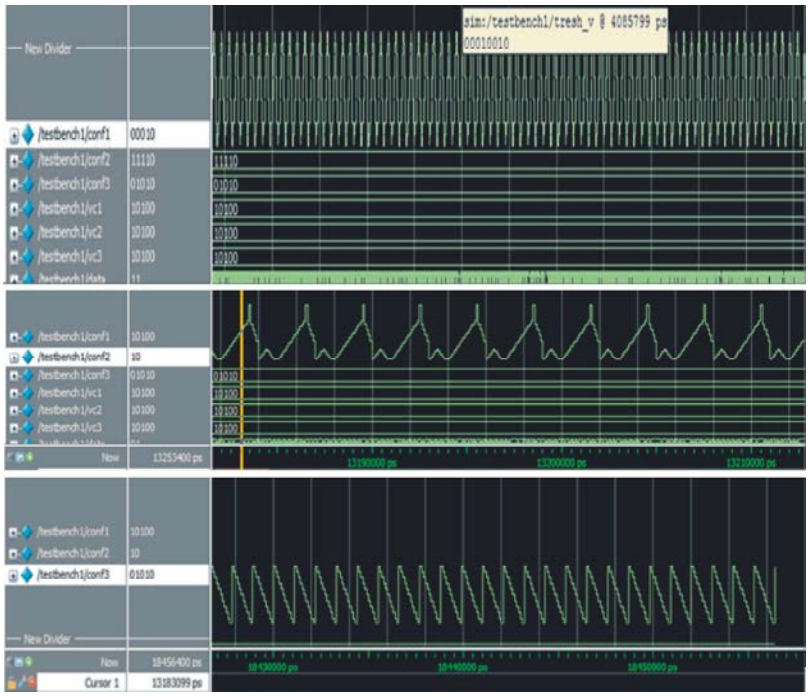

Fig. 4: Simulation result for single output three different configuration based on table 1 with three outputs 1V,2V,1.2V

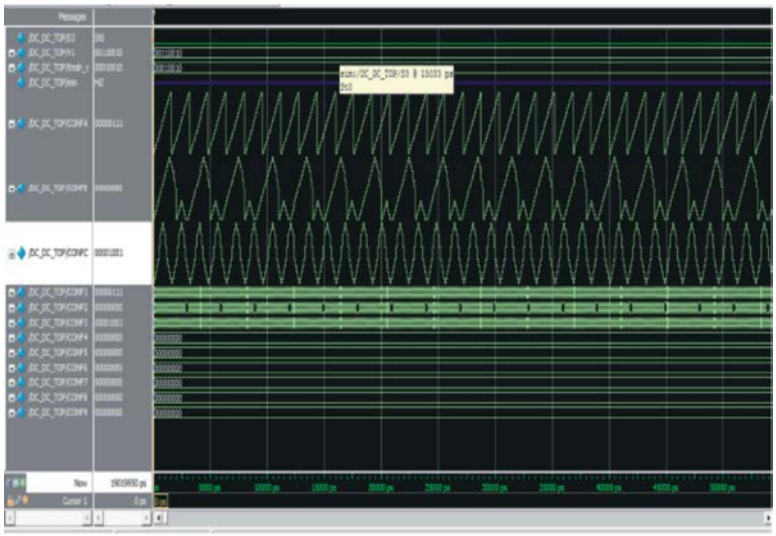

Fig. 5: Simulation waveform Configuration1 for multiple output 2.5V,1.5V,1V with 1.8V Vt and S3 is 0

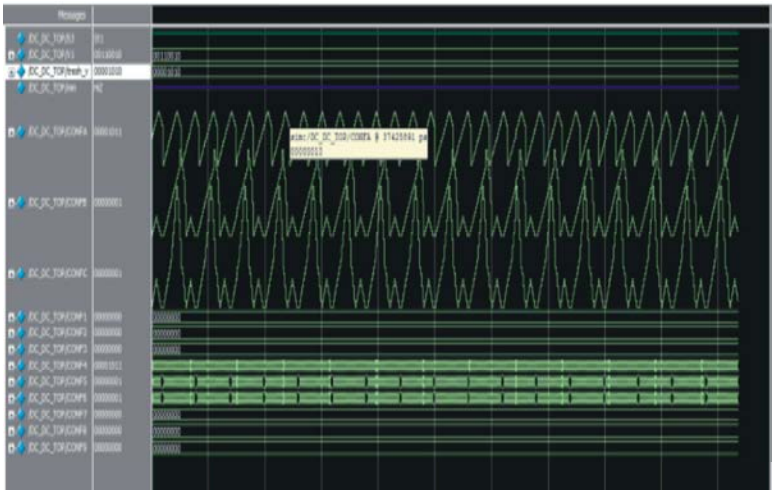

Fig. 6: Simulation waveform for Configuration 2 with multiple output 1.2V,1.8V,2V with 1V Vt and S3 is 1

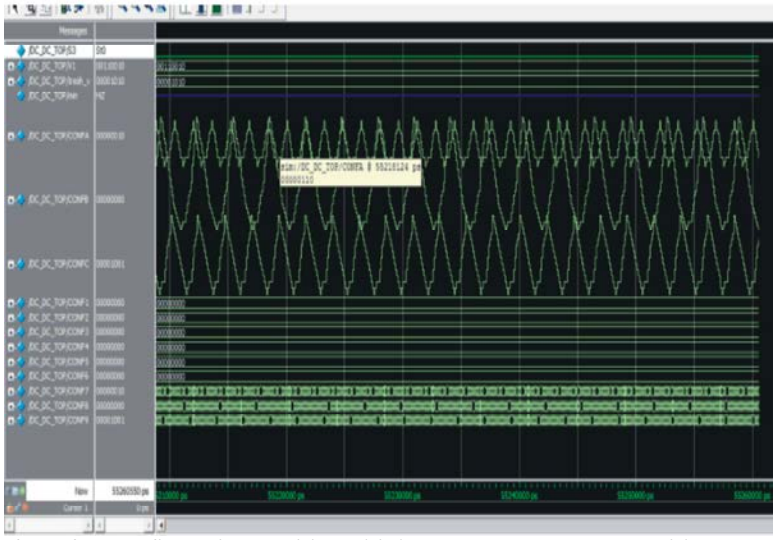

Fig. 7: Simulation waveform for Configuration 3 with multiple output 1.4V,2V,1.6V with 1V Vt and S3 is 0

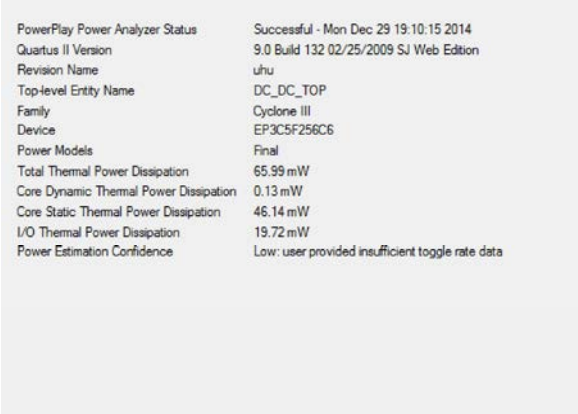

Fig. 8: Power report for single input multiple output DC-DC Converter

Table 3: Configuration for single input multiple output DC-DC converter.

Conf	Voltage input	Voltage output	Threshold voltage	Switch condition (S3)
Conf1	5V	2.5V,1.5V,1V	1.8	0
Conf2	5V	1.2V,1.8V,2V	1V	1
Conf3	5V	1.4V,2V,1.6V	1v	0

On-chip SC DC-DC Converter is designed with Single input with nine variable outputs simultaneously three outputs is designed and tabulated the configuration in Table 3. The simulated output waveform is acquired with three different configurations with 5V as input.

In Table 2 5v is input with nine variable output voltages with two threshold voltages and switch conditions for three different configurations for single input multiple output Converter. According to table three different simulation waveforms given below

In configuration1:5V is converted into 2.5V,1.5V,1V using threshold value 1.8V with switch(S3) condition is off shown in Fig. 5.

In configuration2:5V is converted into 1.2V,1.8V,2V using threshold value 1V with switch(S3) condition is on shown in Fig. 6.

In configuration 2: 5V is converted into 1.4V,2V,1.6V using threshold value 1V with switch(S3) condition is off shown in Fig. 7.

Simulation waveform for three output DC-DC converter with three different configuration based on table 2 The Power report for single input multiple output DC-DC Converter shown in Fig 8.

CONCLUSION

An On chip DC-DC Converter with single input three variable outputs is designed and verified, The demerit in this is that it fails to give simultaneous output. Hence the number of pins used for power supply remains the same. In order to overcome this a method with nine variable outputs is designed and verified. The main merit in this is that it effectively reduces the number of pins used as it manages to give 3 outputs simultaneously. Further enhancement is carried out through reduced ripple using clocking method along with a process where the power is effectively utilized by reducing the wastage providing the amount of power to the core as per the need. while it is in process using clock gating.

REFERENCES

1. Ruzica Jevti and Hanh-Phuc Le, 2014. Per-Core DVFS With Switched-Capacitor Converters for Energy Efficiency in Manycore Processors, [2014] IEEE Transactions On Very Large Scale Integration (VLSI) Systems.
2. Burd, T.D., T.A. Pering, A.J. Stratakos and R.W. Brodersen, 2000. A dynamic voltage scaled microprocessor system, IEEE Journal on Solid-State Circuits, 35(11): 1571-1580.
3. Roy, K., S. Mukhopadhyay and H. Mahmoodi-Meimand, 2003. Leakage current mechanisms and leakage reduction techniques in deep submicrometer CMOS circuits, Proc. IEEE, 91(2): 305-327.
4. Pingqiang Zhou, Dong Jiao, Chris H. Kim and Sachin S. Sapatnekar, 2011. Exploration of On-Chip Switched-Capacitor DC-DC Converter for Multicore Processors Using a Distributed Power Delivery Network, [2011] Custom Integrated Circuits Conference (CICC), IEEE.
5. Le, H.P., S.R. Sanders and E. Alon, 2011. Design techniques for fully integrated switched-capacitor DC-DC converters, IEEE Journal on Solid-State Circuits, 46(9): 2120-2131.
6. Jeon, Heungjun and Yong-Bin Kim, 2012. A fully integrated switched-capacitor DC-DC converter with dual output for low power application, Proceedings of the great lakes symposium on VLSI - GLSVLSI 12, 2012.
7. Anderson, T.M. and F. Krismer, 2013. A 4.6 W/mm2 Power Density 86% Efficiency On-Chip Switched Capacitor DC-DC Converter in 32 nm SOI CMOS, [2013] IEEE Transactions On Very Large Scale Integration (VLSI) Systems.
8. Magarshack, P., P. Flatresse and G. Cesana, 2013. UTBB FD-SOI:A process/design symbiosis for breakthrough energy- efficiency, in Proceedings, pp: 952-957.