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Role of Variable Amplitude Carriers on Single Phase Asymmetrical Multilevel Inverter

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Abstract: MLIs have gained popularity in high power applications due to their low switch voltage stress and modularity. Cascaded H-bridge converters are a promising breed of multilevel converters which generally require several independent DC sources. It is observed from the tables that equal amplitude carrier's gives less THD but unequal amplitude carrier's gives higher fundamental rms and peak voltages. The DC components are almost similar in both equal and unequal amplitude carriers.

Key words: Seven level · Asymmetrical · Binary · R-load · THD

INTRODUCTION

Recently, existence of a redundant switching state has been utilized to replace the independent voltage sources with capacitors except for the one with the highest voltage level. Multilevel inverter techniques are widely used in the power engineering community (for HVDC link, active filtering, static VAR compensators, medium voltage variable speed drives etc). Advantages of this multilevel approach include good power quality, good electromagnetic compatibility, low switching losses and high voltage capability. In this work series connected inverter cells are considered because of the following merits: (i) series structure allows a scalable, modularized circuit layout (ii) the least number of components are required considering there are no extra clamping diodes or voltage balancing capacitors, (iii) potential of electrical shock is reduced due to the separate DC sources and (iv) switching redundancy for inner voltage levels is possible because the load voltage is the sum of each bridge's output. The other attractive features of multilevel inverters are as follows: (i) they can generate output voltages with extremely low distortion and lower dv/dt (ii) they draw input current with very low distortion. In all the well known MLI topologies, the number of power devices required depends on the output voltage level needed.

However, increasing the number of power semiconductor switches also increases complexity of converter circuit and control and cost. To provide a large number of output levels without increasing the number of converters. Asymmetric Multi Level Inverters (AMLI) can be used. Chechnya *et al*. [1] aims to extend the knowledge about the performance of different clamped multilevel inverter through harmonic analysis. Gnana Prakash *et al*. [2] proposed a method which is well suited for a high power applications and it built with three DC sources and six Switches. Gupta *et al*. [3] and [4] developed the topology for multilevel inverters to attain maximum number of levels from given DC sources and a comprehensive review of a recently proposed multilevel inverter. JansiRani *et al* [5] presented the implementation of 81 level inverter using Trinary logic. Mohammed Yaichi *et al*. [6] implemented a mechanism of SVM control strategies applied to five level cascaded multi-level inverter. Sudhakar *et al*. [7] focussed on the design of nine level inverter topology for three phase induction motor drives. Yu Liu *et al*. [8] suggested that trinary hybrid 81-level multilevel inverter for motor drive with zero common-mode voltage. Cheol-soon Kwon *et al*. [9] presented cascaded H-bridge multilevel inverter using Trinary DC sources.

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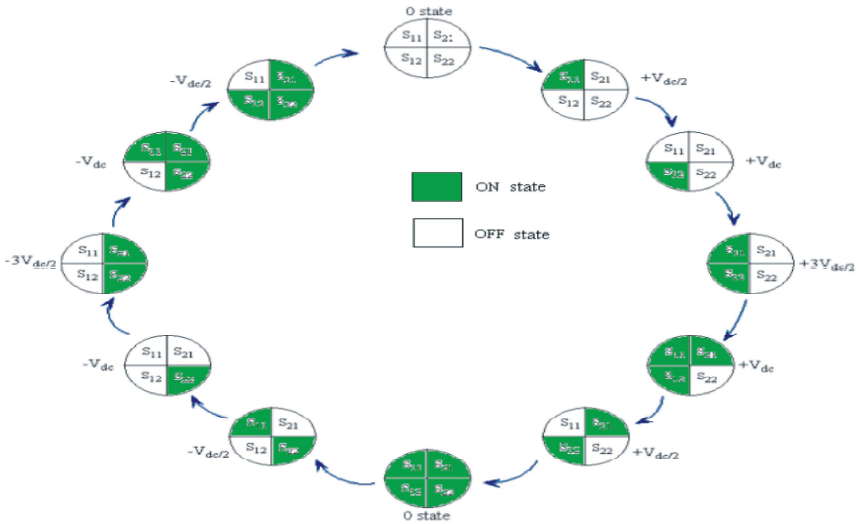

Fig. 1: Cyclic switching sequence of chosen AMLI

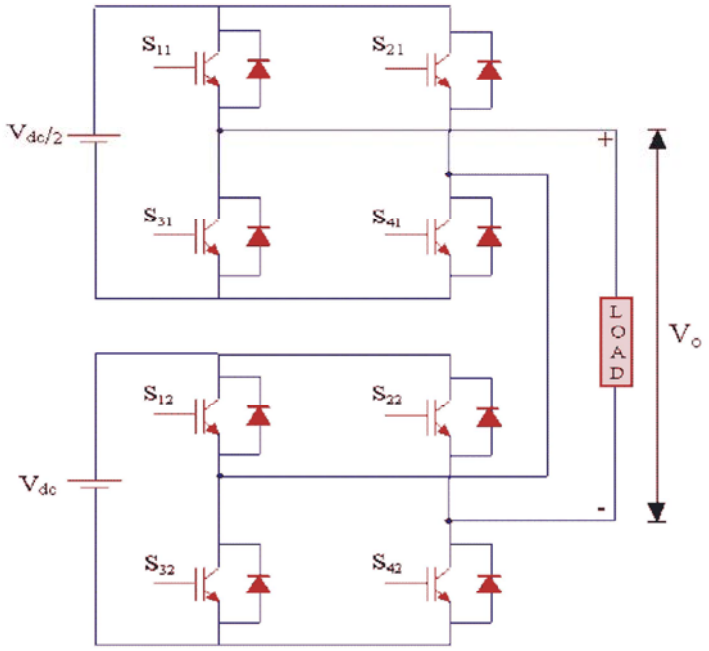

Fig. 2: Asymmetrical seven level inverter

Miranda *et al*. [10] evaluated the modulation techniques to multilevel trinary inverter applied to current active filters. Rahila *et al*. [11] developed a new 81 level inverter with reduced number of switches. Won-kyun Choi *et al*. [12] analysed the performance of cascaded H-bridge multilevel inverter. Employing bidirectional switches. This paper aims at comprehensively analysing the proposed single phase seven level binary source H-bridge cascaded inverter using various bipolar SPWM strategies. In this paper, the aforesaid topology was developed using MATLAB-SIMULINK.

Circuit Diagram: The chosen seven level cascaded multilevel inverter consists of two H-bridges. The first H-bridge consists of a separate DC source Vdc/2 whereas the second H-bridge consists of another DC source Vdc as depicted in Fig. 2. The number of modules (M) which is equal to the number of DC sources required depends on the total number of positive, negative and zero levels (m) of the AMLI. It is usually assumed that m is odd as this would give an integer valued M. Fig. 2 shows a typical seven level AMLI with two H-bridge inverters having unequal DC voltages and producing the following levels:-

Table 1: Switch states and output voltage levels of AMLI

S_{11}	S_{21}	S_{12}	S_{22}	Output (V_o)
1	0	1	0	$+3V_{dc}$
0	0	1	0	$+2V_{dc}$
1	1	1	0	$+2V_{dc}$
0	1	1	0	$+V_{dc}$
1	0	0	0	$+V_{dc}$
1	0	1	1	$+V_{dc}$
1	1	1	1	0
0	0	1	1	0
1	1	0	0	0
0	0	0	0	0
0	1	0	0	$-V_{dc}$
1	0	0	1	$-V_{dc}$
0	1	1	1	$-V_{dc}$
1	1	0	1	$-2V_{dc}$
0	0	0	1	$-2V_{dc}$
0	1	0	1	$-3V_{dc}$

$3/2V_{dc}$, $-V_{dc}$, $-1/2V_{dc}$, 0, $+1/2V_{dc}$, $+V_{dc}$ and $+3/2V_{dc}$. Table 1 lists the output voltages with the corresponding switching states of the upper power devices of the two modules of the chosen AMLI. As depicted from Table 1, sixteen legal configurations of device switching states and output voltage levels are available for a seven level AMLI. From the sixteen configurations available, only seven switching configurations are needed for the AMLI. Fig. 1 shows the cyclic switching sequence for the chosen AMLI. The following equations (1 and 2) give the relationship between M and m.

M=(m-3)/2 1
m=2(M+1)+1 2

The gate signals for chosen seven level AMLI are simulated using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index m_a (0.7-1) and for various PWM strategies. The advantages of the AMLIs are (i) reduced number of DC sources required to produce higher number of levels (ii) low switching loss and (iii) high conversion efficiency. This paper focuses on bipolar PWM strategies for chosen AMLI with triangular carrier and sine, THI and Trapezoidal references.

Modulation Strategies: Several modulation strategies have been proposed for symmetrical MLIs. They are generally derived from the classical modulation techniques used for more traditional inverters. Among all strategies, the most commonly used are the multi-carrier PWM with triangular carrier and sine, trapezoidal and THI references. These modulation strategies can be used to control asymmetrical multilevel inverters. The principle of the multi-carrier PWM is based on a comparison of sine/trapezoidal/THI references waveforms with vertically shifted carrier waveforms. To generate m levels, m-1 carriers are needed and the carriers are in continuous bands around the reference zero [13, 14].

They have the same peak to peak amplitude A_c and the same frequency f_c. The reference wave has a frequency f_m and amplitude A_m. At each instant, the result of the comparison is decoded in order to generate the correct switching function corresponding to a given output voltage level. Multi-carrier PWM strategies can also be categorized into bipolar and unipolar types. This chapter uses the former. In this chapter CD strategies, VFPWM and COPWM strategies are employed to get seven level output voltage from AMLI. Fig. 3 depicts the sample gating pulse generated for PDPWM strategy using MATLAB-SIMULINK block set. The following sections present the carrier disposition (PDPWM, PODPWM and APODPWM) strategies and also VFPWM strategies. The sine, trapezoidal and THI references are taken up for study.

For an m level inverter using bipolar multi-carrier technique, (m-1) carriers with the same frequency f_c and same peak-to-peak amplitude A_c are used. The reference waveform has amplitude A_m and frequency f_m and it is centered in the middle of the carrier signals. The frequency ratio m_f is defined in the bipolar PWM strategy as in eqn.3.

$m_f = f_c / f_m$ 3

In this proposed topology two methods are used.

- Equal Amplitude Carriers
- Un Equal Amplitude Carriers (or) Variable Amplitude Carriers (VAC)

Equal Amplitude Carriers: In this method, all the triangular carriers used will have the same amplitude. The PWM methods used are PDPWM, PODPWM and APODPWM with sine, THI and trapezoidal references. Fig. 4, 6 and 7 shows the sample carrier arrangement, output voltage and FFT plot for EAPDPWM strategy with THI reference (m_a = 0.8 and m_f=20). Where m_a and m_f are the amplitude and frequency modulation index.

Un Equal Amplitude Carriers (or) Variable Amplitude Carriers (VAC): In this method, all the triangular carriers used will not have the same amplitude. The PWM methods used are UEAPD (Un Equal Amplitude Phase Disposition) PWM, UEAPODPWM, UEAAPODPWM

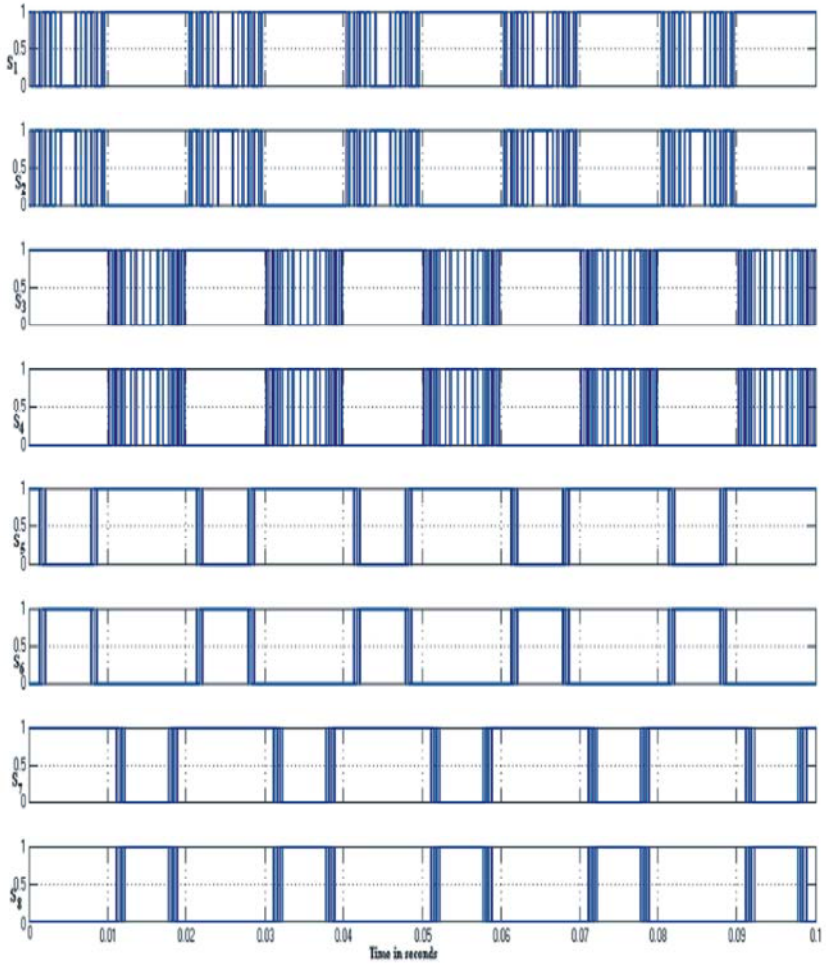

Fig. 3: Sample gating pulse for PDPWM generated using MATLAB

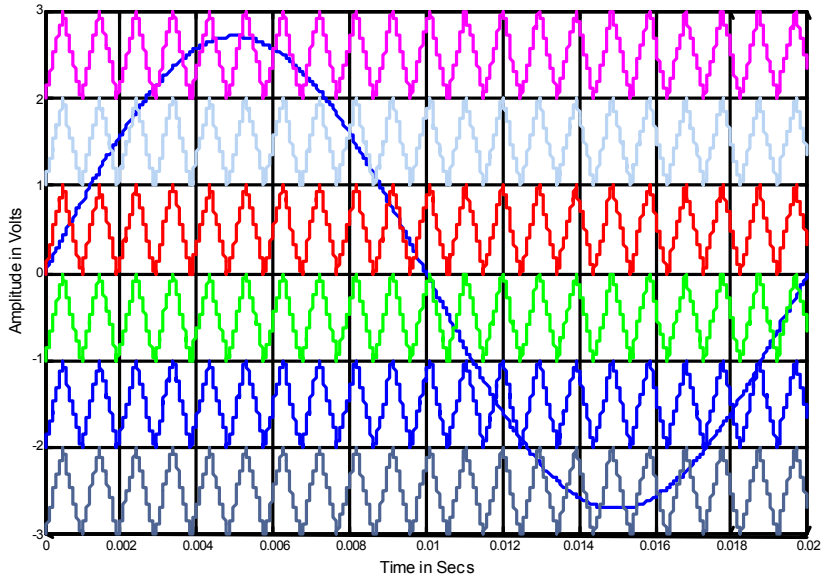

Fig. 4: Sample carrier arrangement for EAPDPWM strategy

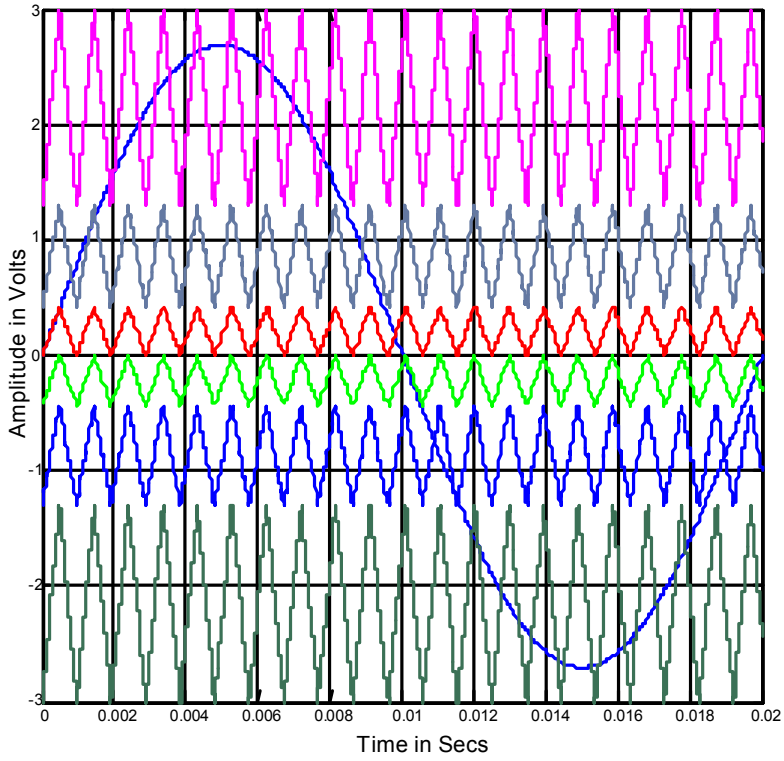

Fig. 5: Sample carrier arrangement for UEAPDPWM strategy

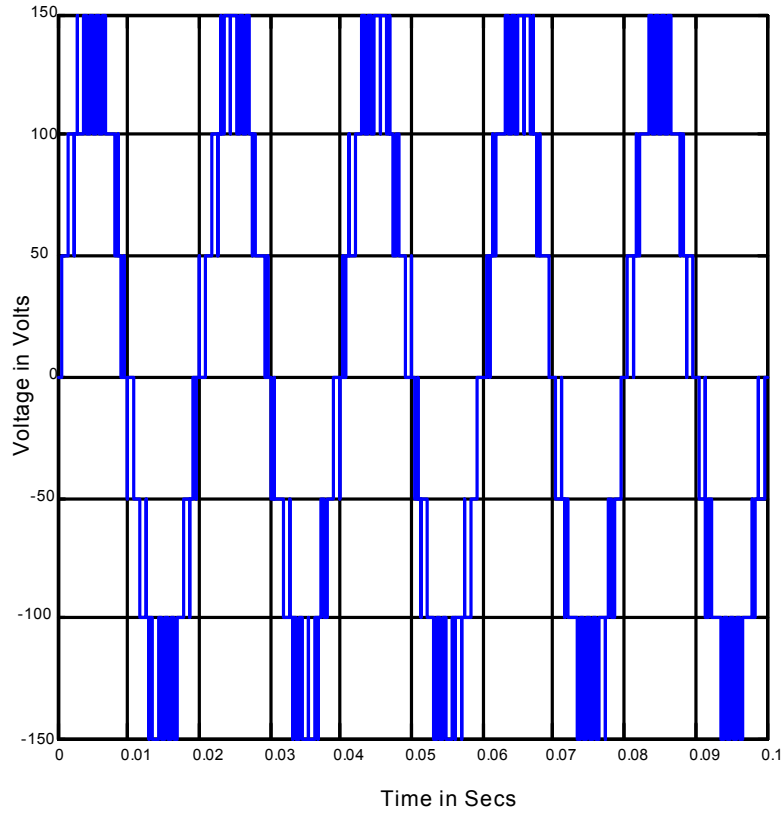

Fig. 6: Sample output voltage for EAPDPWM startegy

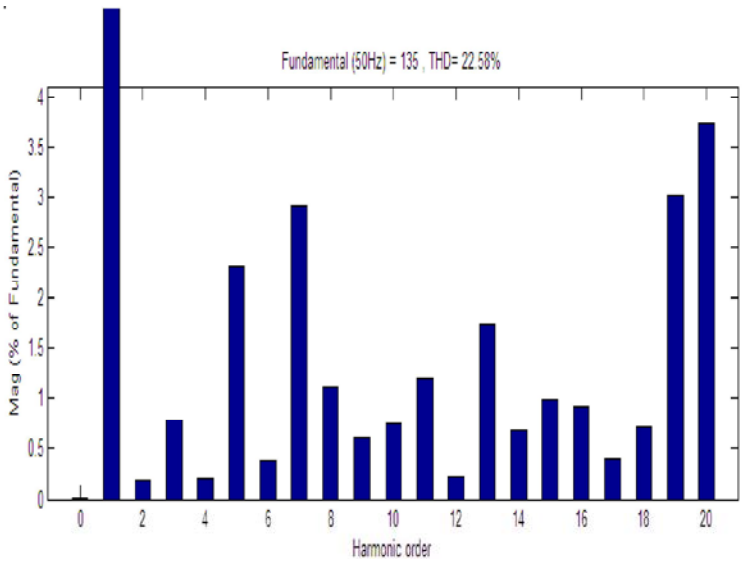

Fig. 7: Sample FFT plot for EAPDPWM startegy

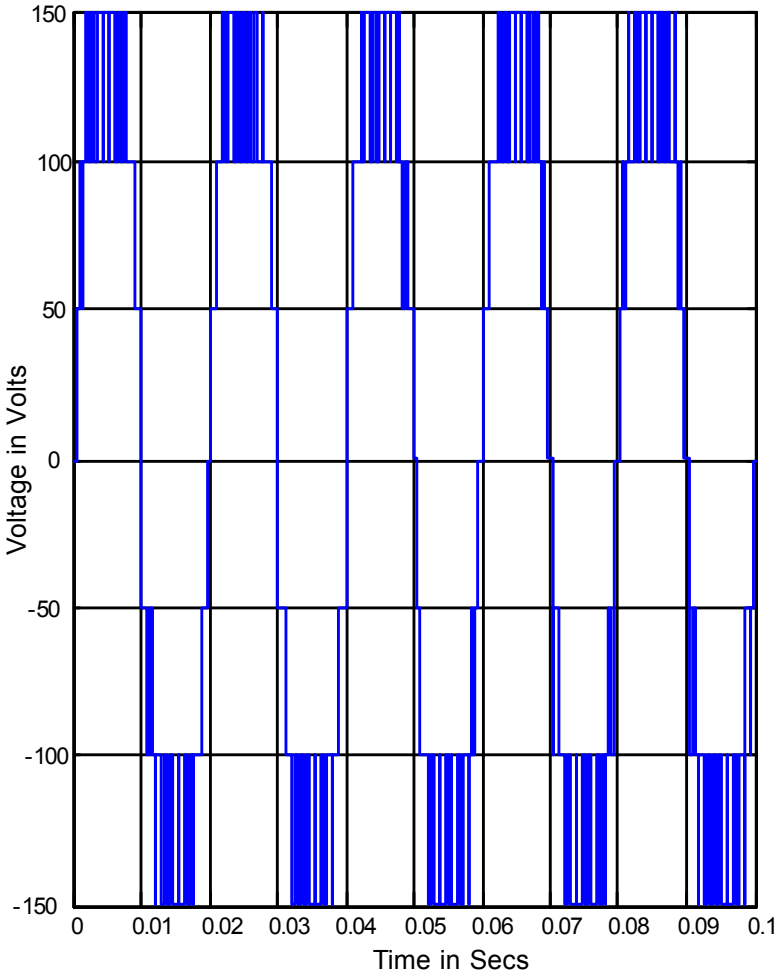

Fig. 8: Sample output voltage for UEAPDPWM startegy

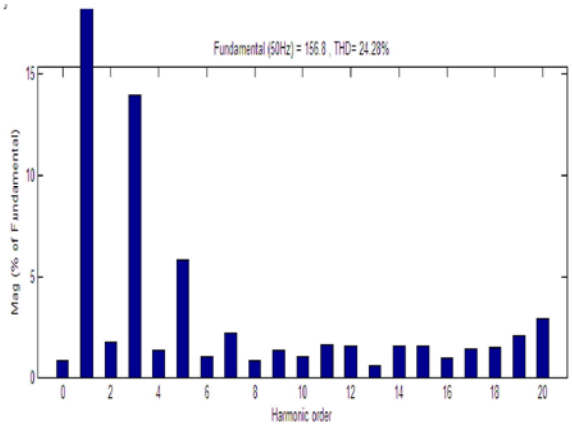

Fig. 9: Sample FFT plot for UEAPDPWM startegy

Table 2: THD for seven level output voltage based on equal amplitude and unequal amplitude carriers with various modulation indices

		% THD for 7-level inverter							
		PDPWM		PODPWM		APODPWM		VFPWM	
Ref.	ma	PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	VF	UEAVF
Sine reference	1	18.24	21.8	17.99	21.71	18.42	22.1	17.68	17.68
	0.9	22.58	24.28	22.51	23.5	23.03	23.64	22.23	22.23
	0.8	24.15	25.95	24.24	25.08	24.24	24.81	24.25	24.25
	0.7	25.34	26.43	25.41	25.79	25.12	25.36	25.49	25.49
	0.6	5-Level	25.68	5-Level	24.99	5-Level	24.81	5-Level	33.49
	0.5		24.77		24.12		24.02		40.22
	0.4		5-Level		5-Level		5-Level		5-Level
	0.3	3-Level		3-Level		3-Level		3-Level	
	0.2								
	0.1		3-Level		3-Level		3-Level		3-Level
	>0								
THI reference	1	24.91	30.86	25.48	29.99	25.23	29.95	24.6	30.46
	0.9	29.25	32.75	29.25	32.13	29.27	32.82	28.96	32.37
	0.8	31.16	33.4	29.66	33.62	30.27	34.41	31.04	32.99
	0.7	28.12	33.8	27.29	34.38	27.73	34.97	28.08	33.3
	0.6	5-Level	33.47	5-Level	33.67	5-Level	34.09	5-Level	32.79
	0.5		31.42		30.42		30.34		31.05
	0.4		5-Level		5-Level		5-Level		5-Level
	0.3	3-Level		3-Level		3-Level		3-Level	
	0.2								
	0.1		3-Level		3-Level		3-Level		3-Level
	>0								
Trapezoidal reference	1	19.01	25.71	18.88	25.48	18.87	26.31	18.66	25.32
	0.9	25.85	27.89	24.43	28.25	25.1	29.07	25.76	27.48
	0.8	27.86	29.74	26.49	30.23	27.18	30.78	29.83	29.27
	0.7	25.21	31.31	25.02	31.44	27.18	31.79	24.86	30.72
	0.6	5-Level	31.52	5-Level	30.65	5-Level	30.71	5-Level	31.22
	0.5		29.59		28.63		28.23		29.31
	0.4		5-Level		5-Level		5-Level		5-Level
	0.3	3-Level		3-Level		3-Level		3-Level	
	0.2								
	0.1		3-Level		3-Level		3-Level		3-Level
	>0								

Table 3: Vrms for seven level output voltage based on equal amplitude and unequal amplitude carriers with various modulation indices

		% THD for 7-level inverter							
		PDPWM		PODPWM		APODPWM		VFPWM	
Ref.	ma	PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	VF	UEAVF
Sine reference	1	105.7	117.2	106.1	116.9	106	116.9	105.9	105.9
	0.9	95.43	110.8	95.43	110.5	95.39	110.3	95.61	95.61
	0.8	84.65	104.2	84.97	103.9	84.87	103.8	84.65	84.65
	0.7	74.22	96.93	74.2	97.05	74.22	97.08	74.21	74.21
	0.6	5-Level	90.15	5-Level	89.95	5-Level	89.83	5-Level	63.56
	0.5		81.74		81.98		82.04		52.97
	0.4		5-Level		5-Level		5-Level		5-Level
	0.3	3-Level		3-Level		3-Level		3-Level	
	0.2								
	0.1		3-Level		3-Level		3-Level		3-Level
	>0								
THI reference	1	122.7	127.8	123	127.5	122.6	127.5	122.8	127.8
	0.9	110.6	120.2	110.5	120.2	110.3	120.4	110.7	120.2
	0.8	98.59	112.6	98.05	112.9	98.1	113.1	98.6	112.5
	0.7	86.27	105.2	86.01	105.4	85.9	105.6	86.27	105.1
	0.6	5-Level	98.19	5-Level	98.23	5-Level	98.18	5-Level	98.02
	0.5		90.71		90.43		90.25		90.69
	0.4		5-Level		5-Level		5-Level		5-Level
	0.3	3-Level		3-Level		3-Level		3-Level	
	0.2								
	0.1		3-Level		3-Level		3-Level		3-Level
	>0								
Trapezoidal reference	1	124.7	127.6	124.1	127.8	124.2	128	124.8	127.5
	0.9	112.4	120.5	111.4	120.7	111.7	121	112.3	120.4
	0.8	99.57	113.5	99.63	113.5	99.54	113.7	99.55	113.3
	0.7	86.26	105.6	87.05	105.7	86.78	105.7	86.42	105.7
	0.6	5-Level	98.67	5-Level	98.33	5-Level	98.08	5-Level	98.65
	0.5		90.02		90		89.99		90.07
	0.4		5-Level		5-Level		5-Level		5-Level
	0.3	3-Level		3-Level		3-Level		3-Level	
	0.2								
	0.1		3-Level		3-Level		3-Level		3-Level
	>0								

Table 4: Vpeak for seven level output voltage based on equal amplitude and unequal amplitude carriers with various modulation indices

		% THD for 7-level inverter							
		PDPWM		PODPWM		APODPWM		VFPWM	
Ref.	ma	PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	VF	UEAVF
Sine reference	1	149.5	165.8	150.1	165.4	149.9	165.3	149.8	149.8
	0.9	135	156.8	135	156.3	134.9	156	135.2	135.2
	0.8	119.7	147.4	120.2	146.9	120	146.7	119.7	119.7
	0.7	105	137.1	104.9	137.3	105	137.3	105	105
	0.6	5-Level	127.5	5-Level	127.2	5-Level	127	5-Level	89.89
	0.5		115.6		115.9		116		74.91
	0.4		5-Level		5-Level		5-Level		5-Level
	0.3	3-Level		3-Level		3-Level		3-Level	
	0.2								
	0.1		3-Level		3-Level		3-Level		3-Level
	>0								

Table 4: Continued

		% THD for 7-level inverter							
		PDPWM		PODPWM		APODPWM		VFPWM	
Ref.	ma	PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	VF	UEAVF
THI reference	1	173.5	180.8	174	180.3	173.4	180.4	173.6	180.8
	0.9	156.4	170	156.3	169.9	156	170.3	156.5	170
	0.8	139.4	159.3	138.7	159.7	138.7	160	139.4	159.2
	0.7	122	148.8	121.6	149.1	121.5	149.3	122	148.6
	0.6	5-Level	138.9	5-Level	138.9	5-Level	138.8	5-Level	138.6
	0.5		128.3		127.9		127.6		128.3
	0.4		5-Level		5-Level		5-Level		5-Level
	0.3	3-Level		3-Level		3-Level		3-Level	
	0.2								
	0.1		3-Level		3-Level		3-Level		3-Level
	>0								
Trapezoidal reference	1	176.4	180.14	175.5	180.8	175.6	181.1	176.6	181.1
	0.9	158.9	170.4	157.6	170.7	158	171.1	158.9	171.1
	0.8	140.8	160.5	140.9	160.5	140.8	160.7	140.8	160.7
	0.7	122	149.7	123.1	149.5	122.7	149.4	122.2	149.4
	0.6	5-Level	139.5	5-Level	139.1	5-Level	138.7	5-Level	138.7
	0.5		127.3		127.3		127.3		127.3
	0.4		5-Level		5-Level		5-Level		5-Level
	0.3	3-Level		3-Level		3-Level		3-Level	
	0.2								
	0.1		3-Level		3-Level		3-Level		3-Level
	>0								

Table 5: DC components for seven level output voltage based on equal amplitude and unequal amplitude carriers with various modulation indices

		% THD for 7-level inverter							
		PDPWM		PODPWM		APODPWM		VFPWM	
Ref.	ma	PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	VF	UEAVF
Sine reference	1	0.08	0.02	0.43	0.65	0.02	0.76	0.07	0.07
	0.9	0	0.89	0.24	0.18	0.09	0.29	0.06	0.06
	0.8	0.06	0.85	0.29	0.15	0.02	0.32	0	0
	0.7	0.1	0.46	0	0.05	0.07	0.02	0.07	0.07
	0.6	5-Level	0.41	5-Level	0.08	5-Level	0.28	5-Level	0.19
	0.5		0.02		0.22		0.26		0.2
	0.4		5-Level		5-Level		5-Level		5-Level
	0.3	3-Level		3-Level		3-Level		3-Level	
	0.2								
	0.1		3-Level		3-Level		3-Level		3-Level
	>0								
THI reference	1	0.19	0.06	0.1	0.62	0.17	0.61	0.24	0.39
	0.9	0.35	0.5	0.14	1.12	0.24	0.48	0	0.12
	0.8	0.56	0.38	0.59	1.24	0.25	0.02	0.32	0
	0.7	0.12	0.17	0.25	0.94	0.27	0.02	0.29	0.13
	0.6	5-Level	0.02	5-Level	0.76	5-Level	0.5	5-Level	0.18
	0.5		1.13		0.33		0.27		0.33
	0.4		5-Level		5-Level		5-Level		5-Level
	0.3	3-Level		3-Level		3-Level		3-Level	
	0.2								
	0.1		3-Level		3-Level		3-Level		3-Level
	>0								

Table 5:Continued

		% THD for 7-level inverter							
		PDPWM		PODPWM		APODPWM		VFPWM	
Ref.	ma	PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	VF	UEAVF
Trapezoidal reference	1	0.34	0.43	0.48	1.02	0.2	0.14	0.08	0.06
	0.9	0.58	0.31	0.67	1.08	0.05	0.09	0.39	0.04
	0.8	0.14	0.09	0.05	0.89	0.05	0.08	0.2	0.17
	0.7	0.2	0.05	0.71	0.8	0.05	0.54	0.14	0.22
	0.6	5-Level	1.06	5-Level	0.22	5-Level	0.31	5-Level	0.36
	0.5		0.67		0.02		0.12		0.08
	0.4		5-Level		5-Level		5-Level		5-Level
	0.3	3-Level		3-Level		3-Level		3-Level	
	0.2								
	0.1		3-Level		3-Level		3-Level		3-Level
	>0								

and UEAVFPWM with sine, THI, trapezoidal and THI references. Fig. 5, 8 and 9 shows the sample carrier arrangement, output voltage and FFT plot for UEAPDPWM strategy with sine reference (m_a = 0.8 and m_f=20). m_a is varied from 1 to 0.7 for equal amplitude carrier methods. In UEAC method if m_a is varied from 1 to 0.5 then the inverter will work as a seven level inverter.

Simulation Results: The following parameters are used for the simulation V_{dc1} = 50V, V_{dc2} = 100, R (Resistance) = 100 ohms, A_m (Amplitude of the modulating signal = 2, f_c (frequency of the carrier signal) = 1000 Hz and 2000Hz and f_m (frequency of the modulating signal) = 50 Hz. Table 2, 3, 4 and 5 shows the THD, $V_{RMS,}$ V_{peak} and DC components values for the proposed seven level inverter.

CONCLUSION

Various bipolar PWM strategies with equal amplitude carriers and unequal amplitude carriers have been developed using MATLAB-SIMULINK and tested for different modulation indices ranging from 0.8-1 for equal amplitude carriers and 0.6-1 for unequal amplitude carriers for the chosen single phase cascaded ternary multilevel inverter. It is observed from Table 4 that all PWM method provides output with relative low distortion for equal amplitude carriers. If equal voltage sources are chosen then the THD will be less in the case of unequal amplitude carriers. But for the unequal voltage sources the THD is more in the case of unequal amplitude carriers. It is observed from simulation results that (Table-5) almost in all the strategies unequal amplitude carriers gives more fundamental RMS values compared to equal amplitude carriers. It is seen from table 6 that peak voltage is more in the case of unequal amplitude carriers compared to equal amplitude carriers. It is observed from the Table 7 that dc components are less in both equal and unequal amplitude carriers.

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