Middle-East Journal of Scientific Research 23 (9): 2246-2250, 2015
ISSN 1990-9233

DOI: 10.5829/idosi.mejsr.2015.23.09.22543

# A New Low Power Bit-Interchanging TPG (BI -TPG) for Test per Scan BIST

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**Abstract:** A new test pattern generator to reduce the number of transition at scan input during scan shifting is proposed. The method is based on generating more correlative neighboring bits by interchanging adjacent bits in a test pattern. The proposed work is known as Bit Interchanging Teat Pattern Generator (BI-TPG) and it consists of basic XOR, XNOR, AND gates, 2:1 Multiplexer and a register. The length of the register is equal to the length of the scan cells. It reduces the shifting power at the scan cell. Experimental results on ISCAS'89 bench marks show minimum of 40% reduction in switching activity during test applications.

**Key words:** BI-TPG · Low power test per scan · Switching activity reduction

## INTRODUCTION

Sequential circuit testing is a complex problem because of the following reasons: we need to know the initial states. For n states there are $2^n$ states and they occur in a different order. There are numerous possible sequences. The test sequence should be long enough to propagate the error at the output. Automatic test pattern generator (ATPG) used in BIST generates patterns with very low correlation since a test pattern is generated for a given target fault without any consideration of the previous test pattern in the test sequence. Scan design for testability (DFT) technique destroys the correlation that typically exists between successive states of the sequential circuit by allowing the application of any desired values to the state latches. Improving correlation between test bits (or reducing horizontal switching transition in test bits) will reduce power dissipation at scan cells.

In full scan method all flip flops are replaced by scan flip flops. These scan flip flops are connected in to scan chain through which test patterns are allowed for scan in and scan out operation during testing. A scan cycle is the period in which a test pattern is shifted into (or test responses are shifted out of) the scan chains. The length of a scan cycle (the number of clock cycles) is equal to the number of scan flip-flops in the longest scan chain. A capture cycle is the period between two adjacent scan cycles. The circuit is set to the normal mode during the period when the test pattern is applied to the circuit and the test responses are captured in the scan flip-flops. Switching transitions at scan chain input is propagating through internal circuit lines. Therefore reducing transitions at the scan input will reduces transition in the entire circuit.

The layout of the paper is as follows. In section 2, the review of related works is discussed. Section 3 explains the design of proposed method and performance of proposed design with some example patterns. These patterns clearly show how the horizontal switching transition (HST) reduction performed by the proposed design. Experimental results and conclusions are presented in sections 4 and 5 respectively.

**Review of Related Work:** Shifting power dissipation is the major contributor to the total power dissipation in scan sequential circuits where the Horizontal Switching Transition (HST) in a test pattern is shifted through every flip flop in the scan cell. Reducing transitions between the adjacent bits in TP can reduce power dissipation. The full scan incurs area overhead, reduced circuit performance and considerable increase of test application time. If the scan chain is too long, multiple chain [1] or partial chain can be used. Scan chain partitioning [2] reduces test time than full scan method. The techniques based on genetic algorithms achieves considerable savings in power dissipation, however cannot be applied to scan sequential circuits. The proposed DFT architecture [1] is based on

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partitioning scan latches into multiple scan chains which reduces the clock tree power dissipation and does not have performance penalty but with a low test data overhead. Peak power reduction can also achieve from multiple scan chains technique with many scan enable inputs to activate one scan chain at a time [16]. The design proposed in [4] mainly to detect all single stuck-at faults in combinational circuits. Scan based BIST [5], swaps the adjacent bits if the $n^{th}$ bit of the present test pattern is logic '1' and it reduces peak and average power. Scan chain is partitioned into multiple segments [6], to improve the test effectiveness of scan-based BIST. The algorithmic technique for diagnosis of faulty scan chains [7] handles both stuck-at and timing failures (transition faults and hold-time faults).

The dynamic scan chain partitioning approach [2, 10] reduces peak shift power by using reconfigurable partitioning hardware. Scan chain partitioning scheme has been presented in [8] to improve the test effectiveness of scan-based BIST. This method inserts capture cycles inside the shift cycles compared with the test scheme using long scan chains but with more test application time. Software and hardware based scan chain diagnosis methods are analyzed and compared in [5]. The initialization method [10] is capable of generating tests for any type of asynchronous circuit where hazards/races may occur while changing from one input vector to the next. Sequential circuit design based on conservative logic gates [11] outperform the sequential circuits implemented in classical gates in terms of testability which using only two vectors. But it cannot detect multiple stuck-at-faults as well as multiple missing/additional cell defects. A new approach given in [12] to test generation for synchronous sequential circuits based on ordering of a fixed precomputed set of test vectors. An automated method [13] to partition a circuit for power-constrained broad side at-speed tests by a new partitioning algorithm with partial scan support. A new technique that diagnose single as well as multiple faults in scan chains has been proposed in [14]. Fast and precise algorithm [15] to diagnose multiple timing faults in the scan chain. But this technique diagnoses only the faults which are consistent and permanent. The scheme needs much less ROM to store the deterministic seeds on-chip is scan-based built-in self-test (BIST) technique [3], which based on weighted scan-enable signals. Many faults escape highly correlated patterns produced by BIST TPG [16] even they have low power dissipation.

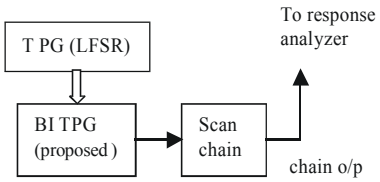

Fig. 1: Proposed method for scan cell testing

**Proposed Scan Cell Testing Method:** The low power testing of scan-based BIST can be achieved by using the proposed TPG (Figure 1) between LFSR and scan cells. BI TPG reduces the number transition in a test pattern by interchanging adjacent bits before at scan input.

**Using BI-TPG as Scan Cell BIST:** The proposed TPG modifies the test pattern in to low horizontal transition test pattern for scan cell testing. LFSR is used here as BIST-TPG. The patterns generated from LFSR are random in nature. Each test pattern has less correlative test bits. Each transition in the TP is shifted throughout the scan chain until it is scanned out. Therefore reducing transitions at scan inputs reduces much power dissipation.

The TPG used here is LFSR. The output of LFSR is applied to scan cells through proposed BI-TPG which reduces transitions at scan input. The scan output is sent to response analyzer.

**BI-TPG:** In scan cell testing the horizontal switching transition should be reduced which reduces power dissipation at scan input. Bit interchanging is done between two adjacent bits in a TP to reduce number of transitions. The main novelty of the proposed design is checking of a bit with its adjacent bit and the bit next to adjacent bit before interchanging and these conditions checking (before interchanging the bits) have not been reported in any previous works to the best of our knowledge. Before interchanging the adjacent bits, we should check the following conditions.

To interchange the bits $q_0$ and $q_1$ they should satisfy the following conditions.

Condition 1: $q_0 = = q_2$ (1)

Condition 2: $q_0 ! = q_1$ (2)

A bit is complement with its adjacent bit it will be interchanged if and only if, the bit and the bit next to the adjacent bit are same. For checking the above conditions

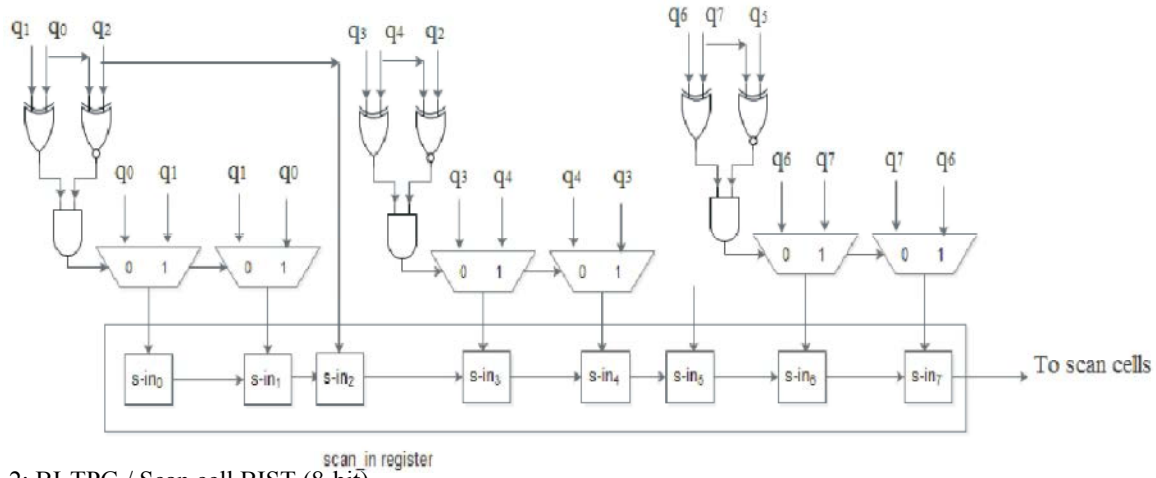


Fig. 2: BI-TPG / Scan cell BIST (8-bit)

Table 1: Comparison of low power scan cell TPs generated by different methods

| Generated TP | Number of HST | TP using bit swapping method [9] | Number of HST | Modified TP(proposed) | Number of HST |
|---|---|---|---|---|---|
| AB - 1010 1010 | 7 | 97-1001 0111 | 4 | 73 - 0111 0011 | 3 |
| 55 - 0101 0101 | 7 | 55 - 0101 0101 | 7 | 8E - 1000 1110 | 3 |
| B5 – 1011 0101 | 6 | BA-10111010 | 5 | 6E - 0110 1110 | 4 |
| 14 - 0001 0100 | 4 | 14 - 0001 0100 | 4 | 0C - 0000 1100 | 2 |
| 10 - 0001 0000 | 2 | 10 - 0001 0000 | 2 | 10 - 0001 0000 | 2 |
| E8 – 1110 1000 | 3 | D4 - 1101 0100 | 5 | E0 – 1110 0000 | 1 |
| Σ Transitions | 29 | | 27 | | 15 |

the basic XOR, XNOR gates are used. If two neighboring bits are different the XOR output is 1.A bit and the bit next to its adjacent bit are given to an XNOR gate. If both are same the output is 1. If both conditions are satisfied interchanging is performed.

The random TPG used here is LFSR and the polynomial used is $x^n+x+1$. The proposed scan cell BIST implementation is shown in Figure 2. The above conditions 1 and 2 are checked using XOR and XNOR gates respectively. If both conditions are satisfied, XOR and XNOR gates output is logic '1'. The outputs of both gates are applied to an AND gate. The AND gate output is logic '1' if both conditions are satisfied. This output is given as select line to the multiplexer which does interchanging the adjacent bits. The outputs of all multiplexers form a new test pattern for scan cells. The resulting test pattern has less horizontal bit transition than the generated test pattern.

The above 8 bit scan cell BIST can interchange only 6 bits. The second and fifth bits of TP are sent as it is. This 8 bit BIST needs six 2:1multiplexers, 3 XOR, 3 AND, 3 XNOR gates and an eight bit scan in register. This implementation can be expanded for large circuits. The same 8 bit arrangement can also be used for many scan cells but each scan cell (each group of scan cell) should be operated with different clock pulses.

**Test Patterns Modified by BI-TPG:** The second and fifth bits of the test pattern are not modified. They are only used for checking the adjacent transition. Using this method, we can reduce 42.8% of peak power and 50.54 % of average power.

Table 1 shows some sample test patterns generated using this method. The interchanged bits are indicated by boldness. The bits are first checked that they are having transition with its adjacent. Transition is reduced by interchanging two adjacent bits. This avoids the transfer of that transition during shifting. Each transition is transferred through the whole scan cell at each clock. Therefore each HST reduction reduces much shifting power. The bit swapping method [5] swapping the adjacent bits if the $n^{th}$ bit is logic '1' but without checking any conditions. Therefore even if a TP has more number of transitions but the $n^{th}$ bit is logic '0' then BS-LFSR does not work on that (Table 1 TP=55) .Some times BS LFSR swapping the adjacent bits unnecessary (Table 1 TP=E8).

The number transition increased than the random TPG output which increases power dissipation also. Many faults escape if random patterns highly correlated and can be detected by continuously complementing values. In BIST TPG [17] the scan cells are applied test vectors through an AND gate and toggle flip flop are highly correlated. But the proposed method generates patterns with reduced TPs which can detect more faults.

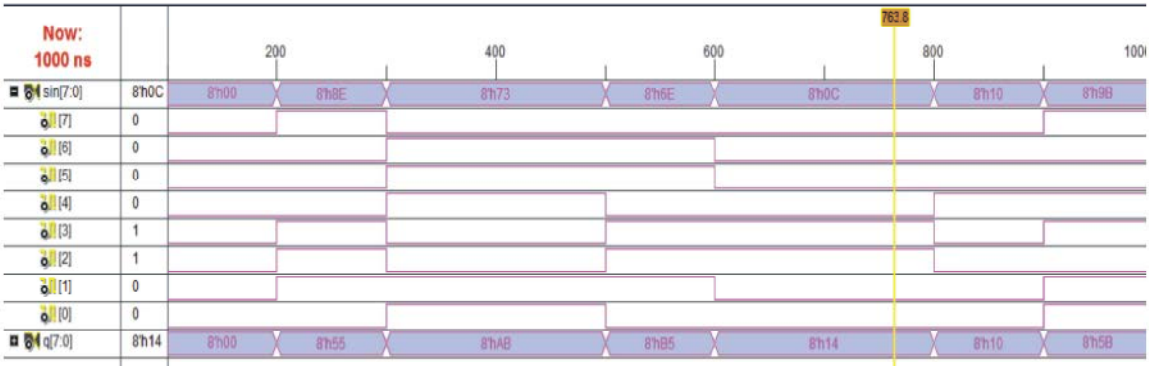


Fig. 3: Simulation output of BI TPG

Table 2: Comparison of peak Switching Transition ($ST_{pk}$) reduction

| Circuit | $ST_{pk}$ reduction % [16] | $ST_{pk}$ reduction BS LFSR% [9] | $ST_{pk}$ reduction % (proposed) |
|---|---|---|---|
| S5378 | 36.6 | 39 | 40.44 |
| S9234 | 38.9 | 45 | 48.66 |
| S13207 | 46.1 | 41 | 37.9 |
| S38417 | 40.1 | 39 | 38.34 |
| S38584 | 35.9 | 51 | 60.06 |
| Avg | 39.5 | 43 | 45.08 |

The proposed method checks the transitions using two conditions: i) the adjacent bits not same ii) The bit interchanging the adjacent bits must be same.

The proposed BI-TPG generates modified pattern for scan cell that has same number of 1s and 0s as the generated LFSR TP. Thus proposed BI-TPG retain the feature any random TPG.

## RESULTS AND DISCUSSION

The hardware requirement for the above scan cell BIST includes basic XOR, XNOR and gates with simple multiplexer. The modified TP is sent to scan cell through a register. The length of the register is equal to the number of test pattern.

The design (Figure 2) has been implemented using Xilinx software and verified. The results show that minimum 40% of HST is reduced.

If conditions 1 and 2 are satisfied, then the adjacent bits are interchanged otherwise the bits applied to scan cells as it is. The above implementation (8 bit scan cell) can be used in the circuits that have dynamic scan chain partitioning [2] which can reduce peak and average power dissipation also. The same method can be done for any number bits as the requirement.

In the simulation output, 'q' denotes the generated test pattern and sin is the modified pattern input for scan cells. From Table 1 it is proven that minimum 40 % transition is reduced and the pattern having very low transitions are not modified unnecessary.

Table 2 shows the comparison of experimental results on ISCAS bench marks of proposed method with some previous methods. It clears that the proposed TPG gives better results for most of the bench marks.

## CONCLUSION

Excessive switching transition in test pattern causes several problems. Reducing heat dissipation in test mode is also an important issue. This method produces test patterns that has more correlated neighboring bits and reduces number of transitions that occur at scan inputs during scan shifting. The proposed BI TPG generates test patterns as conventional random TPG but the order of TP bit is different. By interchanging the adjacent bits using proposed method decreases horizontal switching transitions in a test pattern with preserving its randomness feature. The overall transition of the CUT input is reduced by minimum of 40%.From Table 2 it is proved that the proposed method produces best results for most of the benchmarks. Here every time of interchanging the switching transition is checked between adjacent bits. This feature has not been reported in any previous works to the best of our knowledge. By this method of condition checking some unnecessary interchanging (that increases number of transitions) are avoided. The proposed method preserves the same number of 1s and 0s that retains random TPG and detects more faults.

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