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An Efficient Multiplier Design for Discrete Wavelet Transform (DWT) in Image Fusion

[1]S. Udhaya Suriya and [2]Dr. P. Rangarajan

[1]Department of Biomedical Engineering, Adhiyamaan College of Engineering, India
[2]Department of CSE, RMD College of Engineering and Technology, Kavarapett, India

Abstract: The immense level of application in Digital Image Processing made the Discrete Wavelet Transform (DWT) a powerful tool to analyse the images. Many works have been contributed towards the Discrete Wavelet Transform as the demand for low-power and high-speed discrete wavelet transforms computation increases. In this paper, high speed and low power Booth Encoded Wallace tree multiplier is proposed for Discrete Wavelet Transform (DWT). The proposed Discrete Wavelet Transform (DWT) is further analyzed by implementing in Image Fusion application. The proposed multiplier and image discrete wavelet transform is developed using Verilog HDL and targeted in the EP4CE115 FPGA device. The result of the proposed multiplier outperforms other multiplier such as, Wallace tree multiplier and Modified Wallace tree multiplier. In similar, the proposed Discrete Wavelet Transform (DWT) consumes 2965 logic elements and achieves a maximum frequency of 188 MHz at 498.43 (μW).

Key words: Discrete Wavelet Transform (DWT) · Image Fusion · Multiplier

INTRODUCTION

The multi-resolution signal analysis in frequency domain is made possible by Discrete Wavelet Transform (DWT) [1]. The powerful realization of discrete wavelet transform has successfully implemented in application ranges from signal analysis, image processing, numerical analysis, video coding, statistics and pattern recognition. In this work we have implemented the discrete wavelet transform in image fusion technique. The multiple sub bands of high frequency components and low frequency components of an image are obtained from the output of Discrete Wavelet Transform (DWT). The image fusion techniques, finds extensive research of interest in medical imaging, defence research, remote sensing and weather forecasting. The output of transformed image is added and fused image is obtained by taking the Inverse Discrete Wavelet Transform (IDWT). Most of the modern Digital Signal Processing (DSP) application and communication components depend on DWT and IDWT. The number of mathematical operations in discrete wavelet transforms consumes power and also hierarchical implementation of discrete wavelet transform made the complex architecture. In addition to the parallel and serial representation of data will increase the complexity of the architecture. Apart from these constraints, the major concern is the latency, throughput and storage.

Related Work: The well-known JPEG 2000 standard [2] uses Discrete Wavelet Transform (DWT) in the image encoding process. The VLSI architecture for discrete wavelet transform is implemented in single chip [3]. In [4], the Distributed Arithmetic (DA) is used to implement the multiplier-less architecture for Discrete Wavelet Transform (DWT). The complexity of adder structure in Discrete Wavelet Transform (DWT) is reduced in [5]. In [6-7], the efficient folded architecture for Discrete Wavelet Transform (DWT) is proposed. In [8], approximately 130 MHz throughput is achieved by the polyphase structure of Discrete Wavelet Transform (DWT) in JPEG 2000. The FPGA implementation of parallel distributed structure of discrete wavelet transform is proposed in [9]. The programmable Discrete Wavelet Transform (DWT) is exposed in [10].

The multiplier based on Horner's rule [11] is implemented in Discrete Wavelet Transform (DWT) for high speed and to reduce the delay, tree-height reduction technique is used. The loss and lossless compression

Corresponding Author: S. Udhaya Suriya, Department of Biomedical Engineering, Adhiyamaan College of Engineering, India.

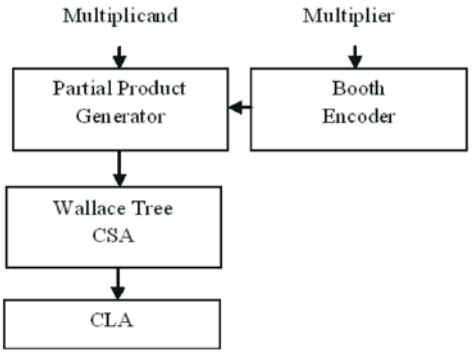

Fig. 1: Architecture of Proposed Multiplier

technique using (5, 3) and (9, 7) wavelet filter is shown in [12]. The reconfigurable architecture [12], developed is based on the (5, 3) wavelet filter, which will switch between 1D-DWT and 2D-DWT. The Discrete Wavelet Transform (DWT) based on lifting scheme [13] is proposed for lossless and loss compression. The discrete wavelet transform based on a convolution approach to reduce delay and complexity is proposed in [14]. The (4, 3) bi-orthogonal wavelet filter for discrete wavelet transform is shown in [15]. The implementation results in [16], concludes that (9, 7) wavelet filter shows better performances than (5, 3) and (4, 3) wavelet filter in Discrete Wavelet Transform (DWT). The proposed Booth encoded Wallace tree multiplier is implemented in the (9, 7) filter of discrete wavelet transform, further the Discrete Wavelet Transform (DWT) is evaluated by utilizing in image fusion.

Design of Proposed Multiplier: The Discrete Wavelet Transform (DWT) is famous transformation techniques which plays a vital role in almost entire image processing applications. The proposed multiplier is shown in Figure 1. The proposed multiplier consists of five important blocks such as, Booth encoder, Partial Product Generator (PPG), Wallace Tree Multiplier, Carry Save Adder (CSA) and Carry Look Ahead Adder (CLA).

The booth encoder will reduce the number of partial products, thereby, reducing the consumption of logic elements (area) and power. The delay in the addition of partial product in the Wallace Tree Multiplier is reduced by utilizing the performance of Carry Save Adder (CSA). Hence the idea emerged here by combining the booth encoder and Wallace Tree Multiplier to achieve low power and area with high speed.

Booth Encoder: The booth encoder will reduce the partial product based on the logic present in Table 1.

Table.1 Booth Encoder Table

MULTIPIER BITS			OUTPUT BITS			OPERATION ON MULTIPLICAND
Y_{i+1}	Y_i	Y_{i-1}	NEG	2	1	
0	0	0	0	0	0	0X
0	0	1	0	0	1	+1X
0	1	0	0	0	1	+1X
0	1	1	0	1	0	+2X
1	0	0	1	1	0	-2X
1	0	1	1	0	1	-1X
1	1	0	1	0	1	-1X
1	1	1	1	0	0	0X

The booth algorithm can be used to compute the product terms of both negative and positive numbers. The delay and area of the multiplier are reduced by using the Carry Save Adder (CSA) and Booth Encoder respectively.

Wallace Tree Multiplier: The Wallace Tree consists of Partial Product Generator (PPG) computed from previous steps. The Carry Save Adder (CSA) is utilized to implement the Wallace Tree operation to add the Partial Product Generator (PPG). The individual block of Carry Save Adder (CSA) consists of Full Adder (FA) connected with some carry-in and carry-out logic. This logic is used to add the Partial Product Generator (PPG) in each column of the multiplier. The addition of 8-bits by Ripple Carry Adder (RCA) consume seven full adders whereas, four full adders are enough in case of Carry Save Adder (CSA), thereby, saving the delay of three full adders.

Partial Product Generator: The partial product is generated by taking the output of Booth encoder. Four Booth encoders are necessary for a total of eight partial product's operation. The generated partial product is shown in Figure 2. In the diagram, each row represents one partial product, although all the partial products are not shown in the diagram, a total of eight partial products present in the diagram.

Carry Look-Ahead Adder: The Carry Look-Ahead Adder is developed to add two numbers with high speed. The logic behind Carry Look-Ahead Adder (CLA) is, the generation of carry is initiated if and only, the least significant bits propagate a carry. The 'P' and 'G', represent the carry-output and sum-output of half adder presents in Carry Look-ahead Adder. The 'P' and 'G' are generated with carry for every bit position.

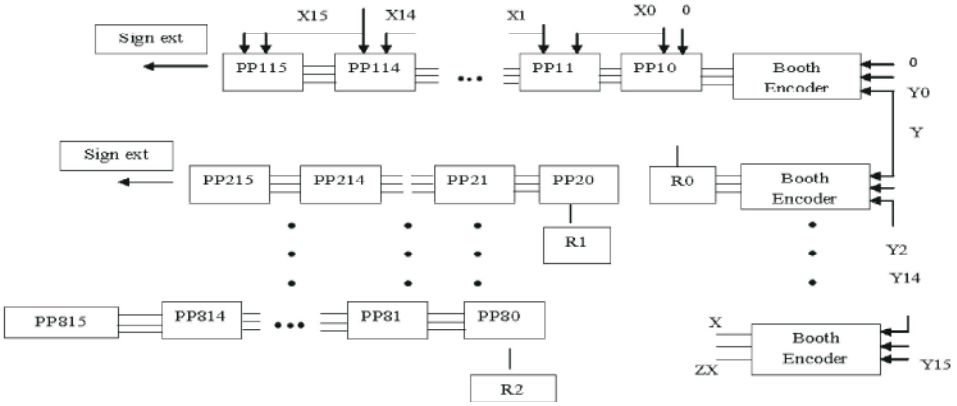

Fig. 2: Partial Product Generator

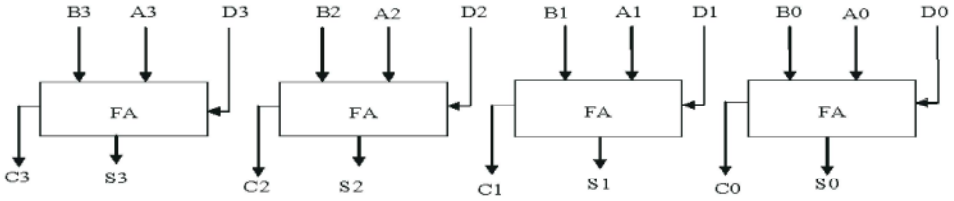

Fig. 3: Carry Save Adder

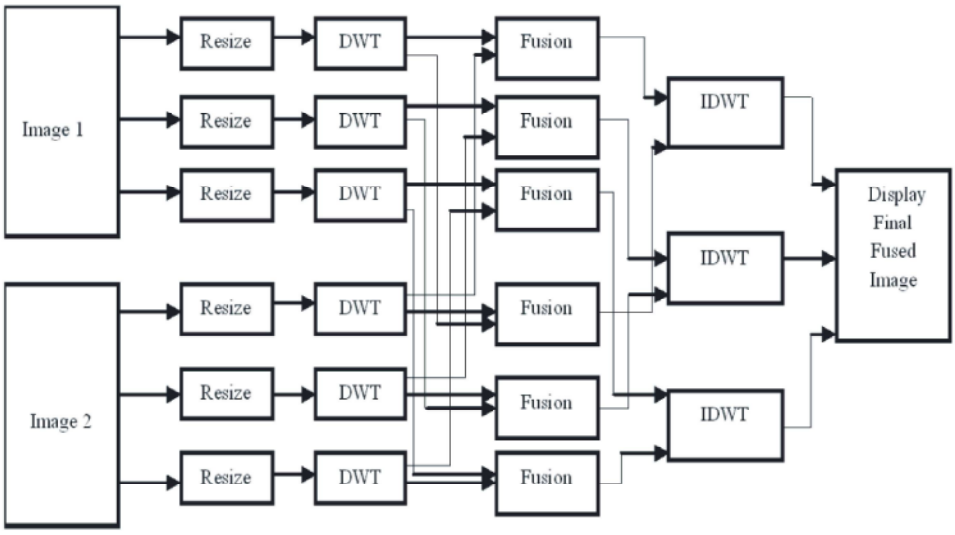

Fig. 4: Proposed DWT in Image Fusion

The computation time in Carry Look-Ahead Adder (CLA) is reduced by pre-generating the carry and sum of the particular input. Hence, this adder is used in the final stage of addition in Partial Product Generator (PPG).

Carry Save Adder: The arrangement of full adders in Carry Save Adder is shown in Figure 3. The initial arrangement of the carry save adder possesses a disconnected ripple carry adder. This misconnection will facilitate the designer to add an input to the adder; as a result three inputs can be given to a single adder.

The sum vector and carry vector is represented by 'M' and 'C' which is actual sum and carry of three input full adder without carry propagation. The redundant representation of the sum is realized in some case, since n-bit sum require a 2n-bit sum to represent them. The overall output of S and C vector is obtained from carry propagate adder.

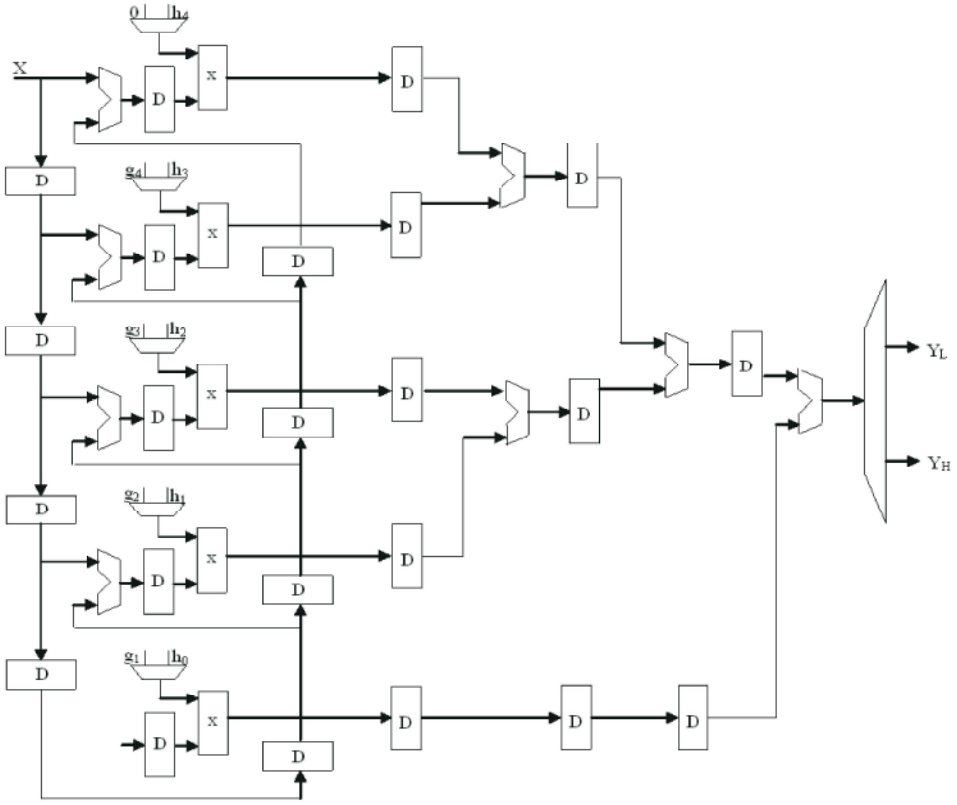

Fig. 5: (9,7) Filter used in Image Fusion

Implementation of Proposed DWT in Image Fusion: The fusion of two images from the set of image, where the resultant image contains more information than any other image in the set of image is called as image fusion. In other word, the combination of multispectral image (*i.e.*. coloured or blurred image) and panchromatic image (gray scale or high resolution) image is called as image fusion [17].

The image fusion based on the proposed Discrete Wavelet Transform (DWT) is implemented in both Matlab Simulink and Altera Quartus II.

The Matlab implementation of image fusion based on proposed Discrete Wavelet Transform (DWT) is shown in Figure 4. Initially the image is divided into their respective R,G,B block and each block is resized to 480 x 640. Then each output from the resize block is sent to proposed Discrete Wavelet Transform (DWT) block and the output of DWT block from Image-1 and Image-2 is given to fusion block.

The Inverse Discrete Wavelet Transform of the fusion block results in the fused image. The execution of Discrete Wavelet Transform on image is made possible by (9,7) wavelet filter shown in Figure 5.

RESULT EVALUATION

The proposed Booth Encoded Wallace Tree Multiplier and Discrete Wavelet Transform (DWT) were developed using Verilog HDL and targeted in Altera Cyclone EP4CE115 FPGA device. The proposed multiplier achieves a maximum frequency (Fmax) of 241 MHz at 97.92 µW.

In similar the proposed multiplier consumes 832 logic elements which are less comparing to 1741 and 1287 consumed by the Wallace Tree Multiplier and Modified Wallace Tree Multiplier. The result analysis shown in Table 2, concludes that the proposed multiplier outperforms the other multiplier.

Table 2: Device Utilization of Proposed Multiplier

Multiplier	Logic Elements	Power (µW)	Maximum frequency (Fmax) (MHz)
Wallace Tree Multiplier	1741	165.32	147
Modified Wallace Tree Multiplier	1287	116.49	179
Proposed Multiplier	832	97.92	241

Table 3: Device Utilization of Image Fusion Application

Analysis of Image Fusion based on Various Discrete Wavelet Transform			
Image Fusion based on	Logic Elements	Power (μW)	Maximum frequency (Fmax) (MHz)
DWT with Wallace Tree Multiplier	4186	788.71	117
DWT with Modified Wallace Tree Multiplier	3787	613.09	139
DWT with Proposed Multiplier	2965	498.43	188

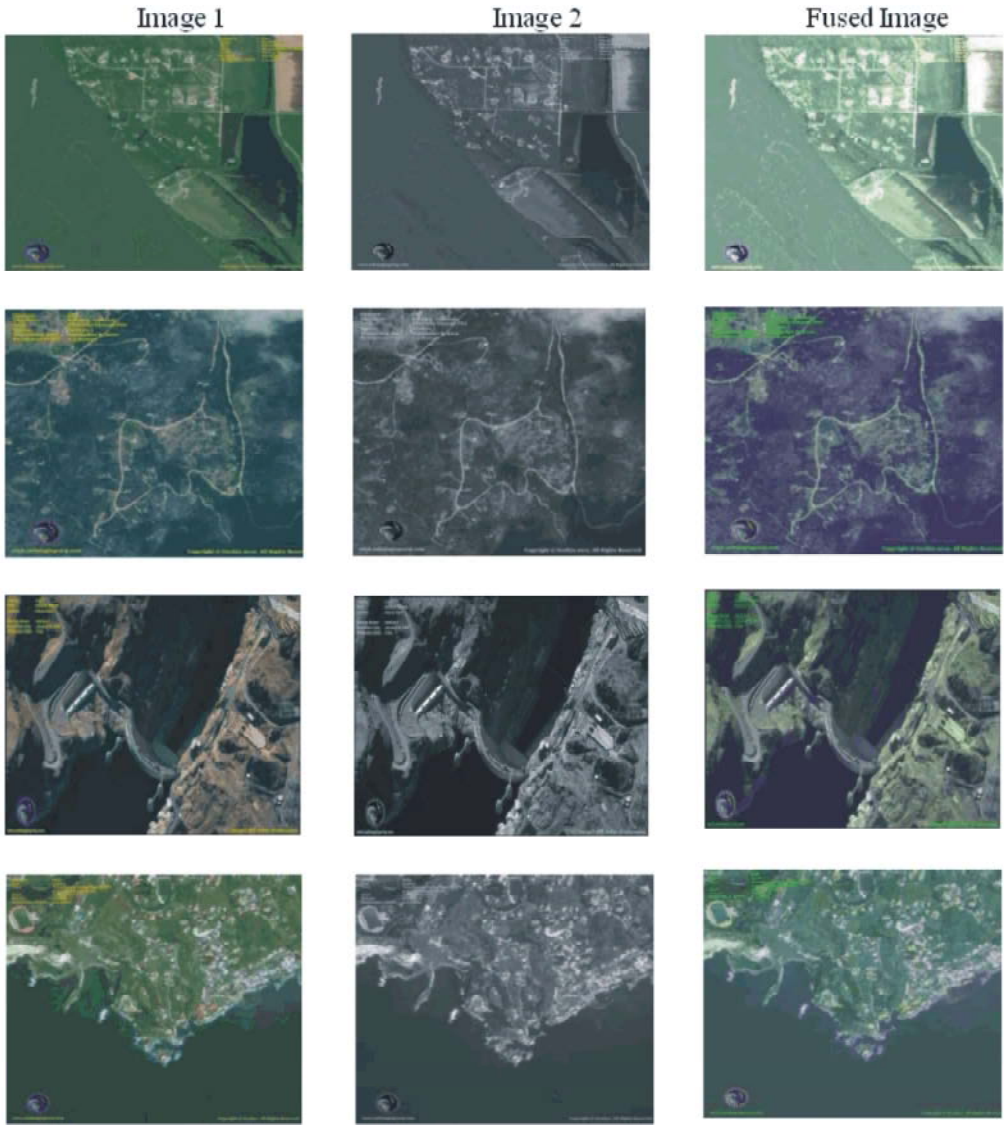

Fig. 6: Fused Image with Proposed DWT

The device utilization of image fusion application is shown in Table 3. The image fusion application based on the proposed Discrete Wavelet Transform (DWT) consumes 2965 which is low compared to other methods. In similar, the maximum frequency (Fmax) achieved is 188 MHz at 498.43 μW, which is remarkable compared to 117 MHz and 139 MHz by DWT with Wallace Tree Multiplier and DWT with Modified Wallace Tree Multiplier respectively. The result evaluation is extended by implementing the image fusion application in Matlab Simulink for fused image quality assessment. From the fused image shown in Figure 6, the quality of the image can be assessed and verified.

CONCLUSION

The efficient Discrete Wavelet Transform (DWT) with a high-speed multiplier is presented in this paper. The proposed multiplier and image fusion application is developed using Verilog HDL and targeted in Altera Cyclone EP4CE115 FPGA device. The proposed discrete wavelet transform is evaluated by implementing in Image Fusion application. The proposed multiplier shows a remarkable performance when compared to Wallace Tree Multiplier and Modified Wallace Tree Multiplier. The device utilization results of the discrete wavelet transform in image fusion is presented and the results of the proposed techniques outperform the other techniques. The quality of the fused image is assessed and found to be quality. As of now, the paper has contributed to the DWT architecture for image fusion, in future the architecture can be evaluated by extending to 2-Dimenesional (2D) and 3-Dimensional (3D).

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