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Analog VLSI Design Based Artificial Neural Network for Lung Sound Signal Processing

K. Sathesh, N.J.R. Muniraj, S. Sowndharya, A. Sathiya Priya, S. Sindhuja and T. Suganthi

Department of ECE, Tejaa Shakthi Institute of Technology for Women, Coimbatore, India, 641659

Abstract: Artificial Neural Network (ANN) is widely used technique in real world Lung sound signal processing and in this paper Artificial Neural Networks is implemented to obtain local minima using analog VLSI signal processing. The Artificial Neural Network response with precise results will be obtained by back propagation algorithm with feed forward neural network. The facets of ANN are artificial synapse, axons and dendrites circuits. The schematic of this proposed ten hidden layers of analog neural network architecture will be verified using Electric VLSI CAD tool in the 180 nm technology. DRC and NCC will be checked with Electric VLSI CAD tool. The simulation results will be obtained using LT Spice tool. The final design is verified using Electric CAD tool. The implementation of proposed architecture in 180 nm technology shows their advantages, in the context of power, speed and area.

Key words: NCC · ERC · Artificial Neural Network · ANN

INTRODUCTION

Artificial Neural Network is basically an electronic model that works based on human brain mechanism. With an advancement of emerging technologies in Electronics and in Information Processing Systems, the Artificial Neural Network model is evolved. The neural network was originally devised by Warren McCullough, a Neurophysiologist and an young mathematician Watterpitts. ANN have the proficiency to learn from the past values which was processed in each iteration and it works on unforeseen way of propagation through the connectionist networks. The processors of neural networks work as neurons. It is perceived that it has an intelligence to mimic human brain activity at least partially. VLSI neural networks are most commonly used connectionist model and searched as an approach to give real time solutions to number of specific problems in an areas of signal and image processing and also in other areas where it has a specific definitions of problems. The Artificial Neural Networks are derived from biological neural feat system. Biological neural network is composed of series of interconnected neurons. Neurons interact with their neighbors in an unforeseen way it consist of axons, connected through weights and dendrites to all other neurons. The progression between neurons about weights is very difficult chemical process. When the sum of two inputs signal is exceeding certain threshold voltage the neuron will send an activation potential, then the neuron will fire to work as a consequence[1]. The weights are stored, multiplied and are summed and it will produce the product of two input signals and the summation of an activation potential, which is the bias generated in the network[2,3]. The weights are stored in the network are called synapse. There are approximately they are huge billions of neurons inside our human brain and they all work through the weights are called synapse to solve problems [4]. Actually human brains consist of hundred billions of neurons on an average which is connected to 7000 synapses. Neural networks are basically a non-deterministic networks. It is slow about 1ms and it is a powerful machinery to react and they emit spikes when they receive the inputs through the synapses and dendrites connected to other neurons as shown in the Fig:1.

It gives rise to the mechanism that works on Artificial Intelligence. To be sanguine the future development of neural networks lies in the hardware development. At present artificial neural augmentation simply shows the superior works. This research, developing neural networks in analog VLSI domain is due to its prodigious parallelism[5].

Corresponding Author: K. Sathesh, Department of ECE, Tejaa Shakthi Institute of Technology for Women, Coimbatore, India, 641659.

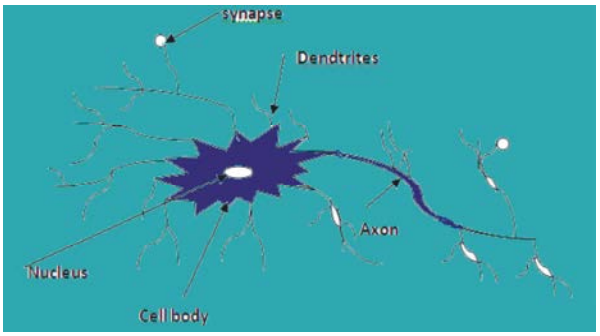

Fig. 1: Biological neuron

Artificial Neural Network: Artificial Neural Network has been drawn to VLSI industry for its unique traits of very high performance computing, tremendous significance and intelligence in processing the signals information and data. It derives its origin from human neural system of brain, which consist of massively large interconnections of neurons. Artificial neural network is slightly different from the conventional computer with unceasingly small amount of processing time and computational capability that exist in human brain and it is extensively unique from processors in the computers in terms of speed. Neurons will process the information in the span of 1ms which is slow when compared with the silicon compiler that works in ns, but the human nervous system is made up of large concurrent neural interconnections that perform the task faster than the today's computers. Artificial neural network tries to process the information based on experience and intelligence. But the human brain neural mechanism can't be completely mimicked, because it has billions of neurons and trillions of interconnections to do the task and it exploits the non-linearity of hierarchy of output so it can be used to process the information because the real world problems are purely non-linear, technical parameters of the system can be adjusted so that it is easy to obtain the desired results with minimum hardware in analog VLSI. Analog VLSI plays its vital role in processing the non-linear signal with massive parallel interconnections [6]. Another useful traits of neural network is its fault tolerance not leading to disastrous failure [7].

Back Propogation Algorithm: To obtain local minima back propagation algorithm is used in the proposed architecture. The neurons of multilayer architecture are connected to several nodes[8,9]. The output unit in n layer passing their activation function to n+1 layer. In multilayer signal processing error propagates in unforeseen paths through the successive layers.

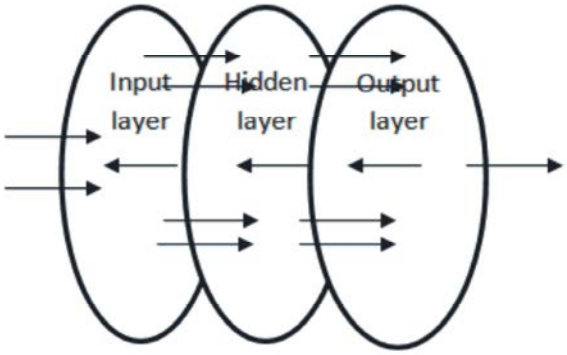

Fig. 2: Representation of Back Propagation Algorithm

Back propagation algorithm can be efficiently used by adjusting the weights to minimize the error signal at the output [10]. The activation function used here for back propagation algorithm is tangential sigmoid function which is CMOS differential amplifier.

Neuron Computation: Each input is multiplied and weighted. i.e., multiplied by some analog inputs. Let us consider two inputs and the weights are multiplied by corresponding integers. In this example input one and input two are multiplied and summed, when the output voltage exceeds threshold voltage or if it is positive integer it will produce binary '1'. If the output below the threshold voltage or if it is positive integer, it will produce binary '0'.

Input 1 *Weight 0 ◎ 24* 0.5 =12 (1)
Input 2 * Weight 1 ◎ 4 * -1 = -4 (2)

Sum inputs: The weighted inputs are then summed.

Sum = 12+ (-4) = 8 (3)
Output f(8)=1 (4)

Facets of Neural Architecture

Analog Neural Network: In this proposed neural network architecture we mainly focus to obtain the local minima at the final tape out. ANN has three layers are input layer, hidden layer and output layer with 2:3:1 structure as shown in the fig. 3 [11].

It comprises number of Multipliers, Adders and MOS differential amplifiers. The input is fed to the transconductance amplifier and the weights are updated simultaneously and added up. Gilbert multiplier itself will act as summer. The output of this adder is given to differential amplifier and differential amplifier is a neuron activation function which is tan-sig function [11].

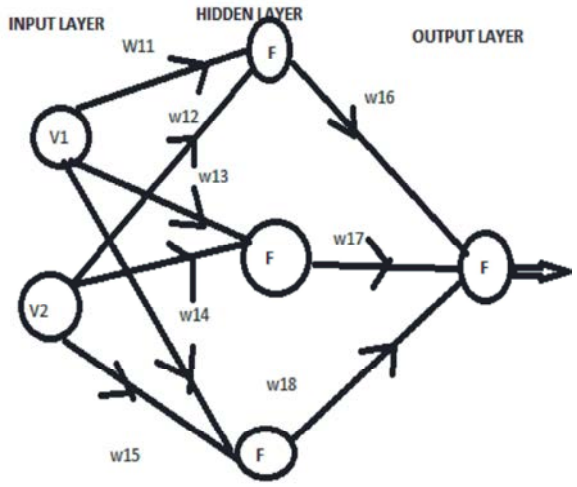

Fig. 3: Three hidden layered structure of Artificial Neural Network

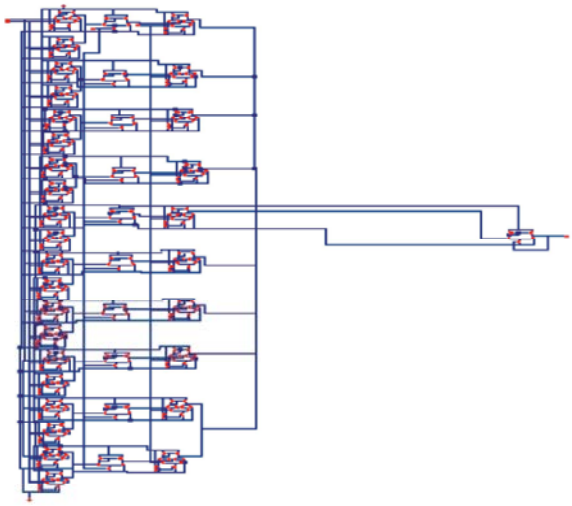

Fig. 4: Schematic design of Ten Hidden layer neural network in Electric CAD tool

The processed input will be fed with reference input to the neuron activation function. Neural network here is trained using these two inputs and the output will be the difference between two signals but it will operate on two modes.

- Differential mode
- Common mode

In differential mode two different inputs are fed and processed. But the common mode configuration will process the signal which are unique and the same signal rejected it will amplify the signals which has different phase. Hence it is sanguine that the output of this activation function can be adapted with the reference input signal to get precise results and local minima. The low frequency signals can be subtracted from the high frequency signals with the help of this proposed architecture. The back propagation algorithm feed forward the input and update the weights [8]. The reference signal can be altered in phase in accordance with the multiplier output to reject the common mode signal and to capture the difference signal. This architecture will be implemented in Analog VLSI for low power consumption and higher parallelism. When a number of single cell layers are connected with each other it forms a multiple layer as shown in the fig.3 w11 to w16 are the weight inputs connecting the input layers to the hidden layer. The weights w21 to w23 propagates the output voltage to the output layer.

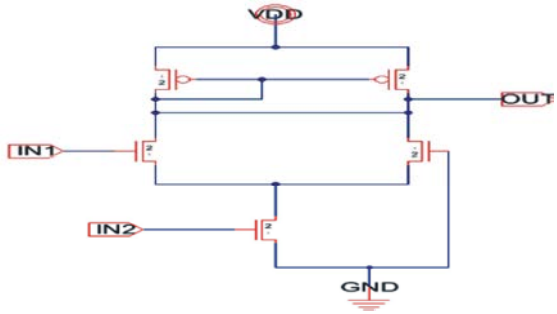

Fig. 5: Schematic design of NAF

Schematic of Proposed Ten Hidden Layer Architecture: In this architecture last stage produces the outputs which are signal with reduced error, which can be back propagated and the weight can be adjusted to yield minimum mean square error signal as shown in Fig 4. This multilayer perceptron network with the help of back propagation algorithm that follows supervised learning through neural network training. In back propagation algorithm, it trains the network by comparing the output with the target for processing the data further and by adding weights corresponding to the output [9]. This multi layered perceptron uses nonlinear activation function as shown in Fig 5.

Neural Architecture Blocks: CMOS diferential amplifier is used as an activation function.This tan sigmoid activation function is actually a single ended two input amplifier,and it works as a neuron activation function in the subthreshold region and current mirror circit is formed with the help of active load.

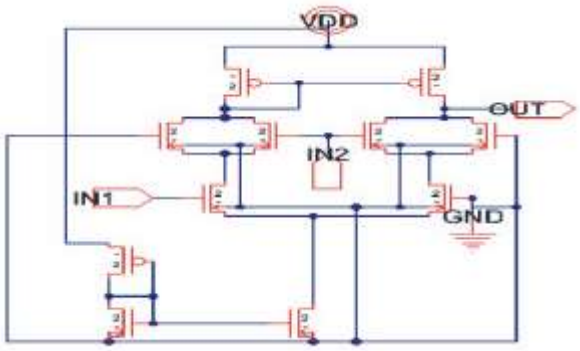

Fig. 6: Schematic of Gilbert multiplier cell

The non linear expression of the tan sigmoid activation function is given in equation (4). To porduce the non-linear output the non-linear activation function is employed follwed by a linear network to process the real world problems which are non-linear.

$$F(x)=\frac{1}{1+e^{-x}} \quad (4)$$

Gilbert Multiplier Cell: Gilbert multiplier cell takes two input and produces the single ended output which is equal to product of their inputs [2,3]. It can be used as voltage multiplier and frequency multiplier. It acts as a phase detector when the two input voltages are more than the threshold voltage of amplifier. Gilbert multiplier is one of the mail processing element in the analog neural processing since it performs both multiplication and addition in the same network and it converts the input voltage into output current and again back to output voltage with the aid of current mirror circuit. It has multiplier adder summing nodes and current mirror circuit as shown in Fig 6.

RESULTS

Output of Synapse as Multiplier: A small signal four quadrant multiplier with the condition of both inputs are being small when compared with V_T (threshold voltage) of 0.025V to produce the accurate output with much less distorted output. This analog multiplier which uses the operational amplifier is more susceptible to noise.

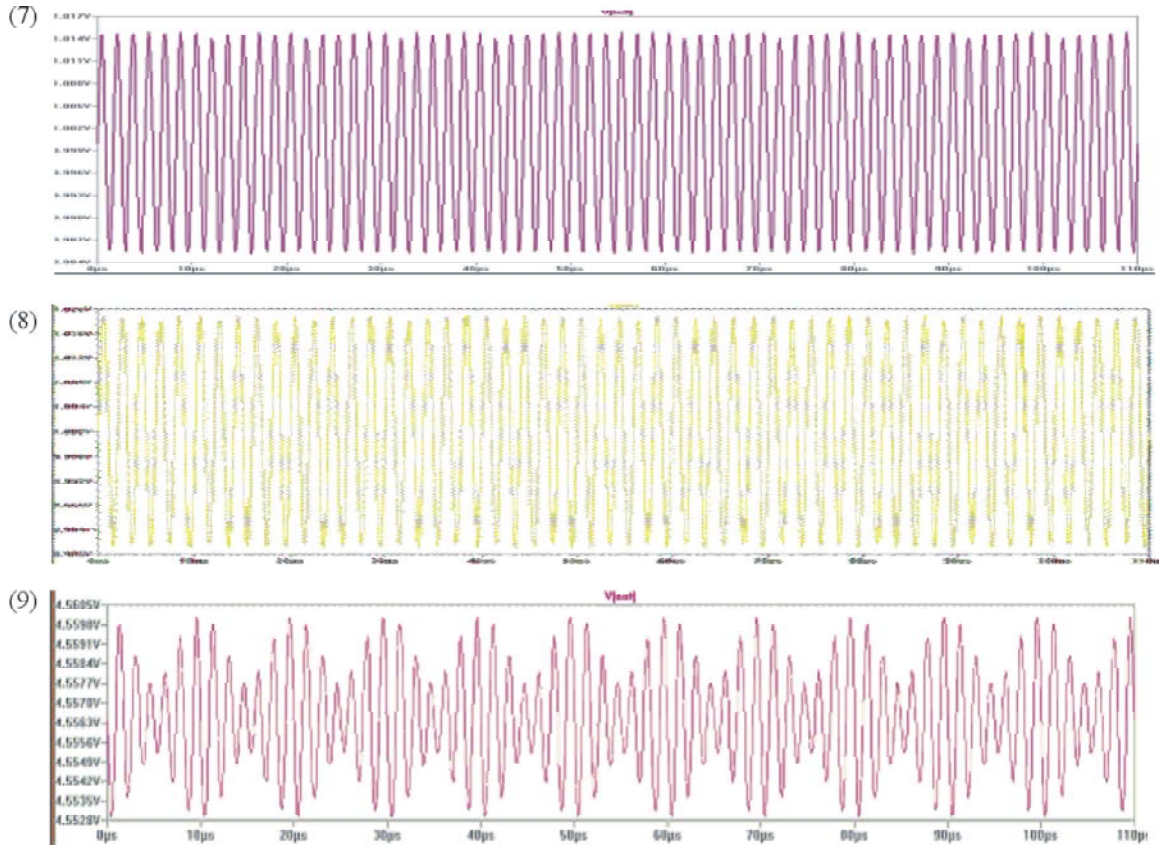

Fig. 7,8&9: Voltage versus time response of four quadrant multiplication of two Differential inputs of analog gilbert multiplier cell multiplier using CMOS devices for adapting the synapses(weight parameters)

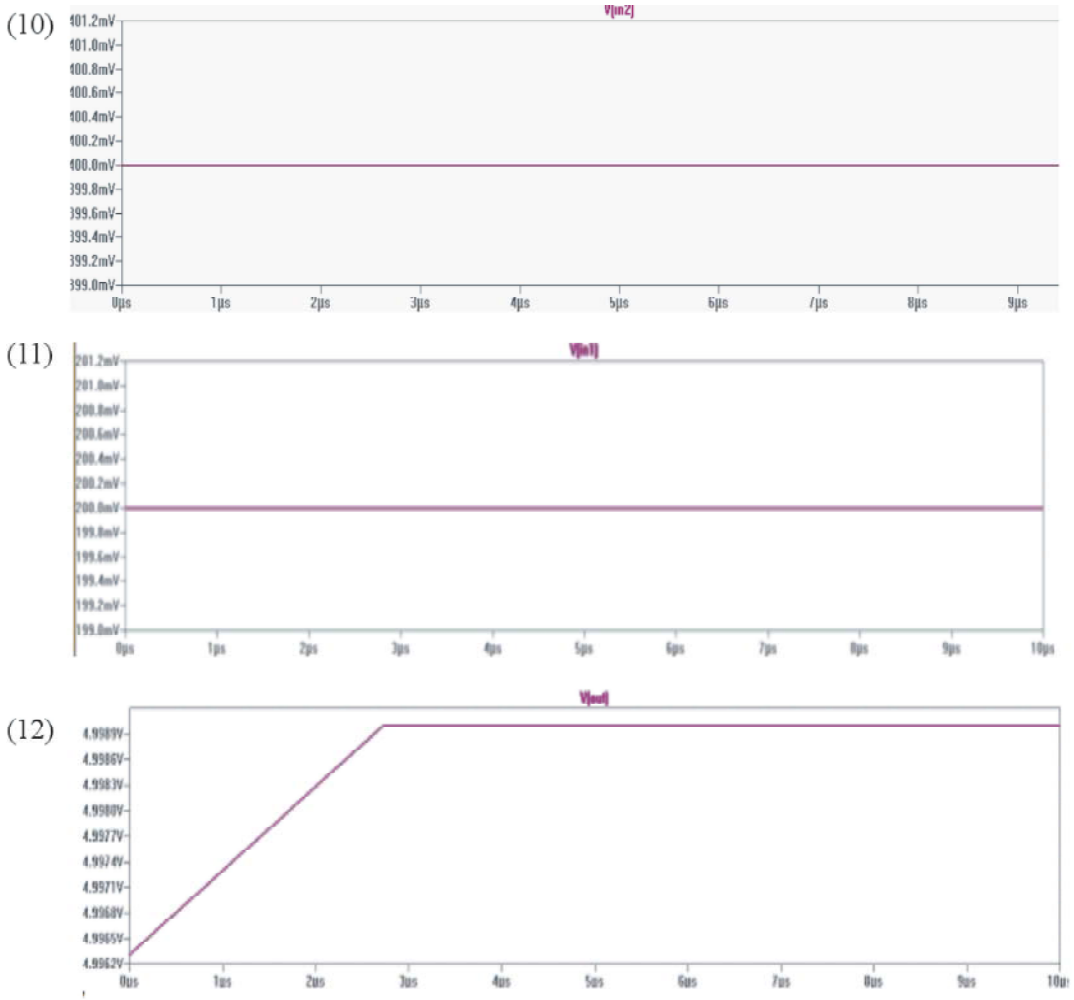

Fig. 10,11&12: Voltage versus time response of CMOS differential amplifier as neuron activation function.

So that it may lead to a highly distorted output. But the Gilbert multiplier is a linear four quadrant cell which produces the output of amplitude modulated signal which is directly proportional to the linear multiplication of two input signals of 0.019 and 0.015 are V1 and V2 respectively as shown in the Fig 7 and Fig 8. The output shows that it works on the sub-threshold region which produces he output of 4.5V with 18KHz frequency as shown in Fig 9.

Transient Analysis of Neuron Activation Function: Neuron activation function produces single ended output with two different input signals, which amplify the difference between two input signals.CMOS amplifier is excited with two different DC input signals are V1 as 2Vpp and V2 as 4Vpp and it is shown in Fig 10 and 11 and it produces the non-linear signal at the output which is equal to the 498mV with 18KHz of frequency, as shown in the Fig 12.

Transient Response of Multi-Layer Perceptron: The simulation results for signal processing with multi layered neural network architecture is shown in the Fig 13, which is the transient analysis of the proposed architecture for obtaining the minimum mean square error using the concurrent interconnections. Higher the parallelism and interconnections lesser will be the error signal at the output. The proposed architecture is not highly made parallel but it is designed with multiple layers using back propagation algorithm. Due to the simulation time, cost function and non-flexibility of analog neural network it is not made with large number of interconnections to obtain the more precise output. The figure 13 shows the output of ten hidden layer architecture for V1 as 1.115V, V2 as 1.009V and V3 as 984.35mV with the output of 364.2mV which is the minimum output that can be obtained.

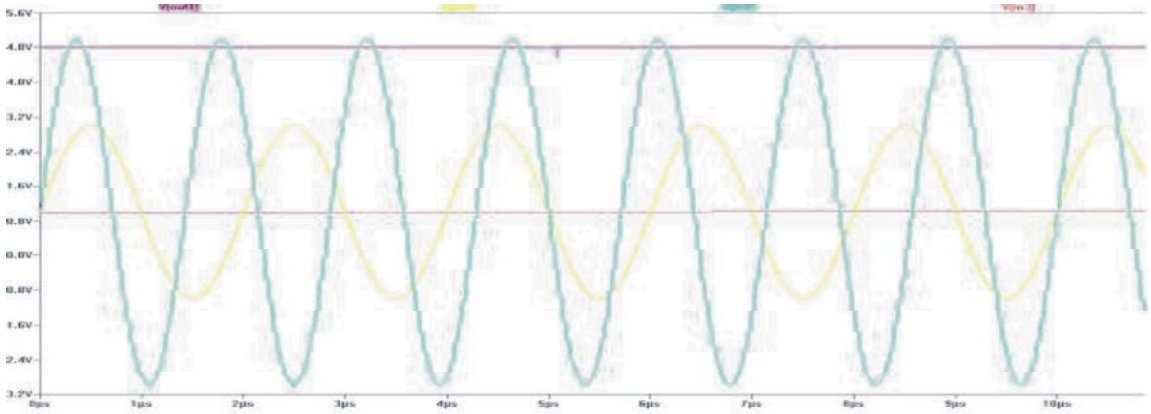

Fig. 13: Voltage versus time response of multi layered neural network architecture

CONCLUSION

A VLSI implementation of artificial neural network has been demonstrated in this paper. It describes the analog circuits used to implement axon, neurons and non-linear elements. Neural network architecture is widely used in real world interfaces and it can be implemented in both analog and digital VLSI. But in this work we have implemented the proposed architecture in analog VLSI. Since it does not need any signal converters and it can be directly interfaced with physical sensors and it can be used in Lung sound signal analysis. This paper emphasises an important role of technology in analog IC design with an effective multi layered(Ten hidden layer) architecture for generating the minimum mean square error.This paper shows that proposed architecture yields better results than existing network.Hence it is sanguine that the performance of backpropogation algorithm yields precise results for getting local minima.The simulation part of the proposed architecture is verified Electric VLSI CAD tool in 180nm technology.

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