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Optimization of Energy Usage in Orthogonal Frequency-Division Multiplexing Networks

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Abstract: Recently wireless local networks and wireless connection network technology are increasing data rate that only can be obtained in frequencies more than 200 GHz. In japan, United States and European countries bands with frequencies more than 200 GHz that make them accessible for implementing WLAN networks or radio connection network are unallowable. Other advantages of transmitters more than 200 GHz. includes eliminating packing and chip antennas that usually have microscale elements arrangement. As long as technology progresses economic modern consumers demand for wireless systems that has less cost, less energy usage and have smaller apparent factors. Thus more attempts is carrying out for design of circuit for wireless systems, for design of transmitter-receptor one chip in technology with optimized cost. This requires examination of new transmitter-receptor architecture and circuit design technics that brings about integrated and balanced RF transmitter- receptor. In this paper it is tried to examine energy usage optimization in orthogonal frequency-division multiplexing networks.

Key words:

INTRODUCTION

In future wireless communication systems the 60 GHz band is considered to be used in several cases such as multimedia communication, inter-vehicle communication and roadside communication [1]. To enable such systems, signal generation with stabilized frequency and low phase noise is needed. The signal can be generated either directly by a fundamental-frequency oscillator or by the combination of a low frequency integrated oscillator and a few frequency-multiplier stages. The use of frequency multipliers to create millimeter-wave signals is an attractive alternative to direct generation of the signal if phase locking is required since, in this case, frequency dividers are required. Frequency dividers are not available commercially for mm-waves and in addition, they consume significantly more dc-power. In this section we briefly explain dynamics of phase locking loops (PLL) is a closed loop control system that consists from a phase detector (PD), a low-pass filter F(s) and a voltage control oscillator (VCO) that VCO synchronize a location to input signal vi(t). this action takes place by adjusting frequency of VCO according with vc(t) and filter response to output is PD namely vd(s) [2].

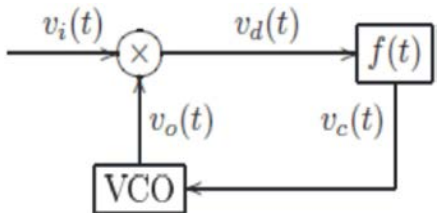

Fig. 1: Diagram block of PLL

Input and output signal are stated as follows:

$$v_i(t) = v_i \sin(\omega_M t + \theta_i(t)) \quad (1)$$

And

$$v_0(t) = v_0 \cos(\omega_M t + \theta_0(t)) \quad (2)$$

Respectively θ_0 is loop estimative to imput phase θ_i, v_i and v_0 are signal domains. Since it is assumed that input and output signals, have has equal free-running ω_M (rad/s) phase error is defind as follows [3]:

$$\theta(t) = \theta_i(t) - \theta_0(t) \quad (3)$$

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Regarding equations (1), (2) and (3) it is determined that for $\theta(t) = 0$, there is a static phase difference $\pi/2$ *rad* between input and output.

PLL is described by differentiate equation of order P+l, considering this filter order f(t), is p.

First order low pass because their simple and reliable behavior in different application are widely useful in PLL design. In order to mathematic reasoning simplicity filter is considered as first order all-pole and is obtained as bellows [4];

$$F(s) = \frac{\alpha}{s+\beta} \tag{4}$$

Output of PD is obtained as follows:

$$v_d(t) = k_m v_i(t) v_0(t), \tag{5}$$

where Km is gain of PD. VCO frequency is controlled as follows:

$$\frac{d}{dt}\theta_0(t) = k_0 v_c(t), \tag{6}$$

And K_0 is VCO gain and v_c is filter output and is obtained by convolution.

$$v_c(t) = \mathrm{f}(t) * v_d(t) \tag{7}$$

G loop gain is defined as follows:

$$G = \frac{1}{2} k_m k_{\cdot} v_i v_0 \tag{8}$$

Considering above relations, convolution and trigonometric identity we have:

$$\sin(A)\cos(B) = \frac{1}{2}[\sin(\mathrm{A} - \mathrm{B}) + \sin(A + B)] \tag{9}$$

Phase error dynamics is obtained as:

$$\ddot{\vartheta}(t) + \beta\,\dot{\vartheta}(t) + \alpha\,\mathrm{G}\sin(\vartheta(t)) = \ddot{\theta}_i(t) + \beta\,\dot{\theta}_i(t) - \alpha\,\mathrm{G}\sin\big(2(\omega_M t + \theta_i(t)) - \theta(t)\big) \tag{10}$$

Phase difference and double frequency relations in equation (10) is responsible of observed nonlinear behavior in PLLs [5].

Another advantage of signal production using multipliers is lower phase noises, because lowest phase noise VCOs is identified in lowest frequencies. Most active multipliers are configured as doublers frequency or quadruplers. The purpose of this work is to develop a 60 GHz local oscillator (LO) chain based on phemt technology for further integration in single chip transmitter-receiver circuit. In what follows we discussed doubler frequency and quadruplers [6].

In this paper, a frequency doubler circuit is presented that converts a 0.6 GHz signal to a 1.2 GHz output using standard CMOS 0.18 mum technology. The proposed circuit uses a time-delay element and an XOR logic gate to perform the frequency multiplication and is implemented entirely on-chip. Explanation of this design is as follows[7]:

In this project a frequency doubler circuit is presented that converts a 0.6 GHz signal to a 1.2 GHz according to Figure 3-2. Using this technic multiplex frequency can be obtained with low energy usage and low chip area and good inherent rejection of undesired frequency components. An important advantage of this topology is that an excellent fundamental suppression can be obtained in output without filtering. Simplified schematic of doubler frequency is shown in Figure 3-3. Since circuit input is sinusoidal and doubler circuit needs a square wave, that is the first stage of generating this change. For this purpose a shifting circuit of Dc- level is used after a series of converters. DC-level shifting circuit, offsets input signal to convertors threshold voltage. Then convertors produce a square wave with high quality for core doubler circuitry [8].

Integrator is implemented with use of RC integrator. RC network approximate ideal integral when input signal period is small regarding time constant of RX. As RC integrator becomes near to ideal integrator, output triangular wave domain becomes smaller, as a result in subsequent stage determining proper situation for comparator is more difficult. For implementing comparator circuit at first a common source amplifier for strengthening triangle wave is used then the convertors are applied. Using this configuration for comparator adds a small excessive delay to T/4 but cannot be used in higher frequencies because this delay becomes significan' [9].

Xor gate with use of transfer gates (Brown and Vranesic 2000) and converter is produced in such manner that is shown in Figure 3-3. Output of this square wave circuit is in input double frequency. If sinusoidal output is considered, a simple pass filter can be used for attenuate higher harmonics in square wave. This circuit layout can be completely continuous and in this implementation approximate area of $200\mu m \times 75\mu m$ ($0.015 mm^2$) is required for core doubler circuitry. Area of complete chip is $400\mu m \times 400\mu m$ and include bonding pads [10].

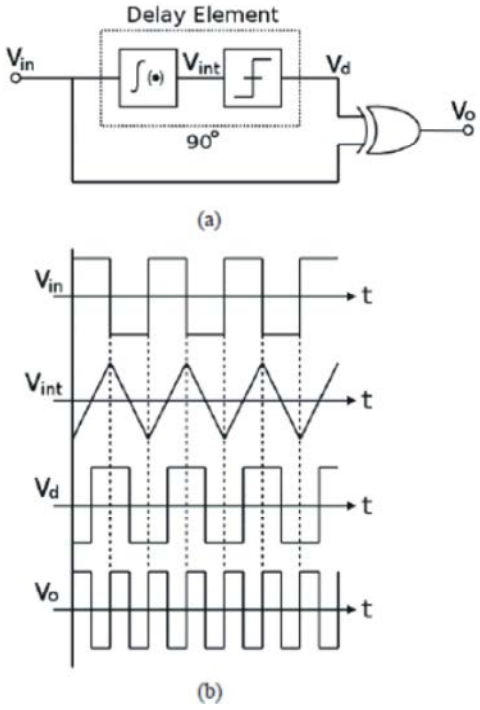


Fig. 2: (a) block diagram of frequency doubler and (b) waveforms

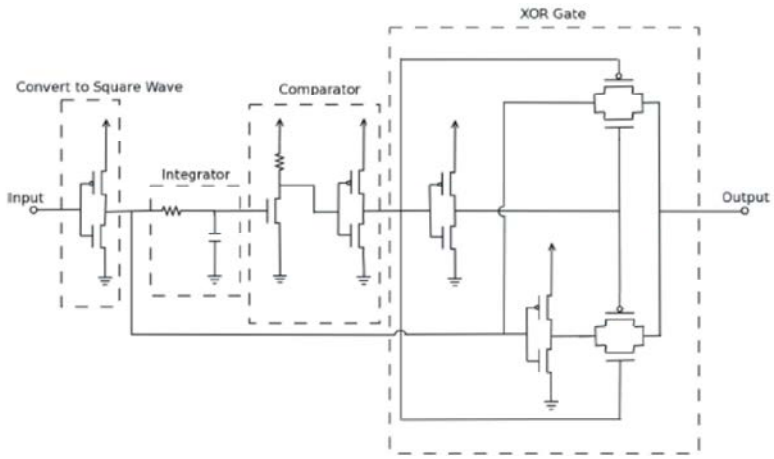


Fig. 3:

Souliotis *et al*., (2012) studied a frequency quadrupler 90 nm CMOS 15/60 Ghz. In their research converting 15 GHz to 60 GHz is on the basis of topology that is shown in figure 4-3. This topology includes frequency doubler, a polyphase filter, gain amplifier and bias circuit. Following some trade-offs some decisions must be taken for optimized design. First decision addresses the type of frequency doubler, that finally a passive double-balanced mixer is selected. Advantage of this topology comparing with other topology is its higher linearity. Advantages of this doubler is its need to a high level signal toward LO input. While at the same time shows high conversion loss. As a result output signal must be strengthened before that guide subsequent stages. Furthermore it must be considered that this output guide second frequency doubler and this doubler requires a high output level. Therefore two gain multipliers must be used after first frequency doubler. Especially two LO amplifiers in cascade are used for strengthening doubler output, that lead to a gain that almost equals to 15 dB. Next stage includes redoubling frequency from 30GHz to 60 GHz. But such doubler requires two different signals from same frequency but it changes up to 90° [11].

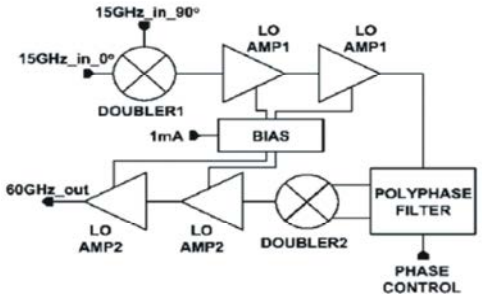


Fig. 4: Complete topology of quadrupler

Therefore a polyphase filter is annexed before doubler that produces two signals that changed 90° in frequency of 30 GHz. For preventing excessive use of another polyphase filter before first doubler, two shifted signals are produced by quad VCO output, therefore decrease in number of polyphase filters is required. The type of used polyphase filter if change of phase angle deviate from required number, present good adjustability. Second doubler that emerges after polyphase filter leads to doubling of frequency from 30 GHz to 60 GHz. repeatedly, doubler output that is attenuated significantly must be strengthened. Furthermore two gain LO amplifiers for signal guidance is used that delivers final output of $70mV_{pp}$ [12-20].

In research of [20] highly integrated transmitter and receiver of MMICs is process of $0.15\mu m$, 88 $Ghz\ f_T$ / 183 $Ghz\ f_{MAX}$ *GaAs pHEMT MMIC* is designs and is described on the basis of system and chip level. These chips have showed highest level of integration presented to date in band of 60 GHz. This system works with LO signal in range of 7-9 GHz. This LO signal is multiplied in X8 LO integrated chain that leads to center frequency of 2.5 GHz IF. Though chips are inherently designed for multiple purposes, especially they are appropriate for wireless data transfer with high speed due to IF broad band characteristics. X8 is a multifunction design that only includes a quadrupler, a feedback amplifier, a double and a buffer amplifier. TX chip (transmitter) includes a three stages RF amplifier, a balanced mixer with integrated IF-balun and an X8 LO chain. RX chip (receiver) includes a low noise three stages amplifier (LAN), an image reject mixer with hybrid integrated IF and a X8 LO chain such as TX chip (figure 6-3). Both chips are designed for assembly of flip-chip [13].

In a research conducted by Karnfelt et al (2005) an X8 multiplier was designed and implemented on unit chip using phemt GaAs 0.15 μm technology and in continue we imply on circuit design and measurement in this research [14].

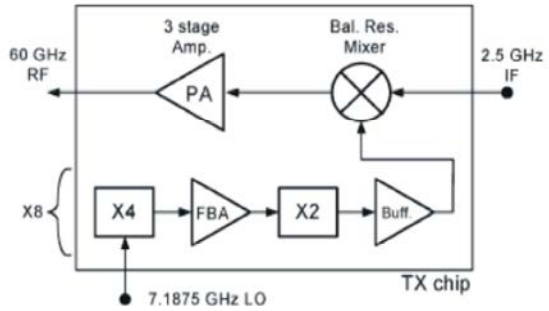


Fig. 5: Circuit block diagram of TX chip

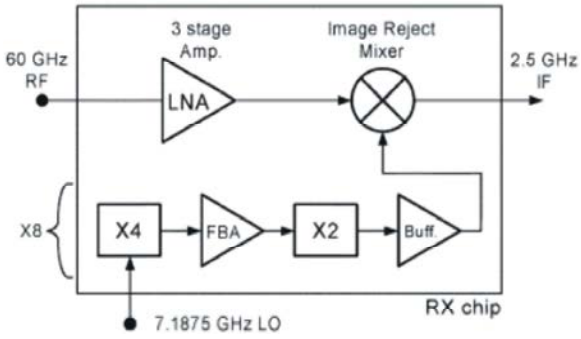


Fig. 6: Block diagram of circuit of RX chip

Circuit Design and Measurements: Objective of the design carried out by Karnfelt et al (2005) is producing a bandwidth multiplier to provide VCO frequency values from 7.0 GHz to 7.7 GHZ with output power of $8^{th}$of harmonic 10 dBM. Output power is assigned to 0 dBM. Eliminating other harmonics (main, 2^{nd}, 3^{rd},…, 7^{th}) is assigned more than 20 dB beneath 8^{th} harmonic.

According to 7-3diagram X8 multiplier have a circuit topography. This topography includes a quadrupler leading to a doubler and two stages buffer amplifier in output. This topology is selected to performing high level of integration that this is carried out only by two X4 and X2 multiplier. Input matching and interstage amplification is designed too in order to minimizing area of chip design [15].

Each part of LO chain is produced as break out circuit. This provide possibility of examining break out circuits separately before complete evaluation of X8. X* unit chip image is showed in Figure 8-3 [16].

Used measurement equipment in this practice includes a PAN network of E8361A analyzer for measuring S parameter. A HP83650B synthesizer is used as input signal source and output power is assessed by use of a spectrum analyzer HP8565EC with pre-selector HP11974. HP4419B is used with power sensor V8486A for examining received power by spectrum analyzer [17].

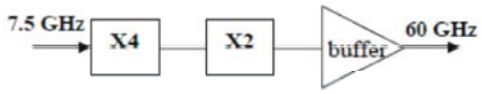


Fig. 7: General representation of multiplier circuit

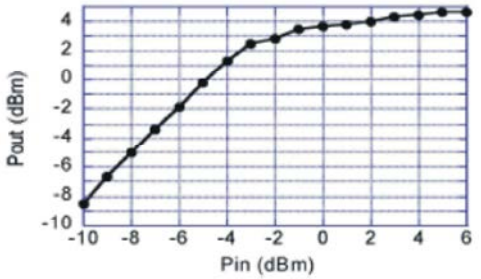


Fig. 8:

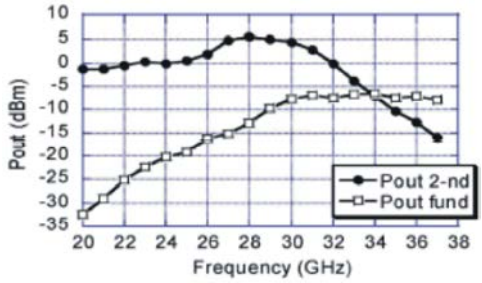


Fig. 9:

The Doubler with Feedback Amplifier: Frequency doubler is constituted from a feedback amplifier (FBA) and a one stage doubler. FBA is received by negative feedback technique so that we can obtain to a vast bandwidth with small gain change and improved stability. Due to sequence of feedback, this amplifier has a flat response and a 3dB bandwidth in a domain of 15.5 to 40 GHZ [18].

The stage of doubler (x2) in pinch-off voltage takes place for optimized multiplication conditions. This bias voltage is useful for minimizing power loss. By effective frequency rejection more than 20 dB through high-pass filter, the output will be obtained [19].

Figure 9 shows complete doublers measurements with feedback amplifier. Compaction point of 1-dB is in -4 dBm of output power, when input power is 2 dBm (namely value of delivered power from quadrupler) output power is 4 dBm [20].

Figure 9 measured output power from second harmonic related to two stages doubler versus input power in input frequency of 29 GHz

Output power depends on input frequency that is shown in figure 10 and also second harmonic and main frequency is presented in this Figure [21].

Measured output power versus second harmonic frequency and main frequency for stage of doubler[22].

Input power is 0 dBm.

When input frequency is within 26 to 32 GHz, at input power of 0 dBm, doubler output power is more than 0 dBm. In input frequency of 28 GHz maximum output power is obtained 5 dBM. Rejection of main signal fluctuate within 18 dB in lowest level to 10 dB in highest level of frequency band[23].

Finally it can be said that in Karnfelt et al research x8 MMIC frequency multiplier an unit chip is designed and it described that output power more than 7 dBm is obtained from frequency of 52 to 61 GHz. Measured phase noise loss of 18.5±0.5 dB shows that this circuit is an appropriate alternative for achieving to low phase noise demands of LO chain with mm- wave [24].

Design Implementation: General block diagram proposed for implementing this design is shown in Figure 11-3. In this figure at first input frequency 6-8 GHz enters in main multiplier circuit and then its output signal enter band pass filter to attenuate undesired signals and 12-16 GHz signal passes. Then by use of a typical amplifier for example a Hittite company products it is amplified and reach to necessary power level. Finally output signal harmonics is attenuated by a low pass filter [25].

In continue of the report we explain detail design and calculation and simulation of each one of blocks[26].

Frequency Multiplier Block: As it is shown in Figure 11-3 for main multiplier a FET transistor is used that is main objective of this project. This transistor must present desired output in terms of frequency and power level by appropriate design in terms of input and output regulatory circuit and required gate voltage. In selecting desired transistor following points are considered:

- Selected transistor in input frequency band has desired gain and in output frequency has capability to work
- Transistor has a desirable saturation point and can work with desired input power.

After exerting above conditions several transistors are selected that NE32400 transistor from NEC factory was used. This transistor has I_D-V_{DS} feature according to figure 3-12. Because objective of the design is frequency doubler and nonlinear mode of transistor is addressed, transistor bias point in selected mode is selected in the Figure [27].

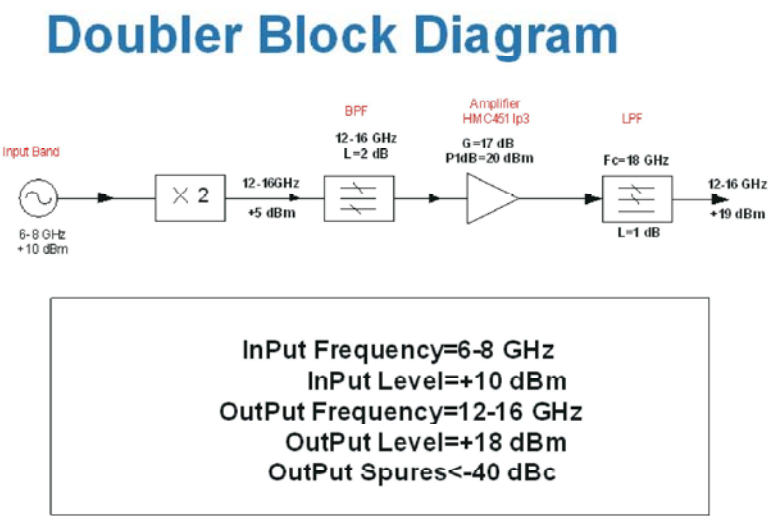


Fig. 10:

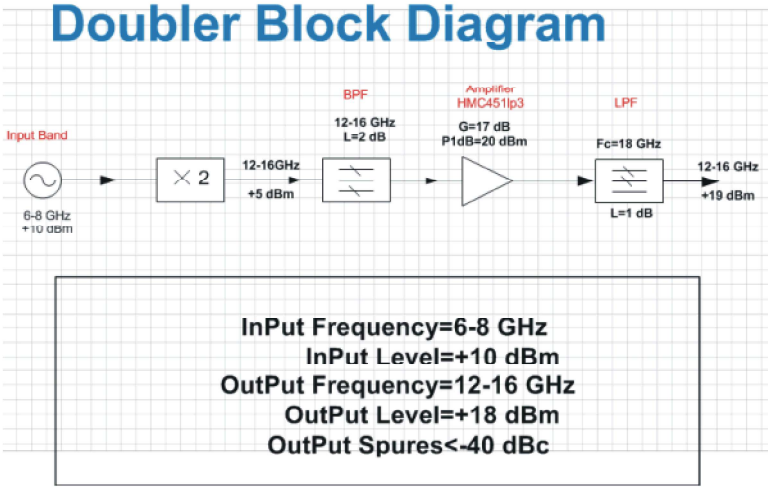


Fig. 11: Proposed block diagram of frequency doubler

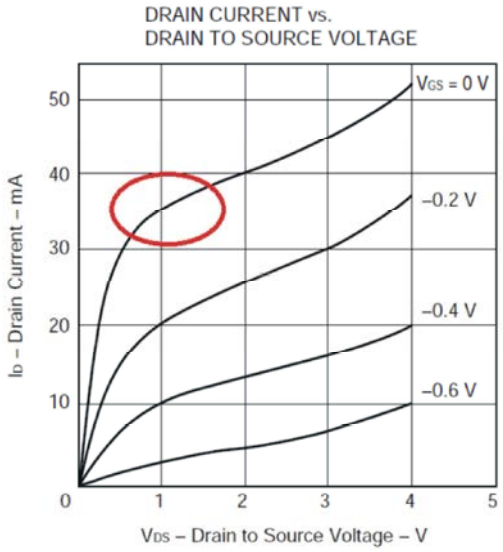


Fig. 12: Transistor I_D-V_{DS} feature

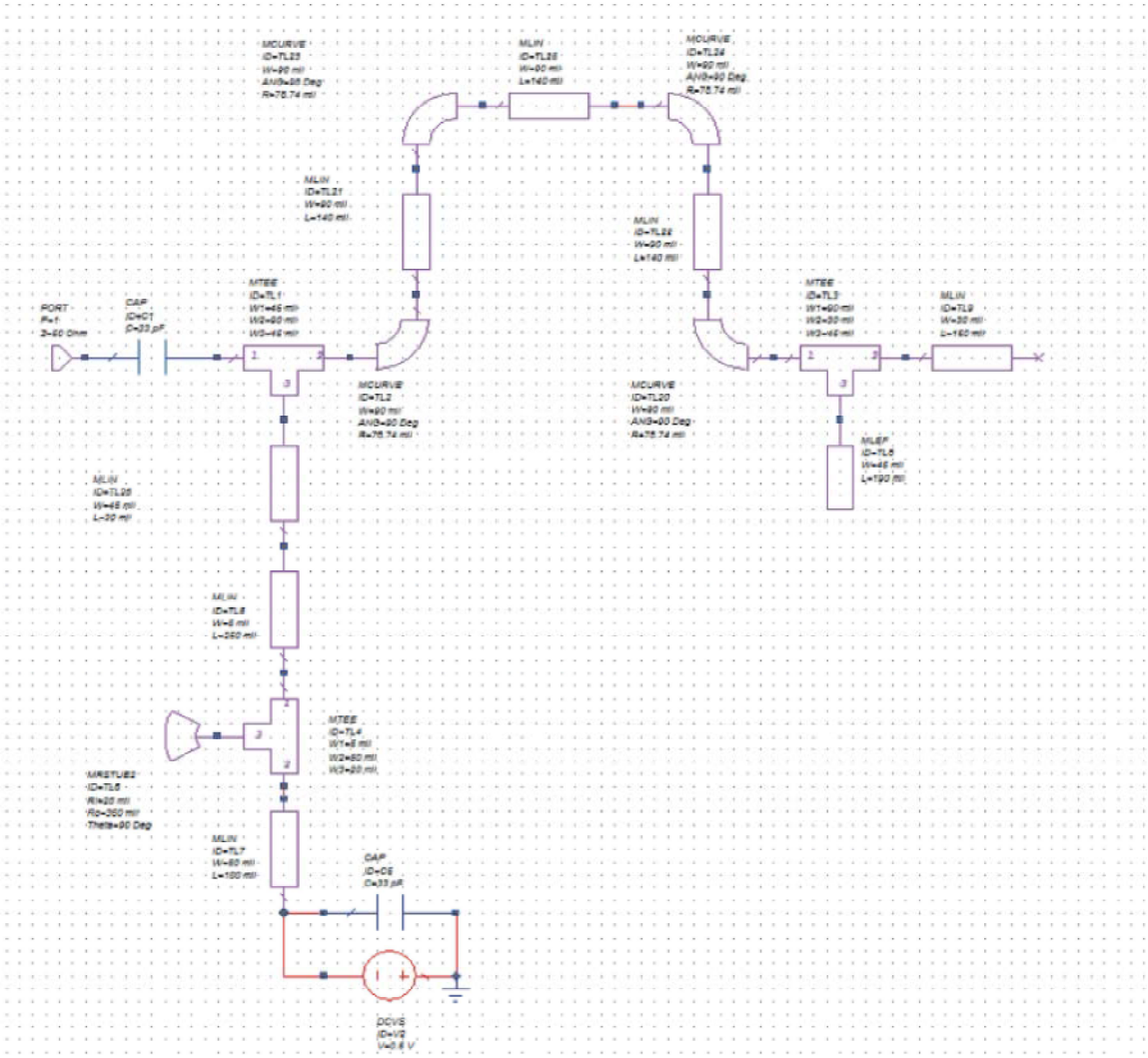


Fig. 13: Input microwave regulatory circuit for transistor

After selecting transistor bias point, input and output regulatory circuits must be designed.

For design of input and output regulatory circuits in frequency range of 6-8 GHz and obtaining desired transfer gain we take action as follows. It is necessary to mention that optimization of input and output circuits was carried out by Matlab software. Calculation relating to gain of a transistor and its stability conditions are as follow:

$$MSG. = \frac{|S_{21}|}{|S_{12}|} \qquad K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2\,|S_{12}|\,|S_{21}|}$$

$$MAG. = \frac{|S_{21}|}{|S_{12}|}\left(K \pm \sqrt{k^2 - 1}\right) \qquad \Delta = S_{11} \cdot S_{22} - S_{21} \cdot S_{12}$$

Regarding this condition and above relations and using optimizing software AWR necessary values for this element can be obtained too [28].

For simulation of regulatory circuits obtained with transfer lines it should reach to desired impedance by optimizing length and width. Since calculation of length and width of desired transfer line using above relations is time consuming and necessitate high accuracy and long time this process is carried out by AWR software. After simulation of available impedances with transfer lines and desired optimization output and input regulatory circuit is obtained as follows:

Simulation Results: Now with extracting input and output microstrip equivalent circuit of multiplier the design is finished and for assuring the design correctness to desired parameters we simulated it by software. With exerting input power of 10 dBm in frequency range of 6-8 GHz, output values are obtained as follows [29]:

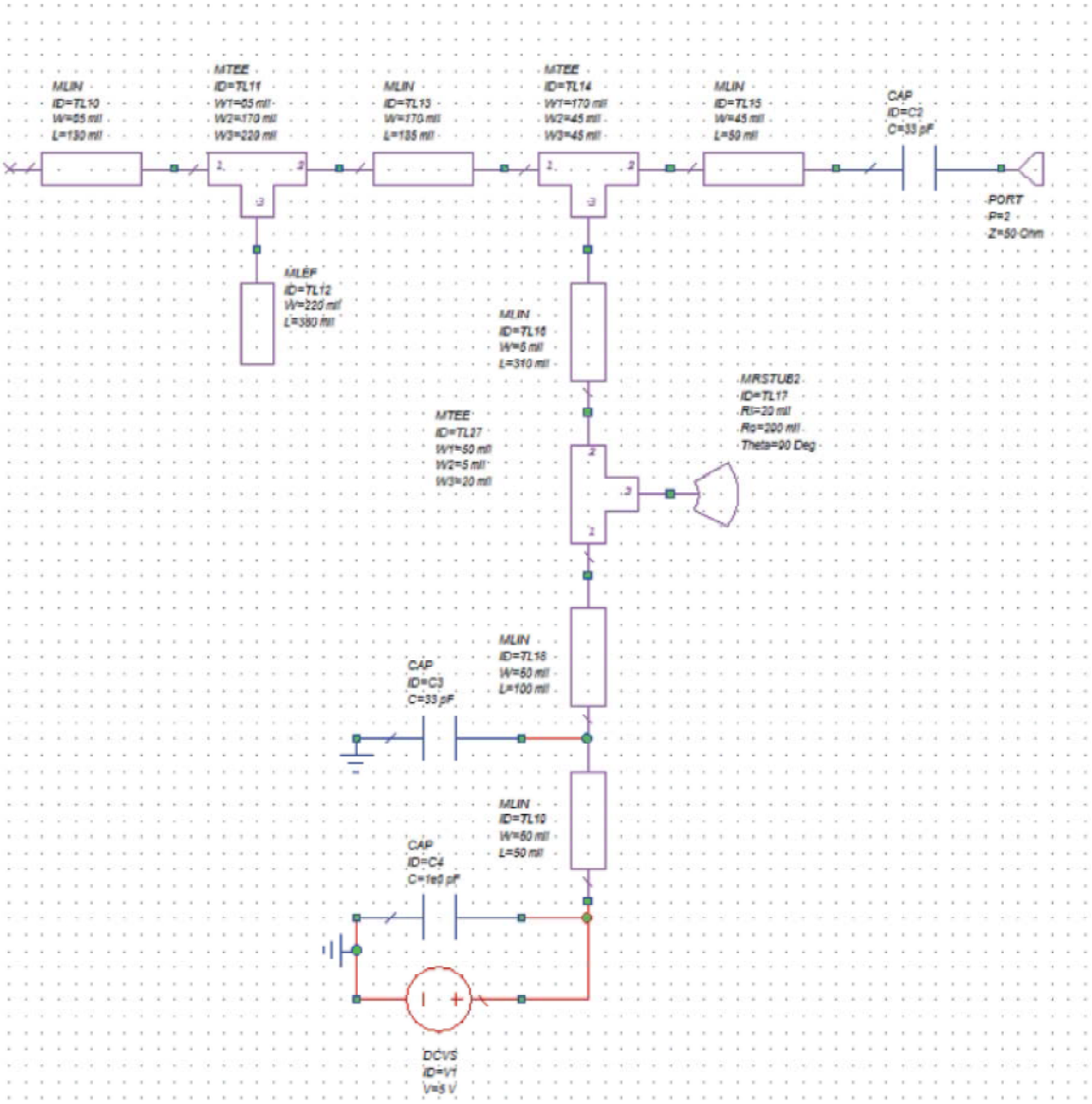


Fig. 14: Output microwave regulatory circuit for transistor

Two banded with frequency multiplier by use of transfer line CRLH

Frequency doubler with transfer lines of CRLH

Design goal is a two bands multiplier with CRLH line that has following specifications:

Table 1 specifications of two bands multiplier

Input frequency 9.5 - 10.67GHz & 11.7 – 12.7GHz

Input power +10dBm

Output frequency 19-21.34GHz & 23.4-25.4GHz

After selecting transistor bias point, at first it should design input and output regulatory circuits and then make it two-banded by CRLH transfer lines.

Following figure is an example of microstrip CRLH transfer line. In presented mode, series capacitor C_L is obtained by interdigital capacitors and inductance L_l is obtained by short circuit end inductances. Parasite capacitor C_R is produced by voltage difference between ground level and design level and parasite inductance L_R is considered from magnetic flux obtained from current flux in interdigital capacitors. This desired equivalent circuit is produced and CRLH line is provided [30].

In following figure CRLH transfer line is designed for input part is shown:

In following figure designed CRLH transfer line for output part is shown:

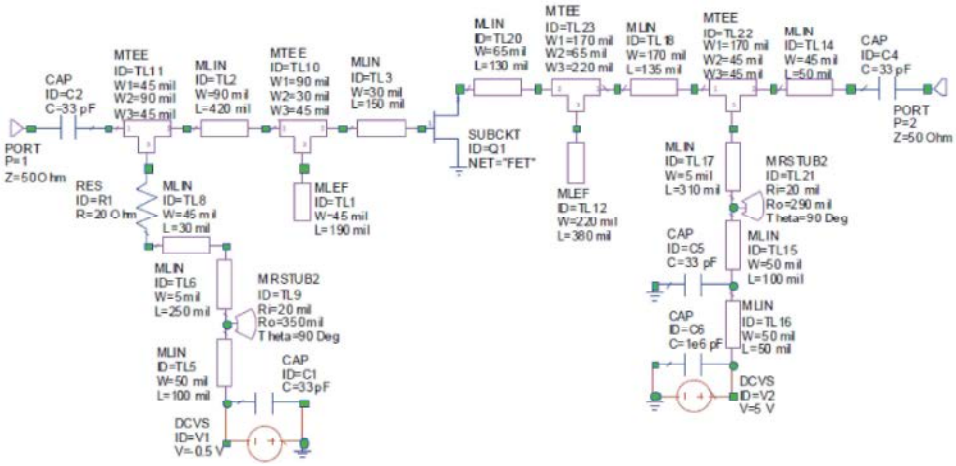


Fig. 15: Complete schematic of input and output microwave regulatory circuit for transistor in microstrip structure

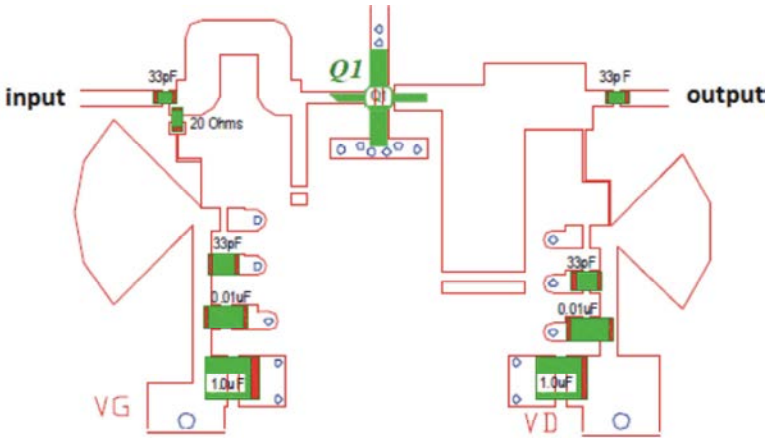


Fig. 16: Complete layout of input and output microwave regulatory circuit for transistor in microstrip structure

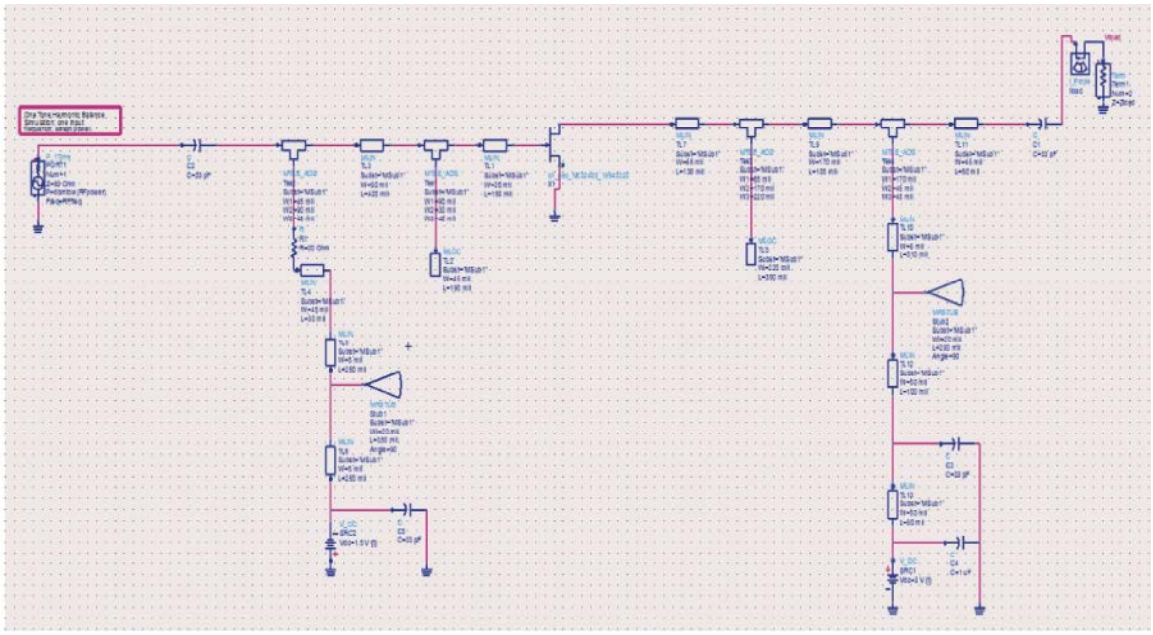


Fig. 17: Image of frequency multiplier majule in input range of 6-8 GHz

Fig. 21: Designed CRLH transfer line for input part

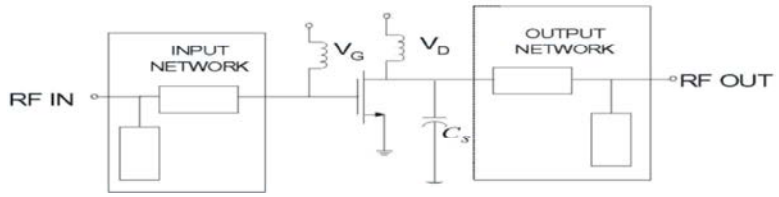


Fig. 22: Input and output regulatory circuits

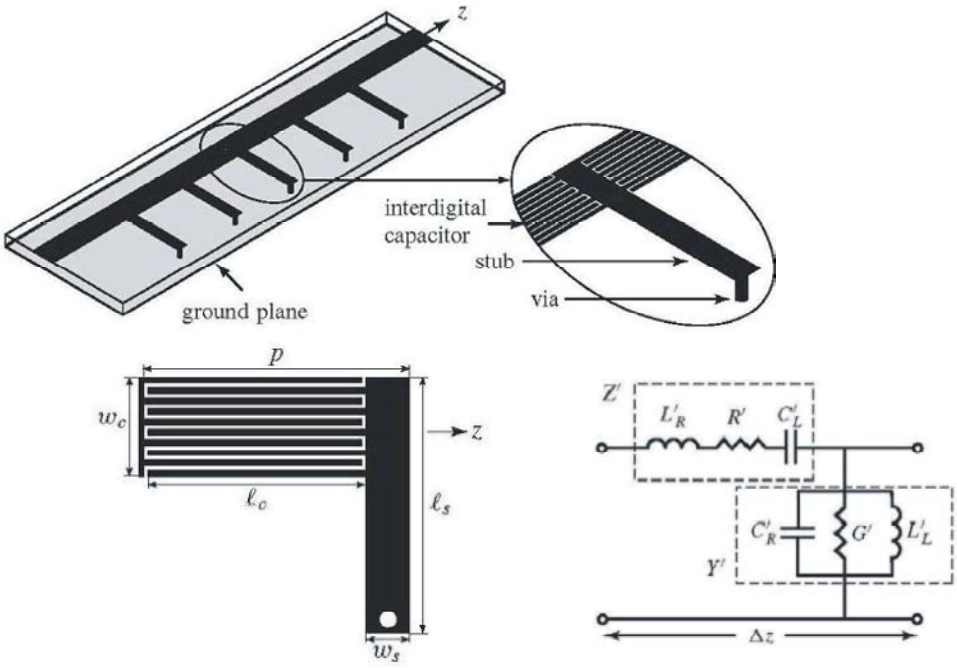


Fig. 23: An example of microstrip CRLH transfer line

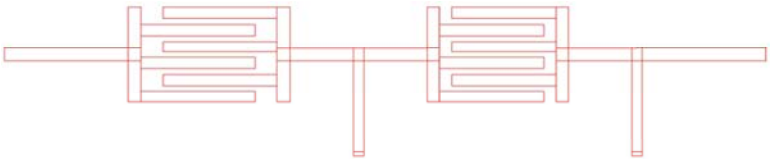


Fig. 25: Designed CRLH transfer line for output part

For depicting diagram of power added efficiency PAE % in terms of output power in ADS software we act as follows:

According to definition of PAE% for transistors is calculated by dividing difference between output and input power on transistor usage power, so regarding following figure we have:

PAE=100*((Pout _W-Pin_W[1])/Pdc) (11)

where in this relation:

Pdc=Is_h*Vs_h +Is_l*Vs_l +1e-20
Pin_W=0.5*real(Vinput*conj(Iinput.i))+1e-20
Pout_W=0.5*real(Vload*conj(Iload.i))+1e-20

With exerting above equations in software, diagrams of PAE % in terms of output power is calculated in different frequencies.

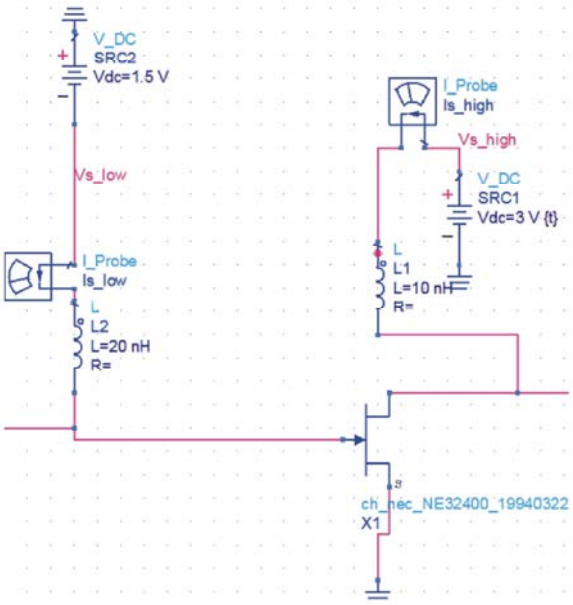
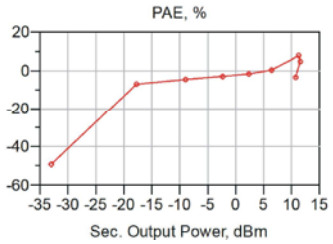
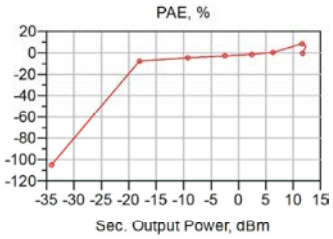


Fig. 26: PAE% in terms of output power in different frequencies



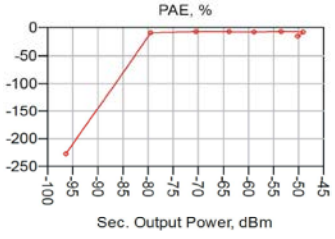
PAE diagrams in term of output power 10 Ghz

Fig. 27:



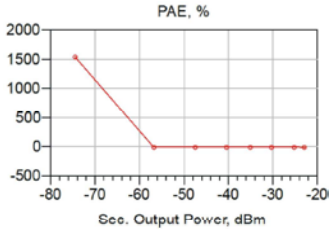
PAE diagrams in term of output power 10.6 GHz

Fig. 28:



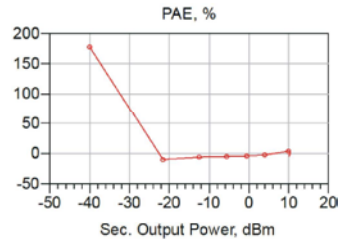
PAE diagrams in term of output power 11 GHz

Fig. 29:



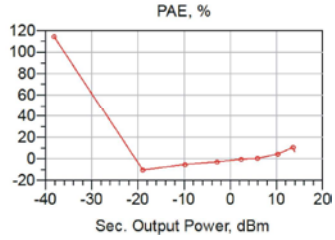
PAE diagrams in term of output power 11.5 GHz

Fig. 30



PAE diagrams in term of output power 12 GHz

Fig. 31:



PAE diagrams in term of output power 12.5 GHz

Fig. 32:

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