Middle-East Journal of Scientific Research 21 (6): 945-949, 2014
ISSN 1990-9233

DOI: 10.5829/idosi.mejsr.2014.21.06.21471

Simulation Analysis and Performance of the Reactive Components of MOS Structure Towards Small Size Vlsi Circuits

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Abstract: In this research thin film layers have been prepared at alternate layers of resistive and dielectric deposited on appropriate substrates to form four–terminal R-Y-NR network. If the gate of the MOS structures deposited as a strip of resistor film like NiCr, the MOS structure can be analyzed as R-Y-NR network. A method of analysis has been proposed to measure the shunt capacitance and the shunt conductance of certain MOS samples. Extensive literature survey has been conducted to shed some light on this particular topic has indicated a asperity of work actually addressing this issue thus indicating that there is need for further research. Mat lab program has been used to compute shunt capacitance and shunt conductance at different frequencies. The results computed by this method have been compared with the results obtained by LCR meter method and showed perfect coincident with each other.

Key word: Layers of resistive and dielectric · The shunt capacitance · The shunt conductance · Film layers · LCR meter method

INTRODUCTION

In recent years, there have been rapid growing interest and activities in thin film integrated circuits as an approach to microelectronics. Electronic circuits have been fabricated on the basis of replacing conventional lumped elements with their thin film equivalents (distributed elements).

The majority of the up-dated work however has been concerned with the investigation of sandwiched three layer rectangular and exponential shaped structures. In these structures, alternate layers of resistive and dielectric films are deposited on appropriate substrates to form four terminal R-Y-NR networks [1], which is a special type of MOS structure. The electrical characteristics of MOS structures determine the switching speed of VLSI circuits. The electrical characteristics of MOS structures, however, may be estimated using few simple formulas, such;

The gate capacitance: $C_G=C_{ox}WL$

And,

The channel resistance: $R_C=R_s$ (L/W)

where: R_s is the sheet resistance, C_{ox} is the oxide capacitance, L is the channel length and W is the channel width. Unfortunately, MOS is not simple and computing the channel resistance and gate capacitance is rather more complicated. As MOS features size is miniaturizing, the thickness of layers is becoming more significant. The correct extraction of parasitic capacitance and resistance in deep submicron VLSI design is becoming a major research area that is worth exploiting.

In this research, a new method to measure the capacitance and conductance of MOS structures is proposed and investigated. The method of analysis that was used to obtain the steady state ac response and the response to a unit step is rather straightforward. It is shown that the partial differential equation relating voltage, position and time is of second order homogeneous ordinary linear differential equation [2]. If the MOS gate deposited as a strip of resistor film like NiCr, MOS structure can then be analyzed as R-Y-NR network [3].

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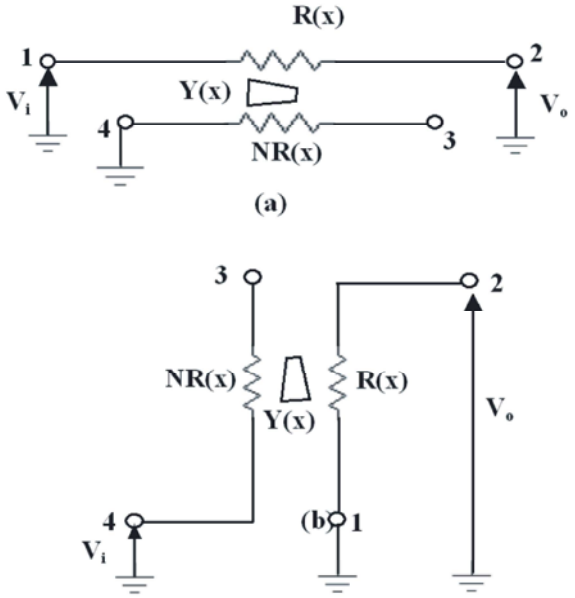

Fig. 1: (a) IOFG (1-Input, 2-Output, 3-Floating, 4-Ground) configuration (b) GOFI (1-Ground, 2-Output, 3-Floating, 4-Input) configuration

Open Circuit Voltage Transfer Function: The matrix parameter functions (MPFs) of a solvable DP R-Y-NR network are defined with the following symbols [2]:

$$r=\begin{vmatrix} M'_0 & F'_0 \\ M'_L & F'_L \end{vmatrix} \quad (1)$$

$$g=(1+N)R_0\begin{vmatrix} M'_0 & F'_0 \\ M'_L & F'_L \end{vmatrix} \quad (2)$$

$$b=(1+N)R_L\begin{vmatrix} M'_0 & F'_0 \\ M_0 & F_0 \end{vmatrix} \quad (3)$$

$$a=(1+N)R_0\begin{vmatrix} M'_L & F_L \\ M_L & F_L \end{vmatrix} \quad (4)$$

$$h=(1+N)R_L\begin{vmatrix} M'_0 & F_0 \\ M_L & F_L \end{vmatrix} \quad (5)$$

$$y=(1+N)^2 R_0 R_L\begin{vmatrix} M_L & F_L \\ M_0 & F_0 \end{vmatrix} \quad (6)$$

Employing the technique of sub network generation [4, 5], the open circuit voltage transfer function (T_{vo}) of the exponential distributed parameter; two-port three Layer sub networks of Fig (1) are obtained in terms of the matrix parameter functions (MPFs). The exponential distributed parameters R-Y-NR structure consists of two

Resistive layers with per unit length (PUL) series resistance given as:

$R = R_o \exp(Kx)$

And $NR=NR_o \exp(Kx)$

For first and second resistive layers respectively. These two resistive layers are separated from each other by an intermediate dielectric layer for which the per unit length (PUL) shunt capacitance is: $C=C_o\exp(-Kx)$ and shunt conductance is: $G=G_o\exp(-Kx)$, where N is a dimensionless constant representing the ratio of the two resistive layers, R_o is a PUL resistive constant, C_o is a PUL capacitive constant, G_o is a PUL conductive constant and K is a PUL exponential taper constant. The open circuit voltage transfer function [4] for the Sub network in Fig. (1a) is:

$$T_{VO}=\frac{V_O}{V_i}=\frac{a+Ng}{(1+N)g} \quad (7)$$

And that for the sub network in Fig. (1b) is:

$$T_{VO}=\frac{v_o}{v_i}=\frac{g-a}{(1+N)g} \quad (8)$$

where g and an are (MPFs) for the exponential distributed parameter (DP) R-Y-NR structure. For structure of length L and ac signal, they are identified as [5, 6]:

$$g=Cosh(mL)+\frac{K}{2}\sinh(mL) \quad (9)$$

$$a=m\exp\left(\frac{KL}{2}\right) \quad (10)$$

$$m=\sqrt{(K/2)^2+(j\omega C_O+G_O)R_O(1+N)}$$

ω= angular frequency = 2ðf

For N=0 which means that the second resistive layer is perfect conductive film, Equations (7) and (8) will respectively be abbreviated to:

$$\frac{V_O}{V_i}=\frac{a}{g} \quad (11)$$

From Fig (1a)

$$\frac{V_o}{V_i}=\frac{g-a}{g}=1-\frac{a}{g} \tag{12}$$

From Fig (1b)

Substituting the matrix parameter functions in the Equations (11) and (12) will respectively give:

$$\frac{V_o}{V_i}=\frac{m\exp\left(\frac{KL}{2}\right)}{mCosh(mL)+\frac{K}{2}Sinh(mL)} \tag{13}$$

From Fig (1a)

$$\frac{V_o}{V_i}=1-\frac{m\exp\left(\frac{KL}{2}\right)}{m\cosh(mL)+\frac{K}{2}\sinh(mL)} \tag{14}$$

From Fig. (1b)

Considering the uniform distributed thin film R-Y-NR network [7, 8]; that means the constant of exponential taper is zero (K = 0) and substituting in the Equations (13) and (14) leads respectively to:

$$\frac{V_o}{V_i}=\frac{m}{mCosh(mL)}=\frac{1}{Cos\,h(mL)}=Sech(mL) \tag{15}$$

From Fig (1a)

$$\frac{V_o}{V_i}=1-Sech(mL) \tag{16}$$

From Fig (1b)

Where m is a complex angle per unit length and

$$m=\sqrt{j\omega C_0 R_0+R_0 G_0} \tag{17}$$

Then the complex angle is mL=m×L and

$$mL=\sqrt{j\omega C_0 R_0 L^2+R_0 G_0 L^2} \tag{18}$$

Let $\frac{V_o}{V_i}=T_{v1}$ for circuit connection in Fig (1a) and $\frac{V_o}{V_i}=T_{v2}$ for that in Fig (1b),

Then: $T_{v1}=Sech\,(mL)$ (19)

And $T_{v2}=1-Sech(mL)$ (20)

Subtracting (20) from (19) and rearranging to give:

$$mL=Sech^{-1}\left(\frac{T_{v1}+1-T_{v2}}{2}\right)$$

And hence:

$$(mL)^2=\left[Sech^{-1}\left(\frac{T_{v1}+1-T_{v2}}{2}\right)\right]^2 \tag{21}$$

From Equation (18):

$$(ML)^2 = j\,\omega\,C_o\,R_o\,L^2 + R_o\,G_o\,L^2 \tag{22}$$

Joining Equations (21) and (22) gives:

$$C = C_O\,L=\frac{\mathrm{Im}\left[Sech^{-1}\left(\frac{T_{v1}+1-T_{v2}}{2}\right)\right]^2}{\omega R_O L} \tag{23}$$

$$G = G_O\,L=\frac{\mathrm{Re}\left[Sech^{-1}\left(\frac{T_{v1}+1-T_{v2}}{2}\right)\right]^2}{R_O L} \tag{24}$$

Experimental Results and Case Study: For the sake of showing the accuracy of the proposed method, shunt capacitance and shunt conductance measurements [9, 10] have been carried out on certain MOS samples. These samples are implemented by depositing a strip of NiCr resistor thin film as a gate contact and then depositing two dot aluminum points at the two ends of the strip for measurement purposes.

At the beginning, the transfer function of the device has been measured for both configurations shown in Fig (1). Response of transfer function magnitude and its phase with respect to frequency have been plotted as shown in Fig (2) and Fig (3) respectively; for positive gate biasing.

Figure (2) above and Fig (4) below, show that the configuration shown in fig (1a) acts as a high pass filter. While the configuration in fig (1b) acts as a low pas filter. It also proves that the sample is an RC network and the reduction in the transfer function is increased as the applied voltage is increased. However, for negative biasing, the transfer function magnitude and phase responses have been plotted as shown in Fig (4) and Fig (5) respectively.

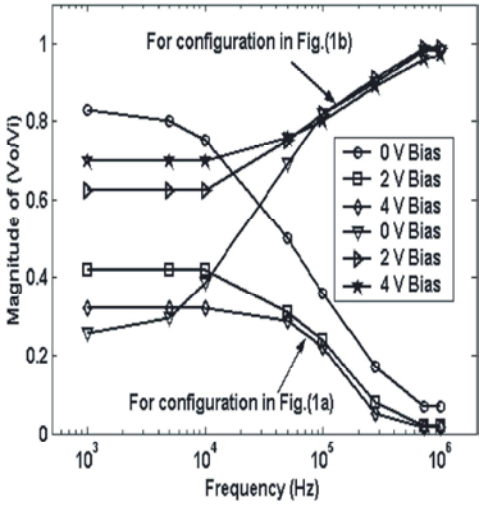

Fig. 2: Transfer function magnitude frequency response of a strip gate MOS device for different positive biases

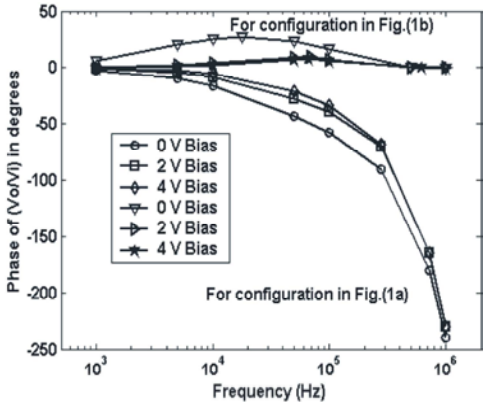

Fig. 3: Transfer function phase frequency response of a strip gate MOS device for different positive biases

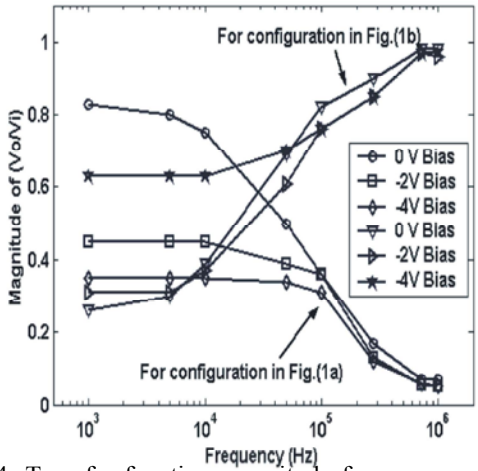

Fig. 4: Transfer function magnitude frequency response of a strip gate MOS device for different nagative biases

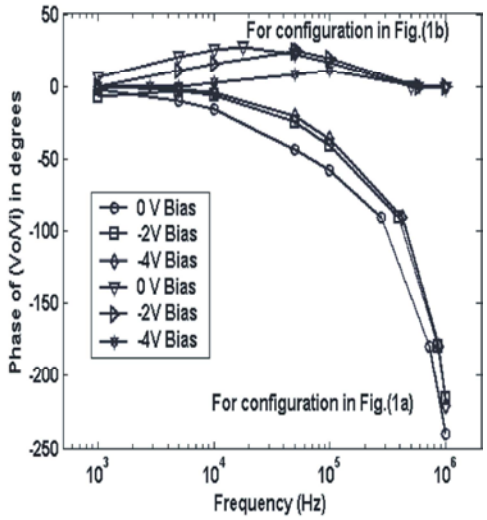

Fig. 5: Transfer function phase frequency response of a strip gate MOS device for different nagative biases

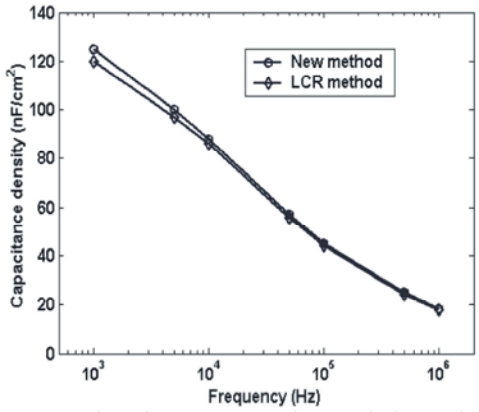

Fig. 6: Comparison between capacitance dedetermined by the two methods for zero bais

Fig (3) and Fig (5) above represent the response of the transfer function phase of the device for positive and negative biasing voltage, respectively. It is clear that the phase is increased rapidly as the frequency increased for both voltages of configuration depicted in fig (1a). While the phase is nearly constant for the configuration shown in Fig (1b). These results were expected because the output was taken across the capacitor in fig (1a), while it was taken across the resistance in the second configuration.

Mat lab program has been designed and implemented to simulate the performance and the computational results of the simulation analysis have been computed for shunt capacitance and shunt conductance for strip gate MOS structure at different frequencies. Therefore, for a zero bias, shunt capacitance and shunt conductance of the

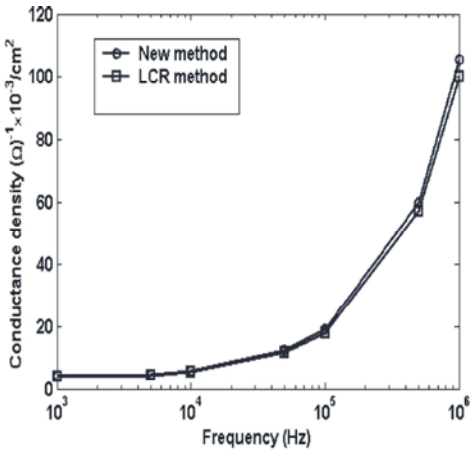

Fig. 7: Comparison between leakage conductance dedetermined by the two methods for zero bais

MOS structure at different frequencies have been investigated. The computed results as well as the results obtained using LCR meter method [6, 11] have been plotted and compared, as depicted in Fig (6) and in Fig (7).

It is apparent from the above figures that the results obtained from the two methods do coincided with each other totally, indicating that the proposed computerized method carry the same degree of accuracy as the old practical method.

CONCLUSION

In this research the high frequency C-V and G-V device measurements were fulfilled using MOS structure as a thin film distributed R-Y-NR structure with four terminal two port network. Therefore, practically it can be concluded that, low frequency range is used for measuring the capacitance. However, high frequency is used for measuring the conductance. This very tiny difference could be due to the stray inductor and stray capacitance of the connecting wires used in the experiment. This conclusion encourages using the proposed method as a tool for C-V and G-V plots at any frequency.

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