Middle-East Journal of Scientific Research 20 (4): 432-435, 2014
ISSN 1990-9233

DOI: 10.5829/idosi.mejsr.2014.20.04.11325

# Advertising System Using Vga Protocol

*M. Surumbar Khuzhali*

M. Tech-VLSI Design,
Bharath University, Chennai, India

**Abstract:** In the recent years, the public advertising techniques takes important role in marketing of products to people. But most of the public advertising are following the showing the advertisement posters with or without lighting in the public places like rail stations, bus terminals and airports. The proposed system gives the better solution of advertising using the FPGA and SD card media. In SD card we can store the advertisement images in JPEG or BMP picture format. In FPGA based system, read the content of the SD card image format and convert it into VGA protocol to display in the any of the VGA screens. This VGA data can drive any size / any number of the TFT monitors or LCD screens. Also the pictures will changes in pre defined or programmable timings and animation of the pictures is possible while showing the screens. The storage capacity of a SD card is so high, since possible display entire product range. The SD card is easy to store the pictures using a PC.

**Key words:** While showing the screens · Display entire product range · Defined or programmable · The showing the advertisement posters

## INTRODUCTION

Modern advertising methods incorporate target advertising and interactive advertising more than traditional advertising methods do. But when many people think of modern advertising methods, they usually think of advertising techniques that use more technology like online advertising and mobile phone advertising. These modern advertising methods include many cheap and low cost advertising methods. Today more small business owners track advertising spending and advertising revenue. [1] The present advertisements are showing offline method like flex screens, rolling banners and tri-stand displays etc… But these are most common and can show fixed image or static data only. If an advertiser wants to show more number of his products image mean, its not possible for present static methods.With this in mind, this project shows that the advanced advertising method which will be useful for the railway station pavements, bus terminus and airport corridors. Presently in such areas are engaged by a big size flex banners with/without front/back lighting screens, some trivision displays or LCD monitors are showing the moving advertising video etc…[2].

**SD Card Interface with FPGA:** Secure Digital (SD) cards are removable ash-based storage devices that are gaining in popularity in small consumer devices such as digital cameras, PDAs and portable music devices. Their small size, relative simplicity, low power consumption and low cost make them an ideal solution for many applications.

**SD Card Standard:** The SD card standard is a standard for removable memory storage designed and licensed by the SD Card Association. The SD Card standard is largely a collaborative eort by three manufacturers, Toshiba, SanDisk and MEI and grew out of an older standard, Multi Media Card (MMC). The card form factor, electrical interface and protocol are all part of the SD Card specification. The SD standard is not limited to removable memory storage devices and has been adapted to many different classes of devices, including 802.11 cards, Bluetooth devices and modems [3].

**Comparison with Other Technologies:** SD is one of many different types of removable memory storage devices. Among the other competing standards are CF, CF+, Sony Memory Stick and USB. These devices all perform similar functions, but differ widely in form factors, complexity and power consumption. SD Cards measure only 32x24 mm [4].

**Corresponding Author:** M. Surumbar Khuzhali, M. Tech-VLSI Design, Bharath University, Chennai, India.

This is very small compared to most competing technologies, but is both an advantage and a disadvantage, since the small size and weight requirements cannot accommodate microdrives.

However, if size is a significantcant design consideration, SD is an ideal choice. The SD Card electrical interface is relatively simple, requiring at most only 6 wires for communications, while still supporting data rates in the Mbps range. Compared to USB and CF/CF+, the SD physical interface is very simple, a strong consideration if interface complexity is a concern. SD Cards typically draw no more than 100 mA of current while active, generally less than that drawn by CF or USB devices. [3] If power consumption is important, SD again is a good choice [4].

**Send the Picture Info to the Frame Buffer Using Sdram:** The SDRAM stores the data being transferred to VGA and from the SD card. This task is achieved by the Image loader program which is written in the application. Accessing the bitmap files locations and sends to the Video frame buffer through the SDRAM [5].

**Sdram (Synchronous Dynamic Random Access Memory):** Synchronous dynamic random access memory (SDRAM) is dynamic random access memory (DRAM) that is synchronized with the system bus. Classic DRAM has an asynchronous interface, which means that it responds as quickly as possible to changes in control inputs. SDRAM has a synchronous interface, meaning that it waits for a clock signal before responding to control inputs and is therefore synchronized with the computer's system bus. The clock is used to drive an internal finite state machine that pipelines incoming instructions. This allows the chip to have a more complex pattern of operation than an asynchronous DRAM, enabling higher speeds.

Pipelining means that the chip can accept a new instruction before it has finished processing the previous one. In a pipelined write, the write command can be immediately followed by another instruction without waiting for the data to be written to the memory array. In a pipelined read, the requested data appears after a fixed number of clock pulses after the read instruction, cycles during which additional instructions can be sent. (This delay is called the latency).

**Sdram Control Signals:** All commands are timed relative to the rising edge of a clock signal. In addition to the clock, there are 6 control signals, mostly active low, which are sampled on the rising edge of the clock:

**Cke Clock Enable:** When this signal is low, the chip behaves as if the clock has stopped. No commands are interpreted and command latency times do not elapse. The state of other control lines is not relevant. The effect of this signal is actually delayed by one clock cycle. That is, the current clock cycle proceeds as usual, but the following clock cycle is ignored, except for testing the CKE input again. Normal operations resume on the rising edge of the clock after the one where CKE is sampled high.

- Put another way, all other chip operations are timed relative to the rising edge of a masked clock. The masked clock is the logical AND of the input clock and the state of the CKE signal during the previous rising edge of the input clock.

**/CS Chip Select:** When this signal is high, the chip ignores all other inputs (except for CKE) and acts as if a NOP command is received.

**Dqm Data Mask:** (The letter Q appears because, following digital logic conventions, the data lines are known as "DQ" lines.) When high, these signals suppress data I/O. When accompanying write data, the data is not actually written to the DRAM. When asserted high two cycles before a read cycle, the read data is not output from the chip. There is one DQM line per 8 bits on a x16 memory chip or DIMM.

**Ras Row Address Strobe:** Despite the name, this is not a strobe, but rather simply a command bit. Along with /CAS and /WE, this selects one of 8 commands.

**Cas Column Address Strobe:** Despite the name, this is not a strobe, but rather simply a command bit. Along with /RAS and /WE, this selects one of 8 commands.

**We Write Enable:** Along with /RAS and /CAS, this selects one of 8 commands. This generally distinguishes read-like commands from write-like commands.

SDRAM devices are internally divided into 2 or 4 independent internal data banks. One or two bank address inputs (BA0 and BA1) select which bank a command is directed toward [6-9].

Many commands also use an address presented on the address input pins. Some commands, which either do not use an address, or present a column address, also use A10 to select variants.

**VGA Interface (Video Frame Controller):**

- The output device of the system will be the VGA screen.
- Uses a 4-bit resistor-network DAC
- With 15-pin high-density D-sub connector
- Supports up to 640x480 at 60-Hz refresh rate
- Image data stream from the SRAM sends towards the VGA. (video frame controller core).

**Introduction:** The Video Graphics Array (VGA) interface is common to most modern computerdisplays and is based on a pixel map, color planes and horizontal and vertical sync signals. A VGA monitor has three color signals (red, green and blue) that set one of these colors on or off on the screen. The intensity of each of those colors sets the final color seen on the display. For example, if the red was fully on, but the blue and green off, then the color would be seen as a strong red. Each analog intensity is defined by a two bit digital word for each color (e.g. red 0 and red l) that are connected to a simple digital to analog converter to obtain the correct output signal.

The resolution of the screen can vary from 480 × 320 up to much larger screens, but a standard default size is 640 - 480 pixels. This is 480 lines of 640 pixels in each line, so the aspect ratio is 640/480 leading to the classic landscape layout of a conventional monitor screen.

The VGA image is controlled by two signals-horizontal sync and vertical sync. The horizontal sync marks the start and finish of a line of pixels with a negative pulse in each case. The actual image data is sent in a 25.17 µs window in a 31.77 µs space between the sync pulses. (The time that image data is not sent is where the image is defined as a blank space and the image is dark.) The vertical sync is similar to the horizontal sync except that, in this case, the negative pulse marks the start and finish of each frame as a whole and the time for the frame (image as a whole) takes place in a 15.25 ms window in the space between pulses, which is 16.784 ms.

There are some constraints with regard to the spacing of the data between pulses that will be considered later in this chapter, but it is clear that the key to a correct VGA output is the accurate definition of timing and data by the VHDL.

**Basic Pixel Timing:** If there is a space of 25.17 µs to handle all of the required pixels, then some basic calculations needs to be carried out to make sure that the Field Programmable Gate Array (FPGA) can display the correct data in the time available. For example, if we have a 640 × 480 VGA system, then that means that 640 pixels must be sent to the monitor in 25.17 µs. A simple calculation shows that for each pixel we need 25.17 µs/640 = 39.328 ns per pixel. If our clock frequency is 100 MHz on the FPGA, then that gives a minimum clockperiod of 10 ns, which can be achieved using a relatively standard FPGA.

**Image Handling:** Clearly it is not sensible to use an integrated image system on the FPGA, but rather it makes much more sense to store the image in memory (Random Access Memory (RAM)) and retrieve it frame by frame. Therefore, as well as the basic VGA interface it makes a lot of sense for the images to be moved around in memory and therefore using the same basic RAM interface as defined previously is sensible. Thus, as well as the VGA interface pins, our VGA handler should include a RAM interface.

## CONCLUSION

This product consumes less power compared with other method of advertising. The synthesizer and hardware tools are easy to learn and coding can be modified according to the image size. Since VGA screen supports the mentioned tools in an appreciable manner, different application requirements can be accomplished by this product.

With the advancement in VLSI techniques, the product size can be highly reduced (SD card measures only 32*24mm). The hardware for expanding the memory size can be included in the future for showing videos and loading maximum number of images.

Current displays like LCD, TFT, Plasma support VGA protocol. The upgradation of display techniques also require the same protocol. Thus this product serves effectively for the society at present and in future also.

## REFERENCES

1. An Evaluation of the Suitability of FPGAs for Embedded Vision Systems: W. James MacLean, Department of Electrical & Computer Engineering, University of Toronto, Toronto, Ontario, M5S 1A1.
2. VSIA homepage. Online: http://www.vsia.org.
3. Field-Programmable Gate Arrays: Steve Brown, R. Francis, Jonathan Rose and Zvonko Vranesic.. Kluwer Academic Publishers, May 1992.

4. Preliminary Testing Tool for VGA Monitor Using FPGA XC4005XL and XS-Board, Indar Sugiarto, Department of Electrical Engineering- Petra Christian University.
5. Human-Machine Interface Based on FPGA and VGA Monitor: J.L. Russi Federal, University of Pampa, Alegrete Campus, Brazil.
6. Ahmed, Naseer, 2013. Ultrasonically Assisted Turning: Effects on Surface Roughness World Applied Sciences Journal, 27(2): 201-206.
7. Tatyana Nikolayevna Vitsenets, 2014 Concept and Forming Factors of Migration Processes Middle-East Journal of Scientific Research, 19(5): 620-624.
8. Shafaq Sherazi and Habib Ahmad, 2014. Volatility of Stock Market and Capital Flow Middle-East Journal of Scientific Research, 19(5): 688-692.
9. Kishwar Sultana, Najm ul Hassan Khan and Khadija Shahid, 2013. Efficient Solvent Free Synthesis and X Ray Crystal Structure of Some Cyclic Moieties Containing N-Aryl Imide and Amide,Middle-East Journal of Scientific Research, 18(4): 438-443.