Implementation of Improved Z-Source Inverter with Reduced Z-Source Capacitor Voltage Stress and Soft-Start Capability

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Abstract: This paper proposes an improved Z-source inverter topology. Compared to the traditional Z-source inverter, it can reduce the Z-source capacitor voltage stress significantly to perform the same voltage boost and has inherent limitation to inrush current at startup. The control strategy of the proposed Z-source inverter is exactly the same as the traditional one, so all the existing control strategy can be used directly. A soft-start strategy is also proposed to suppress the inrush surge and the resonance of Z-source capacitors and inductors. The operation principle of the proposed topology and comparison with the traditional topology are analyzed in detail. Simulation and experimental results are given to demonstrate the new features of the improved topology.

Key words: Z-source capacitor voltage · Existing control strategy · Proposed topology

INTRODUCTION

The voltage-source inverter and current-source inverter are two types of traditional power inverter topology. For the voltage-source inverter fed from a voltage source, the ac output voltage is lower than the available dc bus voltage; thus, it can only perform the buck dc–ac power conversion. For the current source inverter fed from a current source, the ac output voltage, however, is greater than the dc source voltage, thus presenting a voltage boost dc–ac power conversion. In applications where both voltage buck and boost are required, an additional dc–dc converter is needed in both voltage-source and current-source inverters, which increases the system complexity and cost to a significant extent.

A Z-source inverter is proposed as the single-stage inverter topology to demonstrate both buck and boost power conversion ability. In addition, the two switches in the same phase leg can be gated on simultaneously and no dead time is needed, so the output distortion is greatly reduced and the reliability can be improved. Recent research on Z-source inverters mainly focuses on the modulation strategy, the modeling and controller design, the application fields and other derived Z-source converter topologies. Despite the aforementioned merits, the traditional Z-source inverter topology also shows the

following drawbacks: 1) the voltage across Z-source capacitors is no less than input voltage, thus high-voltage capacitors should be used, which may result in larger volume and prove to be cost expensive to the system; 2) it cannot suppress the inrush current and the resonance introduced by Z-source capacitors and inductors at startup, thus causing the voltage and current surge, which, in turn, may destroy the devices.

To solve the aforesaid drawbacks in traditional Z-source inverter, a new Z-source inverter topology is presented with reduced Z-source capacitor voltage stress and inherent inrush current limitation at startup. It can suppress the resonance well by adopting a proper soft-start strategy. The operation principle and comparison with the traditional topology reveal the merits of the proposed topology and are also verified in both Saber simulation and experiment.

Considerations on Z-source Inverter: The Z-source inverter topology where a unique impedance network is introduced to couple the inverter main circuit to the power source. The two-port impedance network consists of two identical inductors $L1$ and $L2$ and two identical capacitors $C1$ and $C2$ connected in X shape. The Z-source inverter has an additional shoot-through zero state, which is forbidden in voltage-source inverter. When the input voltage is high enough to produce the desired output

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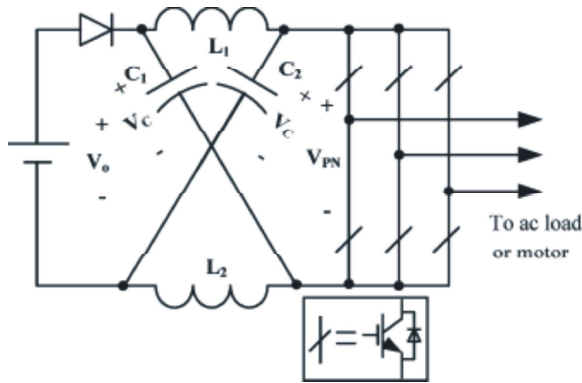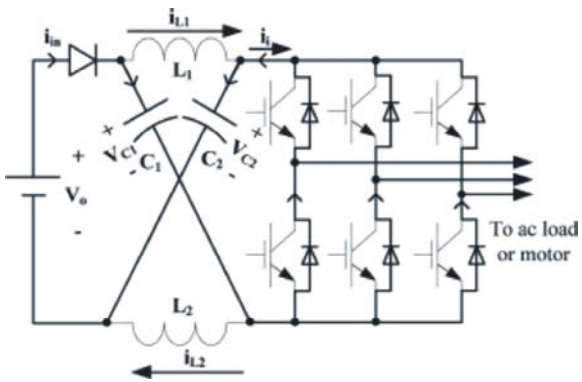
Fig. 1: Z-source inverter.

Fig. 2: Inrush current at startup.

voltage, the shoot-through zero state is not used and the Z-source inverter performs the buck conversion the same way as the voltage-source inverter. When the input voltage is low, the shoot-through zero state is used to boost the voltage; therefore, the Z-source inverter performs as a buck–boost inverter.

A. Z-Source Capacitor Voltage Stress

As described by Peng [1], the peak dc-link voltage canbe expressed as

$$\hat{V}_{PN} = BV_o = \frac{1}{1-2D_0}V_0$$

where Vo is the input dc voltage and B is the boost factor; B is determined by the shoot-through duty ratio $D0$. The Z-sourcecapacitor voltage is determined by.

$$V_{C1} = V_{C2} = V_C \frac{1-D_0}{1-2D_0}V_0.$$

As can be derived from (2), VC is no less than Vo, thus presenting a high Z-source capacitor voltage stress.
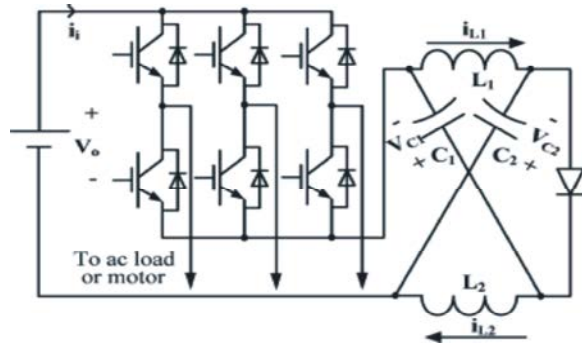
$vL1 = vL2 = vL$, $VC1 = VC2 = VC$.

Fig. 3: Improved Z-source inverter.

Inrush Current at Startup: Huge inrush current exists at Z-source inverter startup. The initial voltage across the Z-source capacitors is zero, so the current path can be seen in Fig. 2 and huge inrush current charges the capacitors immediately to $0.5Vo$. Then, the resonance of Z source capacitors and inductors starts, which results in large voltage and current surge. Because of the inherent current path at startup in this topology, it cannot achieve the soft-start capability.

Improved Z-source Inverter: The improved Z-source inverter is shown in Fig. 3. The elements used are exactly the same as the previous one. The difference is that the positions of the inverter bridge and diode are exchanged and their connection directions are inversed. The voltage polarity of Z-source capacitors in the proposed topology remains the same as the input voltage polarity; therefore, to get the same voltage boost, the capacitor voltage stress can be reduced to a significant extent. In addition, as can be seen from Fig. 3, the topology has inherent inrush-current limitation ability compared to the previous one, because there is no current path at startup.

Operation Principle and Comparison with Previous Topology: The equivalent circuit of the improved Z-source inverter is shown in Fig. 4. Assuming that $L1 = L2 = L$, $C1 = C2 = C$, then we have

When in the shoot-through state, the inverter side is shorted, as shown in Fig. 4(a), we can get

$$vL = Vo + VC. \tag{4}$$

When in the non-shoot-through state (including the active and null states), the inverter side can be simplified by an equivalent current source (the current value is zero when in null state), as shown in Fig. 4(b). The following equation can be derived in this state:
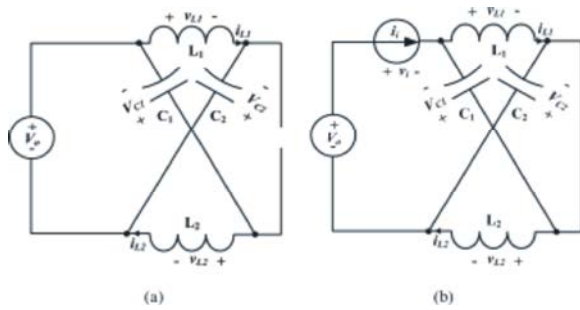
Fig. 4: Equivalent circuit of improved Z-source inverter. (a) Shoot-through state. (b) Non-shoot-through state.
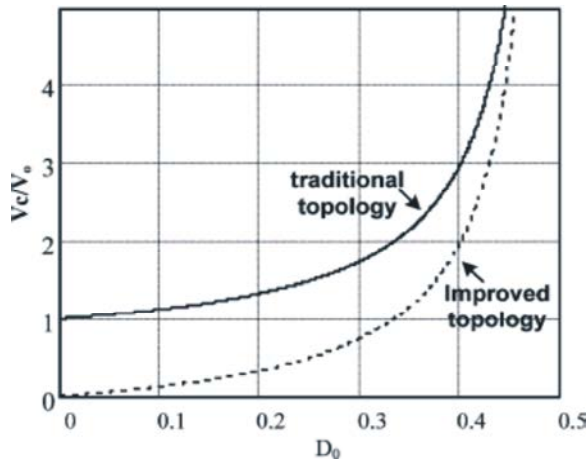

Fig. 5: VC/Vo versus $D0$ of the two topologies.

$$vL = -VC \qquad (5)$$

The shoot-through duty ratio is $D0$ and the average value of vL over one switching period is zero, so we can get

$$V_C - \frac{D_0}{1-2D_0}V_o. $$

From this derivation, we can see that in the improved topology, when the shoot-through duty ratio $D0$ is zero, the Z-source capacitor voltage VC is equal to zero. When the converter is in the soft-starting state, VC is zero naturally, so if we control the $D0$ increase from zero gradually, VC can also increase from zero gradually and soft start can be achieved. But this is not the case in traditional topology.

The peak dc-link voltage across the inverter phase legs and peak output phase voltage can be expressed as

$$\hat{V}_{PN} = V_o + 2V_C = \frac{1}{1-2D}V_o = BV_o \qquad (7)$$

$$\hat{V}_P = M\frac{\hat{V}_i}{2} = MB\frac{V_o}{2}. \qquad (8)$$

where B is the boost factor determined by $D0$ and M is the modulation ratio. As can be seen from (8), the output voltage is boosted by a factor B ($B \geq 1$), which is the same as the traditional topology. All the power switches and diodes used in improved and traditional topologies are exactly the same. A comparison is given on the Z-source capacitor, Z-source inductor and input current ripple.

A. Z-Source Capacitor Voltage Stress and Voltage Ripple The peak dc-link voltage of the two topologies is exactly the same, as can be seen from (1) and (7). Comparing (6) with (2), one can see that the Z-source capacitor voltage decreases by Vo while maintaining the same voltage boost. The comparison of VC in the two topologies is shown in Fig. 5. Aswe already know, the Z-source inverter is suitable in applications where the input voltage varies in a wide range, such as the fuel cell and photovoltaic power conditioning systems. Consider, for example, the input voltage is 150–300V. In traditional topology, the capacitor voltage stress is decided by the maximum input voltage, so VC is no less than 300V. However, in the improved topology, VC is decided by the minimum input voltage to achieve the maximum voltage boost, the capacitor voltage stress is only 75V to get the required voltage boost under 150V input voltage; thus, low-voltage capacitors can be used [2-6].

During shoot-through time, the condition for previous and improved Z-source inverters is the same, the Z-source inductor current discharges the capacitors; therefore, the voltage ripple across the capacitors in both inverters can be expressed as

$$\Delta V_C = \frac{I_L D_0 T}{C} \qquad (9)$$

where IL is the average inductor current and T is the switching period of the Z-source network.

Z-Source Inductor Current Ripple: The average Z-source inductor current equals the average input current; therefore, the average Z-source inductor current in both topologies is the same. For improved topology during the nonshoot-through state, as shown in Fig. 4(b), the Z-source inductor current decreases and the current ripple can be expressed as

$$\Delta i_L = \frac{(1-D_0)TV_C}{L} = \frac{D_0(1-D_0)TV_o}{(1-2D_0)L}. \qquad (10)$$
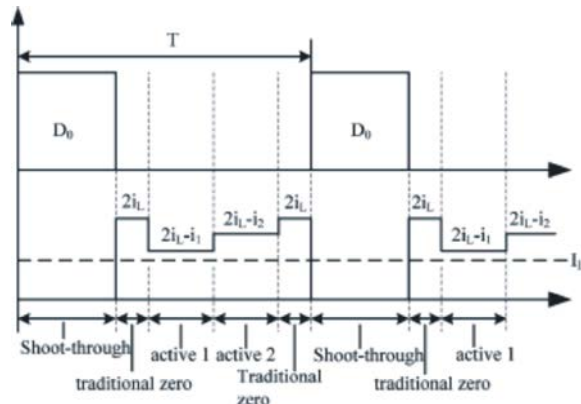
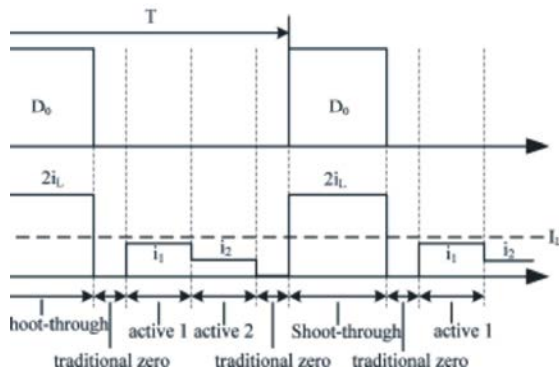Fig. 6: Input current of the traditional Z-source inverter.

Fig. 7: Input current of the improved Z-source inverter.

For the previous topology, however, during the shoot-through state, the Z-source inductor current increases and the current ripple can be expressed as

$$\Delta i_L = \frac{D_0 T V_C}{L} = \frac{D_0(1-D_0)TV_o}{(1-2D_0)L}. \tag{11}$$

From (10) and (11), we can see that the current ripple is the same in these two topologies.

Input Current Ripple: The input current for a Z-source inverter is different under different controls and the following analysis will take the simple boost control as an example. For traditional Z-source inverters, the current to the inverter bridge is ii, so the input current can be expressed as

$$iin = 2iL - ii \tag{12}$$

In shoot-through state, the input current is zero; in traditional zero-state, ii is zero, so iin is $2iL$; in active states 1 and 2, ii is $i1$ and $i2$, respectively, so iin is $2iL - i1$

and $2iL - i2$, respectively and the average input current is IL. Ignoring the inductor current ripple, iL can be represented as IL. The input current for traditional topology is shown in detail in Fig. 6. The deviation of input current and its average value can be expressed as

$$\Delta iin = |iin - IL| = |2IL - ii - IL| = |IL - ii| \tag{13}$$

For improved topology, the input current is actually the current fed to the inverter bridge, so in shoot-through state, the input current is $2iL$; in traditional zero state, the input current is zero; in active states 1 and 2, the input current is $i1$ and $i2$, respectively and the averaged input current is IL. The input current for improved topology is shown in detail in Fig. 7. The deviation of input current and its average value can be expressed as

$$\Delta iin = |iin - IL| = |ii - IL| \tag{14}$$

From (13) and (14), we can see that the input current ripple of these two topologies is exactly the same.

Simulation Results: The Saber simulation results are given to verify the merits of the proposed Z-source inverter and compare with the tradition alone in a stand-alone system. Simple boost control is applied as an example. The simulation parameters are:

- *Z-source network*: $L1 = L2 = 1000\,\mu H$, $C1 = C2 = 2000\,\mu F$;
- *Output filters*: $Lf = 1000\,\mu H$, $Cf = 15\mu F$;
- switching frequency: 20 kHz;
- *load*: three-phase resistance load $R = 13\,\Omega/phase$.

Three cases are given under different input voltages, shoot through duty ratios and modulation ratios, while the output phase voltage is 115V in all the cases.

Case 1: $Vo = 210V$, $D0 = 0.218$, $M = 0.9$ with 1/6 third harmonic injection. Fig. 8(a) and (b) shows the simulation results of traditional topology and improved topology, respectively.

The waveforms from top to bottom are input current iin, Z-source capacitor voltage VC, dc-link voltage VPN, Z-source inductor current IL and output phase voltage $vload$, respectively.

From Fig. 8(a), we can see that in traditional topology, VC is boosted to 288V in steady state, VPN is boosted to 368V and huge inrush current occurs at startup. VC is charged from 0 to 105V instantaneously. Then, the
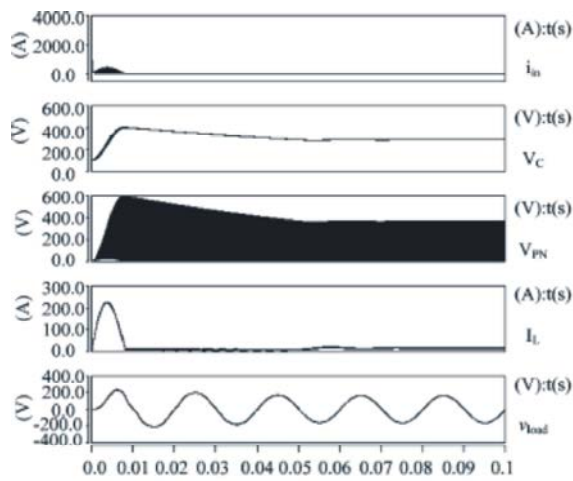
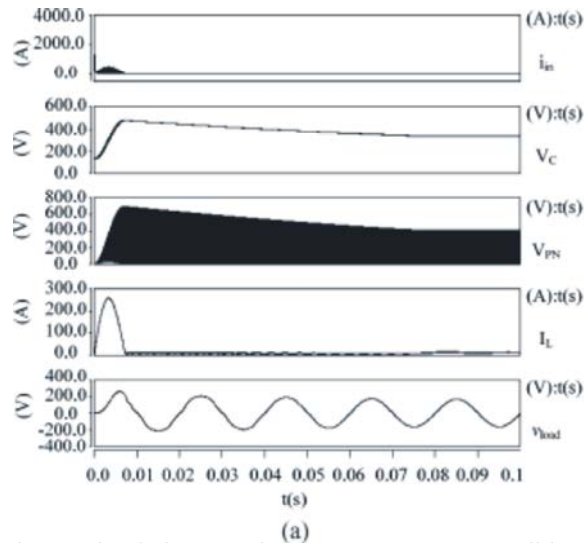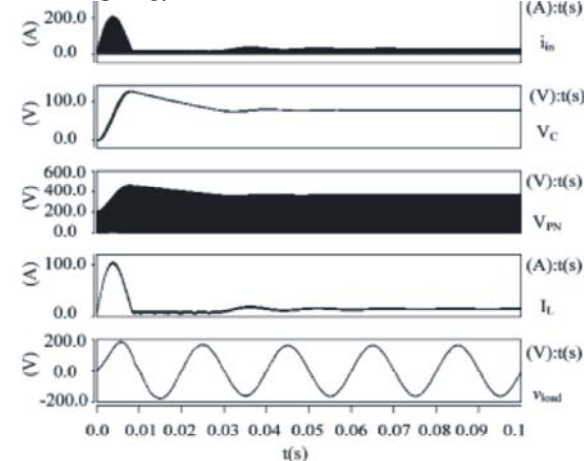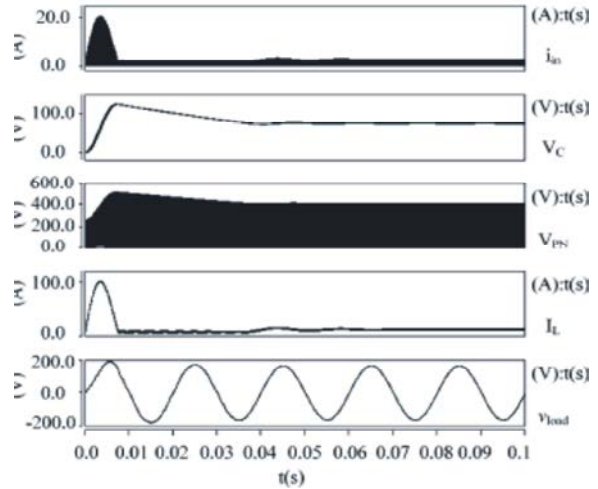Fig. 8: Simulation results in case 1. (a) Traditional topology

(b) Improved topology.

Fig. 9: Simulation results in case 2. (a) Traditional topology

(b) Improved topology.

resonance of Z-source capacitors and inductors starts and voltage surge and current surge may destroy the converter.

From Fig. 8(b), we can see that in improved topology, *VC* is equal to 78V in steady state, *VPN* is boosted to 368V and the inrush current and the resonance also exist though they are much smaller than the previous one [7-13].

Case 2: *Vo* = 260V, *D0* = 0.187, *M* =0.813 without third harmonic injection. Fig. 9(a) and (b) shows the simulation results of traditional topology and improved topology, respectively.

In Fig. 9(a), we can see that in traditional topology, *VC* is boosted to 335V in steady state, *VPN* is boosted to 413V and huge inrush current occurs at startup. *VC* is charged from 0 to 130V instantaneously and the voltage surge and current surge may also destroy the converter.

In Fig. 9(b), we can see that in improved topology, *VC* is equal to 75V in steady state, *VPN* is boosted to 413V and the inrush current and the voltage and current surge also exist though smaller than the previous one.

Case 3: *Vo* = 320V, *D0* = 0, *M* = 1.05 with 1/6 third harmonic injection. Fig. 10(a) and (b) shows the simulation results of traditional and improved topology, respectively.

In Fig. 10(a), we can see that in traditional topology, *VC* and *VPN* are equal to *Vo* in steady state and huge inrush current occurs at startup. *VC* is charged from 0 to 160V instantaneously and the voltage surge and current surge can also be seen.

In Fig. 10(b), we can see that in improved topology, *VC* is about 0V and *VPN* is equal to *Vo* in steady state, the inrush current and the resonance are well suppressed; therefore, the new topology is more reliable. Noting that
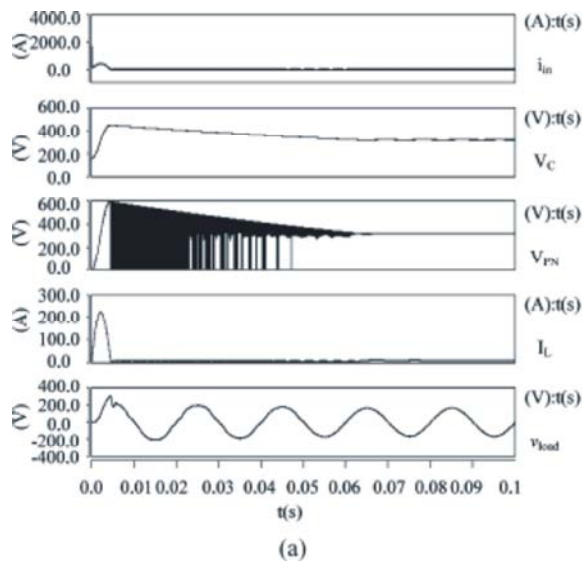
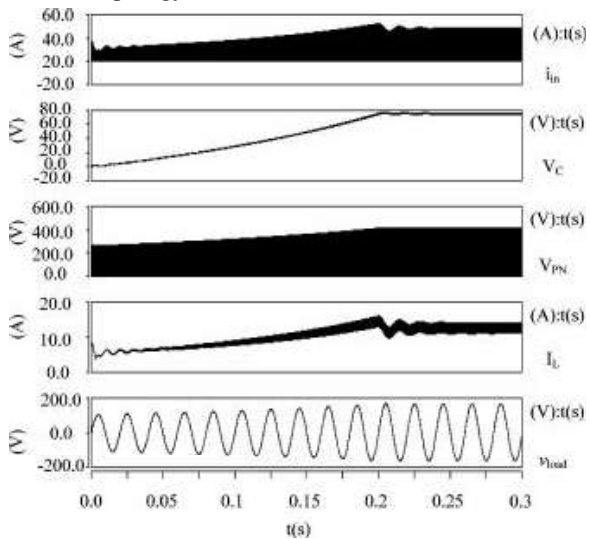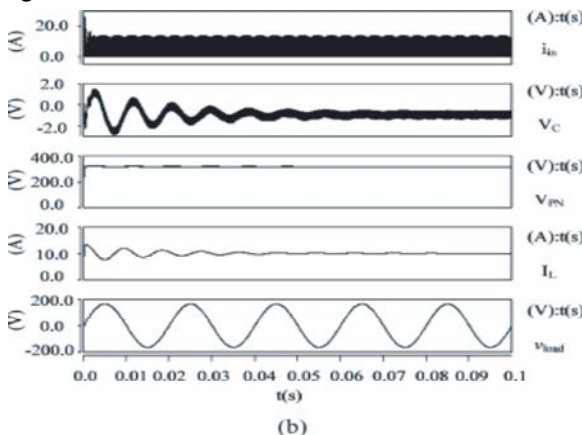Fig. 10: Simulation results in case 3. (a) Traditional topology.

Fig. 11: Soft-start waveforms in case 2.

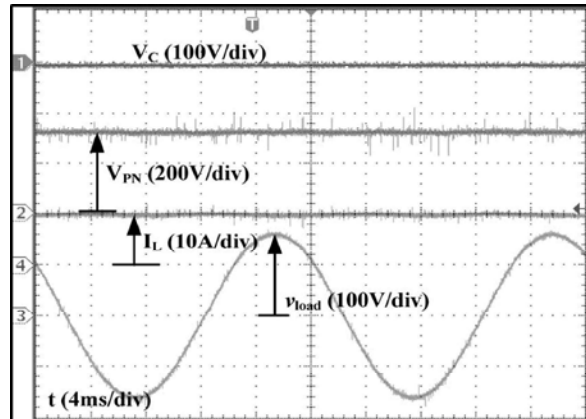
(b) Improved topology

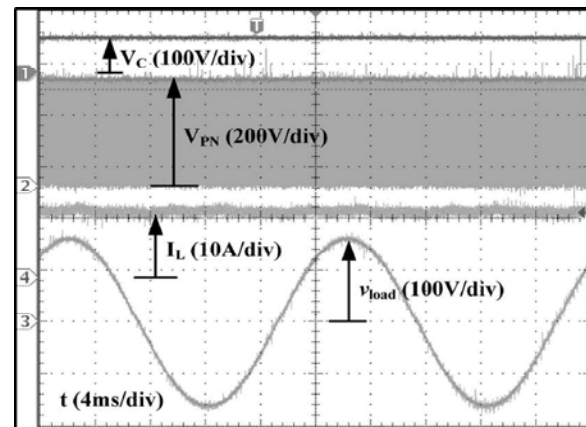Fig. 12: Experimental results in case 1.

Fig. 13: Experimental results in case 2.

there is a small negative offset across the Z-source capacitor mainly caused by the forward voltage drop of the diode, a film capacitor is more reasonable in practical use to suffer the high current ripple in the Z-source network; therefore, this negative offset is not a problem.

To avoid the resonance in improved topology, a soft-start strategy is also given here, i.e., increase $D0$ from 0 gradually at startup. Fig. 11 shows the waveforms of improved topology with a soft-start strategy in case 2. $D0$ increases from 0 to 0.187 in 200 ms and we can see that the inrush current and resonance are suppressed without voltage and current surge.

Experimental Verification: The parameters used in the experiment are the same as insimulation (several electrolytic capacitors are connected in parallel to suffer the high current ripple in the experiment; in fact, the film capacitors are preferred here). Fig. 12 shows the experimental results in case 1; VC is about 80V, VPN is boosted to 370V and the output phase voltage is 115V. Fig. 13 shows the experimental results in case 2; VC is less
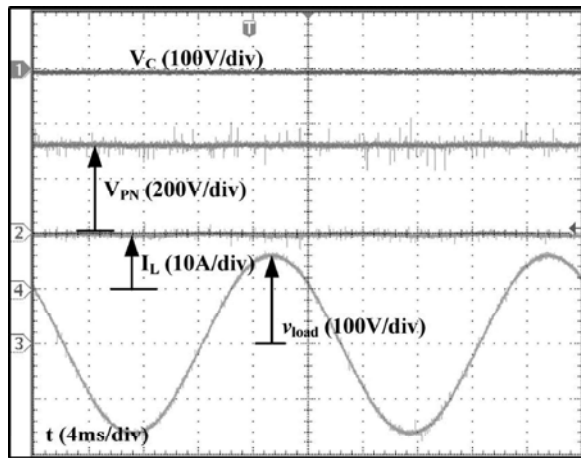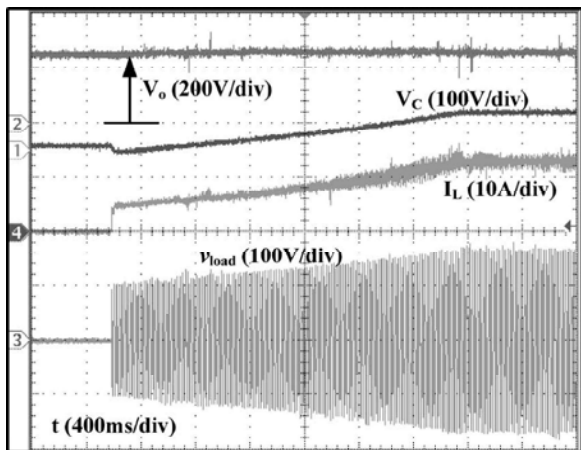
Fig. 14: Experimental results in case 3.

Fig. 15: Soft-start waveforms in case 2.

than 80V, *VPN* is boosted to 415V and the output phase voltage is 115V. Fig. 14 shows the experimental results in case 3; *VC* is 0V and *VPN* is equal to *Vo* and the output phase voltage is 115V. Fig. 15 shows the soft-start waveforms in case 2. Here, the Z-source capacitor voltage and inductor current increase slowly and no surge or resonance exists. The experimental results coincide well with the simulation results.

CONCLUSION

This paper has presented a new Z-source inverter topology. Compared to the previous Z-source inverter, the improved topology has several merits.

- The Z-source capacitor voltage stress is reduced greatly to perform the same boost ability; thus, low-voltage capacitors can be utilized to reduce the system cost and volume;

- The inrush current and resonance of Z-source capacitors and inductors in traditional topology can be suppressed with a proper soft-start strategy. Simulation and experimental results verified the aforesaid merits of the proposed topology.

REFERENCES

1. Peng, F.Z., 2003. Z-source inverter, IEEE Trans. Ind. Appl., 39(2): 504-510.
2. Tran, Q., T. Chun, J. Ahn and H. Lee, 2007. Algorithms for controlling both the DC boost and AC output voltage of Z-source inverter, IEEE Trans. Ind. Electron., 54(5): 2745-2750.
3. Peng, F.Z., M. Shen and Z. Qian, 2005. Maximum boost control of the Z-source inverter, IEEE Trans. Power Electron., 20(4): 833-838.
4. Shen, M., J. Wang, A. Joseph, F.Z. Peng, L.M. Tolbert and D.J. Adams, 2006. Constant Boost control of the Z-source inverter to minimize current ripple and voltage stress, IEEE Trans. Ind. Appl., 42(3): 770-777.
5. Loh, P.C., D.M. Vilathgamuwa, Y.S. Lai, G.T. Chua and Y. Li, 2005. Pulsewidth modulation of Z-source inverters, IEEE Trans. Power Electron., 20(6): 1346-1355.
6. Peng, F.Z., A. Joseph, J. Wang, M. Shen, L. Chen, Z. Pan, E.O. Rivera and Y. Huang, 2005. Z-source inverter for motor drives, IEEE Trans. Power Electron., 20(4): 857-863.
7. Peng, F.Z., M. Shen and K. Holland, 2007. Application of Z-source inverter for traction drive of fuel cell-battery hybrid electric vehicles, IEEE Trans. Power Electron., 22(3): 1054-1061.
8. Huang, Y., M. Shen, F.Z. Peng and J. Wang, 2006. Z-source inverter for residential photovoltaic systems, IEEE Trans. Power Electron., 21(6): 1776-1782.
9. Loh, P.C., D.M. Vilathgamuwa, G.J. Gajanayake, Y.R. Lim and C.W. Teo, 2007. Transientmodeling and analysis of pulse-width modulated Z-source inverter, IEEE Trans. Power Electron., 22(2): 498-507.
10. Liu, J.B., J.G. Hu and L.Y. Xu, 2007. Dynamic modeling and analysis of Zsource converter-derivation of AC small signal model and design-oriented analysis, IEEE Trans. Power Electron., 22(5): 1786-1796.
11. Shen, M., A. Joseph, J. Wang, F.Z. Peng and D.J. Adams, 2007. Comparison of traditional inverters and Z-source inverter for fuel cell vehicles, IEEE Trans. Power Electron., 22(4): 1453-1463.

12. Tang, Y., S.J. Xie and C.H. Zhang, 2007. Z-Source AC-AC converters solving commutation problem, IEEE Trans. Power Electron., 22(6): 2146-2154.

13. Loh, P.C., F. Blaabjerg and C.P. Wong, 2007. Comparative evaluation of pulse width modulation strategies for Z-source neutral-point-clamped inverter, IEEE Trans. Power Electron., 22(3): 1005-1013.