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π/4DQPSK Transceiver Design with Efficient Exploration of Advance Design System (ADS)

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Abstract: The world is advancing at a faster rate. There was a time when wired technology was considered as something unrealistic whereas now people have started discussing wireless technology (WIFI, WIMAX etc). The software ADS is a step towards this development. Advance Design system is a software build for RF and microwave related simulations. Both analog and digital simulations can be performed on the software. There were a number of modulation techniques that could be used to perform the transceiver operation as DQPSK, QAM, 256 QAM, pi/4 DQPSK etc. Considering our requirement the best suited technique was pi/4 DQPSK. In this paper the design and analysis of DQPSK system is given by using ADS software.

Key words: ADS · DQPSK · S-Band · BER · PSK

INTRODUCTION

This work is an attempt to make a wireless transceiver for S-Band supporting data rate of 1.5Mbps. The signal initially would be in VHF band that is 70MHz, which then would be taken to S band that is 2.4GHz. Numerous modulation techniques can be utilized for this purpose that includes ASK, PSK, FSK and DQPSK etc. DPSK is the differential PSK that basically codes the difference between the current input at any point and delayed output at that point. Further, ASK can be very easily subjected to noise as it uses the amplitude as the varying factor. Frequency modulation can be prone to noise easily that creates errors at the receiving end. Keeping in view our requirement, the modulation scheme used for the transmission and reception is DQPSK. The signal lost at any of the stages during processing can be recovered as we have two channels, I and Q channels. Since the signal is going to be propagated in the atmosphere at a very high frequency and altitude, the choice of modulation scheme becomes critical so that environmental degradations can be brought to an acceptable level. All simulations are performed on Advanced Design System, a product of Agilent Technologies. Different constellations, eye diagrams and other graphs have been obtained at each stage to provide complete circuit description [1]. The system consists of two paths, one path forms a normal RF communication link from the transmitter to the receiver via antenna and the second path provides bit error rate (BER) [2] calculation which compares the signal transmitted from one end with that received at the other end. To start with the system we had different options in ADS. The data can be taken in analog form and can be converted into digital form using ADC and similarly vice versa is also possible. For both, the simulations are a little bit different, analog approach requires the selection of Analog RF network option and for latter case Digital RF network option needs to be selected. The approach used in this work for the transmitter is to take the digital data initially and to convert it into analog which should then be propagated through antenna [3].

The transmitter function starts with the data source i.e. bit sequence. Bit sequence can be random or it may be some standard sequence. The bit sequence selected in our case has been random one with probability of zeros being 0.5. The data is in digital form and needs to be converted into a continuous time signal for further processing. Logic to NRZ block of ADS has been used for this purpose that converts the logic 1 and 0 into logic 1 and -1. This avoids DC biasing in the circuit. Output from this block goes into Float to timed block. The function of the block is to convert the sequence into a time based signal. Over sampling of the obtained analog signal is then performed with a sample and hold block. Since the modulation scheme used for the transmission and

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reception is DQPSK, the signal needs to be converted into I and Q channel. The function is performed using data splitter. IQ channel is encoded using ð/4 DQPSK scheme. The two signals are passed through Raised Cosine filter that acts as Low Pass Filter. The reason of using this filter is that it provides good pulse shaping of the signal through it. The data is finally QAM modulated to passband using carrier frequency of 70MHz. The IQ channel is converted into IF modulated format. The sampled base band signal is up converted to an IF frequency. The step conversion takes the signal from 70MHz to 2.4GHz [4]. If the transmission is required to be in some higher band as Ku-Band, K band etc, further up conversion is needed to take the signal to a higher frequency band. The additional stage required for this up-conversion involves mixers and oscillators, choice of which is very sensitive as hardware challenges and tolerances should be kept in mind too. Hence substantial amount of calculations would be required for the up conversion of the IF signal. The signal passing through raised cosine filter has partial distortions that are intentionally inherited in the system as noise density, temperature variation so as to have a considerable value of BER [5]. The signal is ready for transmission, which is finally transmitted via antenna. Gain of the antenna can be set according to the signal strength required and considering the signal degradation factors in the environment. To make the simulation close to a practical scenario, noise is deliberately inherited in the signal which is then received by the receiver. At the receiving end, firstly the pass band signal is brought to baseband. The signal has two components, noise and the information. If mixers are made the first stage of the receiver there is a chance that noise might propagate through and get doubled in the recovering process as mixer isn't truly a noise sensitive device. To cater this problem Low Noise Amplifier (LNA) can be used, that makes the signal free of noise and at the same time amplifies it too by a significant amount. Filters again would be required for pulse-shaping and attenuation of the unwanted part of the signal in case if LNA is used. The Low pass filter choices are butter worth, Chebby Chev, raised cosine and elliptic filters. Both I and Q channel data is passed through the preceding stages and thereby comes the stage to reconstruct the signal transmitted with as much SNR as possible [6]. Down conversion of the signal is performed which brings the signal to the same 70MHz. Signal needs to be QAM demodulated, there after Low pass filter provides the pulse shaping of the signal. Signal is decoded using the same modulation scheme i.e. pi/4 DQPSK. Data combiner at the end transfigures the IF modulation formatted signal to the same IQ signal format [7]. The BER calculation involves a delay block that compensates for all the modulation and encoding pattern, after the delay a gain is inserted in the signal from where the signal is finally compared with that received [8,9].

System Description: Random Number Generator block is used to generate a series of bits consisting of 1's and 0's. Its parameters are 'Type', 'Prob of Zero', 'LFSR_Length' and 'LFSR_inistate'. 'Type' shows the type of bit sequence that is either random, prbs, random or pseudo random. 'Prob of Zero' is probability of bit value being zero; it can be used only when we select the 'Type' as random. Its range is [0, 1]. 'LFSR_Length' is linear feedback shift register length which can only be used when 'Type' is 'prbs'. Last parameter 'LFSR_inistate' is linear feedback shift register Initial state which is also used when 'Type' is 'prbs'.

The next block is 'Logic to NRZ'. It converts a logic level to NRZ level.Here this block is used for conversion of logic signal of 0 and 1 to floating number of -1 and 1. It depends only on the amplitude of NRZ signal. Its range is from – 8 to + 8.

'Float to Timed' block converts a floating point real signal to timed signal. If input is floating point real signal then output is a real baseband timed signal. It has one parameter that is 'T Step' whose value is set equal to the inverse of the bit rate.

'U SampleRF' block up-samples an input timed signal to produce an output timed signal which is sampled with a time step and is equal to TStepOut = TStepIn / Ratio, where 'TStepIn' is the input time step. This block has 7 parameters: 'RIn', 'Rout', 'Rtemp', 'Type', 'Ratio', 'InsertionPhase' and 'ExcessBW'. 'RIn' and 'Rout' are input and output resistance respectively. They range from 0 to 8. 'Rtemp' is physical temperature in C which has range of [-273.15, 8). 'Type' can be up-sampling interpolation type, Sample and hold, zero insertion, poly phase filter or linear. Sample and hold is by default. 'Ratio' is up-sampling ratio. 'InsertionPhase' is up-sampling insertion phase for the output non-zero sample when 'Type' is Zero Insertion. 'ExcessBW' is excess bandwidth of raised cosine interpolation filter, used only when 'Type' is Poly Phase Filter.

The next block is 'SymbolSplitter' which is used to convert an input bit stream into two output bit streams: I and Q. Its parameters are 'RIn', 'Rout', 'Rtemp', 'Delay' and 'SymbolTime'. 'Delay' is data input time delay from t=0 for start of the data stream, while 'Delay' is equal to -1 for auto synchronization. 'SymbolTime' is the input data symbol time whose range is [Tstep, 8].

'EncoderIQ' is encoder for IQ data. The input data signals are assumed to be in the NRZ binary format, with logic 0 level at -1V and logic 1 level at +1V. This component can be used to differentially encode data according to either the DQPSK or pi/4 DQPSK formats. Data encoding begins after the delay time has elapsed. Inputs are integrated beginning at t='Delay' and dumped at 'SymbolTime' intervals. The outputs I and Q are then calculated from the results of the integrate and dump operations. Due to this integrate and dump operation, the component introduces a delay of 'SymbolTime' at its output. Its parameters are 'RIn', 'Rout', 'Rtemp', 'SymbolTime', 'Delay' and 'Type'. Each of these parameters is discussed earlier. Only the parameter 'Type' is a new one, it is type of IQ data encoder, it uses only two schemes these are DQPSK and pi/4 DQPSK.

'LPF_RaisedCosine Timed' is a lowpass cosine filter. Its parameters include 'RIn', 'Rout', 'Rtemp', 'Loss', 'CornerFreq', 'ExcessBW', 'Type', 'SquareRoot', 'Delay' and 'WindowType'. 'Loss' shows the power loss, measured in dB, referenced to matched source and load resistors. Its range is from [0, 8). 'CornerFrequency' is equal to half of symbol time. 'Type' is type of raised-cosine model i.e. Impulse model or Model with pulse equalization. 'SquareRoot' is just asking of whether to use the square-root raised-cosine model, its answer will be just No or Yes. 'Delay' is filter time delay. User can give it any value but recommended value is 4*symbol time. Delay range is (0, 8). 'WindowType' is window applied to filter impulse response i.e. Rectangular, Bartlett, Hanning, Hamming or Flat Top.

'QAM_Mod' block is Quadrature Amplitude Modulator with internal oscillator. It takes I and Q baseband input signals and as an output it gives a QAM RF signal. Its parameters are 'RIn', 'Rout', 'Rtemp', 'FCarrier', 'Power', 'VRef', 'Phase', 'Gain Imbalance' and 'PhaseImbalance'. 'FCarrier' is the carrier frequency ranging from (0, 8). 'Power' is the modulator output power. 'VRef' is the modulator voltage reference level. 'Phase' is the reference phase in degrees. 'Gain Imbalance' is the ratio of Q channel to I channel, measured in dB, while 'PhaseImbalance' is ratio of Q channel to I channel but is measured in degrees.

Next block is called 'RF_TX_IFin'. It is RF transmitter with IF input and two filter amplifier pairs. The transmitter is used for the purpose of converting input IF signal to output RF signal with nonlinear distortion and additive noise. Nonlinear distortion is determined by the 'PSat' parameter. 'PSat' can models am-am distortion only. Its parameters include 'RIn', 'Rout', 'IF_Freq', 'RF_Freq', 'RF_BW', 'TX_Gain', 'PSat' and 'NDensity'. 'TX_Gain' is transmitter power gain in dB. 'PSat' is saturated output power. 'NDensity' is noise spectral density at output, in dBm/Hz. Range of 'TX_Gain' and 'NDensity' is (-8, +8) while range of all other parameter is (0, 8) and type of all parameters is real.

The next block is 'AntBase' that is Base Station Stationary Antenna Model. Base or fixed station antennas are linearly polarized antennas and are used in mobile communication services at the base station of a radio relay link. It has four parameters: 'Gain', 'X', 'Y' and 'Height'. 'Gain' is gain of the antenna measured in dB, 'X' is x-position coordinate and 'Y' is y-position coordinate while 'Height' is height of antenna above X-Y plane. 'X', 'Y' and 'Height' are measured in meters.

'AddNDensity' block is named after Add noise density to input signal. It adds white Gaussian noise of the specified noise density to the incoming signal.Input signal power is saved when the component is connected to a matched load. It has three parameters:'RIn', 'Rout' and 'NDensity'. These parameters are already explained above.

'DelayRF' or Time Delay block delays the input signal by a certain 'Delay' time units. Its parameters are 'RIn', 'Rout' and 'Rtemp' which are already discussed. Other parameters are 'Delay', 'InterpolationMethod' and include carrier phase shift. 'Delay' is time delay and must be greater than or equal to TStep and is set to -1 for one TStep delay. Signal InterpolationMethod' may be linear or none. 'IncludeCarrierPhaseShift' tells whether to include phase shift or not. When the input is an RF time domain signal, the delay will be applied to the RF envelope and also (optionally) to the RF carrier phase when 'IncludeCarrierPhaseShift' is set as 'Yes'.

Next block is of 'TkPlot': plot inputs versus time. It has a few parameters which are very simple and self-explanatory. These are 'Label', 'Geometry', 'xTitle', 'yTitle', 'xRange', 'yRange', 'Persistence', 'Style', 'UpdateSize' and 'RepeatBorderPoints'. 'Persistence' is the number of points displayed on the plot at any time, while 'UpdateSize' is the number of new points plotted per plot update. 'RepeatBorderPoints' are Repeat rightmost border point on left border, it has just two options these are NO or 'YES'.

'TimedSink' is used as timed data collector which collects timed data from the output of the connected components and saves it to the simulation dataset. Timed baseband data is in the form of real voltage values versus time. It depends on 6 factors: 'Plot', 'RLoad', 'Rtemp', 'Start', 'Stop' and 'ControlSimulation'. "Plot? is used if

option is set to open data display (from the drop down menu) after simulation, "Plot? can be put to Rectangular or None. Software plots the data accordingly for the selected sink.

'RLoad' is load resistance, measured in ohm and ranges from (0, 8). 'Rtemp' is resistor physical temperature, measured in Celsius and range is [-273.15, 8). 'Start' is start time for data collecting, which has range of [0, 8). 'Stop' is stop time for data collecting. Its range is from [Start, 8). If 'ControlSimulation' is set to Yes then it tells how long the simulation will run. Its setting is just 'Yes' or 'No'.

The next block is of 'Gain'. It is very simple block and depends on only one parameter that is the factor gain whose value can be set by the user. 'RF_RX_IFout1' block is Single down-conversion RF receiver with IF output. It is a hierarchical model and is composed of some other components. The receiver is used to convert an input RF signal to an output IF signal with additive noise and nonlinear distortion. Its parameters are 'RIn', 'Rout', 'RX_AntTemp, RX_Gain', 'RX_NF', 'RF_Freq', 'RF_BW', 'IF_BW', 'IF_Freq' and 'IP3in'. Most of the parameters are discussed earlier. 'IP3 in' is the IP3 at the receiver input whose range is (-8, 8). 'RX_AntTemp' is receiving antenna noise temperature, measured in Kelvin. Its range is from [0, 8). 'RX Gain' and 'IP3in' determine the nonlinear distortion. 'RX_AntTemp' and 'RX_NF' parameters determine the additive noise.

'QAM_Demod' is Quadrature amplitude demodulator with internal oscillator. It has an internal oscillator which generates the require reference carrier signal, used to demodulate the RF signal. Its parameters include 'RIn', 'Rout', 'Rtemp', 'Ref Freq', 'Sensitivity', 'Phase', 'GainImbalance' and 'PhaseImbalance'. All these parameters are already discussed, the range of last four parameter is (-8, 8).

The next block is 'DQPSK_Pi4Decoder' which is used for pi/4-DQPSK IQ data decoding. This block is used when the differential encoding is required prior to modulation and the modulated signal is coherently demodulated. The output of the coherent demodulator should be fed directly to 'DQPSK_Pi4Decoder'. Its parameters include 'RIn', 'Rout', 'Rtemp' and 'SymbolTime'.

The next block is 'BinaryCombiner'. The input data signals are assumed to be in NRZ binary format with logic 0 level of -1V and logic l level of +1V. The output data is also in the binary NRZ format but with +1 and -1 levels and whose symbol time is half of the'Symbol Time'. The data combiner can perform the integrate and dump operation on the input data to determine the state of the input data. Its parameters are 'RIn', 'Rout', 'RTemp', 'Delay' and 'Symbol Time'. The value of 'Delay' is used to set the time instant at which the integration begins. If the value of the integral is positive at the end of the integration period, then a decision is made that the input bit is a +1, otherwise it is assumed to be -1. The integration period is equals to 'SymbolTime'.

'berMC' is another block used in our design also known as Error Probability measurement using Monte Carlo Method. It has 2 inputs and no output. 'berMC' uses the Monte Carlo method for probability of error measurement of linear as well as nonlinear communication systems.

The measurement is done by comparison of test data to reference data waveforms, symbol by symbol. It depends on many parameters those include 'Plot', 'Rload', 'Rtemp', 'Start', 'Stop', 'ControlSimulation', 'SymbolTime', 'EstRelVariance', 'NumThreshold', 'ThresholdSetting', 'Threshold', 'DelayBound', 'berOutput' and 'Status update period'. 'EstRelVariance' is estimation relative variance; if its value is set to 0.0, simulations will run until 'Stop' is reached. 'NumThreshold' is number of threshold range from [1, 8). 'Threshold' setting is type of threshold settings that whether we want it to be automatically or manually. To simplify detection, the parameter 'ThresholdSetting' is set to automatically and all detection thresholds are normalized from -1 to 1. 'Threshold' is the threshold values if user selects manual setting. The threshold range results in symbol ranges that are equally spaced between -1 and +1. 'DelayBound' is the upper bound of delay for synchronizing inputs. Its range is {-1} or (0, 8). 'berOutput' is type of ber output, it is bit error rate vs time. 'Status update period' is status update period in number of bits: range is [1, 8).

A schematic can include many numbers of variable items, these variables are stored in the 'VAR' block. A 'VAR' icon defines multiple variables or equations that are used in the design. Variable and equation names always begin with a letter and they should not exceed 32 characters. An important point is that names are always case sensitive in ADS.

'DF' block has different Data Types, Controllers, Sinks and Components.In some applications, particularly those which use timed components, data types can be thought of as signal types. Packets of data are passed from one component to another. The data point can be Scalar Fixed Point, Scalar Integer, Scalar Fixed Point (real), Scalar Complex, Scalar timed or other. Whenever we

connect components of the same data type (color), data is copied between different components. If we connect components represented by different data types, such as scalar complex to scalar floating-point (real), or scalar integer to matrix integer, the software automatically converts dis-similar data types to similar data types, such as complex to floating-point (real) or place an appropriate converter.Controllers are used to control the simulation and they are present unconnected anywhere in the design. They can be found in the Controllers library or palette. Sinks are components with no outputs. When a sink controls the simulation then 'ControlSimulation' is set as 'YES'. By default, a sink's 'ControlSimulation' parameter is set to 'YES'. Sources are components similar to sinks as they also have no inputs. Sources that read from files, instruments and datasets also have a 'ControlSimulation' parameter. By default, its value is set to'NO'. Controlling sources are used for the purposeof creating designs that process all the data in a file.

SIMULATION RESULTS

Now that all the blocks and their respective parameters have been explained, we move towards a graphical elucidation of the working of these blocks. Numerous options were there on bit sequence generation. The option taken was a random sequence of binary digits. Note the number of zeros and ones have equal probabilities in this sequence. The output of bit sequence generation block is given in Figure 1.

'LOGIC TO NRZ' block defines a step toward making the signal into an analog one as shown in Figure 2. We can see that the two states from the above random sequence i.e. 1 and 0 have been translated into -1 and 1 state. The 0.5 probability of the ones and zeros in this case is the probability of -1 and 1.

The signal has now been transformed into a continuous time based signal by using the 'Float to Time' block, as shown in Figure 3. The reason for this is to avoid DC biasing of the circuit.

The up-sampling of the analog signal is then performed as given in Figure 4. It should be noted that if the samples are taken at a rate lower than the highest frequency component of the signal then aliasing would occur which would result in the information loss.

Interpolation of the data has been performed and now the serial data is being splitted into the parallel I and Q channels respectively, as shown in Figure 5 and Figure 6. Information loss in any of the channel can be recovered easily from the other channel.

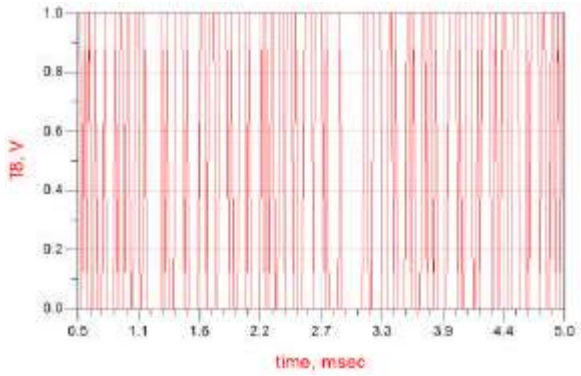


Fig. 1: Bit Sequence Generation

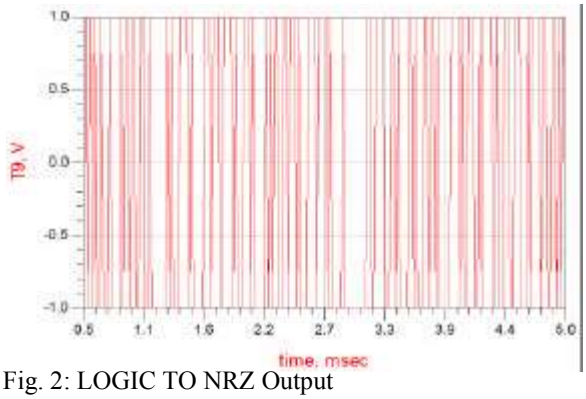


Fig. 2: LOGIC TO NRZ Output

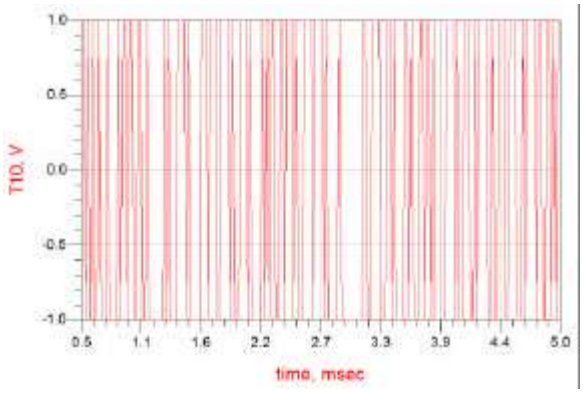


Fig. 3: Float to Time Output

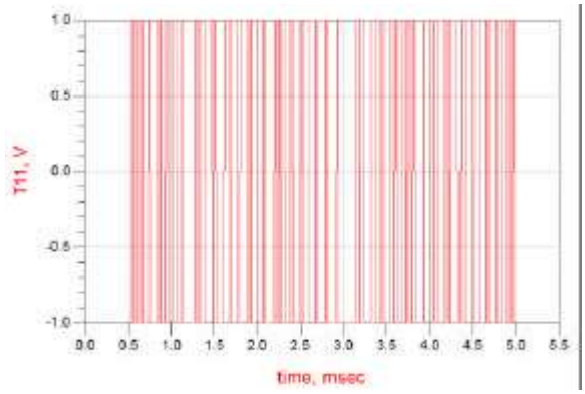


Fig. 4: Up-Sample RF Output

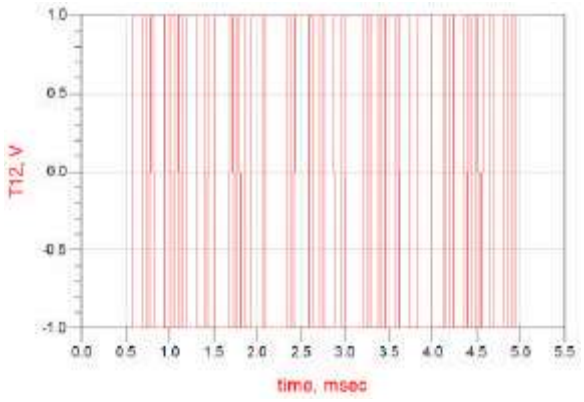


Fig. 5: Data Splitter I-Channel Output

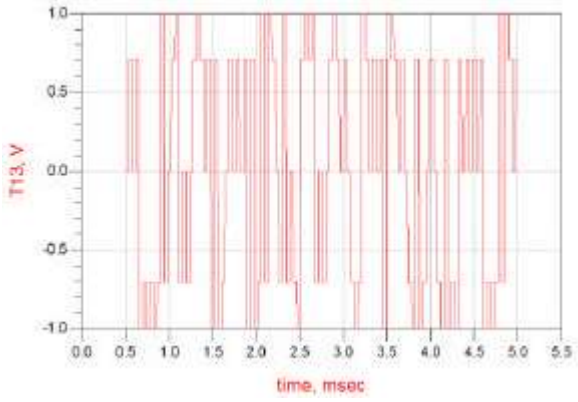


Fig. 8: Data Encoder Q-Channel Output

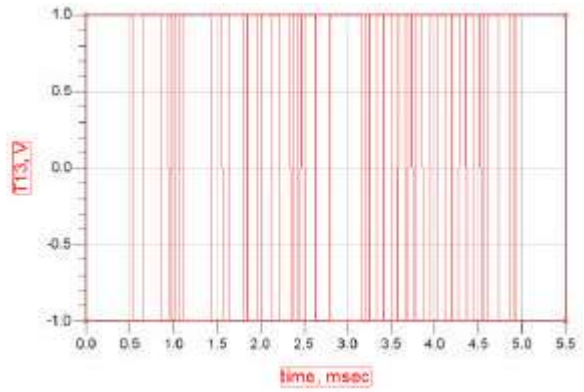


Fig. 6: Data Splitter Q-Channel Output

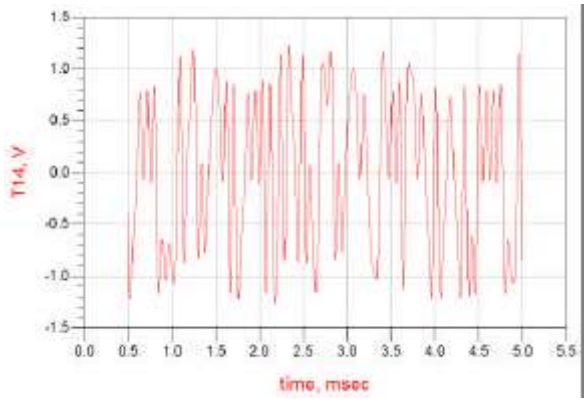


Fig. 9: LFP I-Channel Output

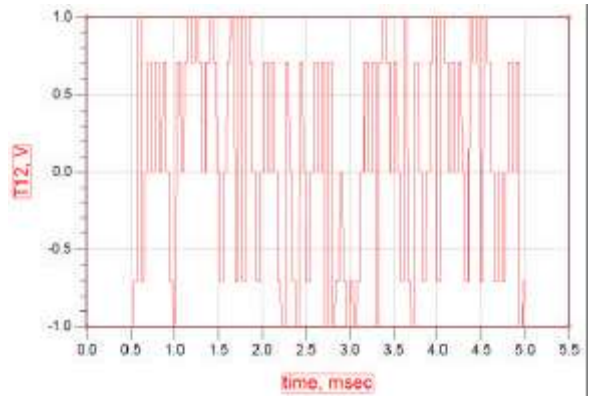


Fig. 7: Data Encoder I-Channel Output

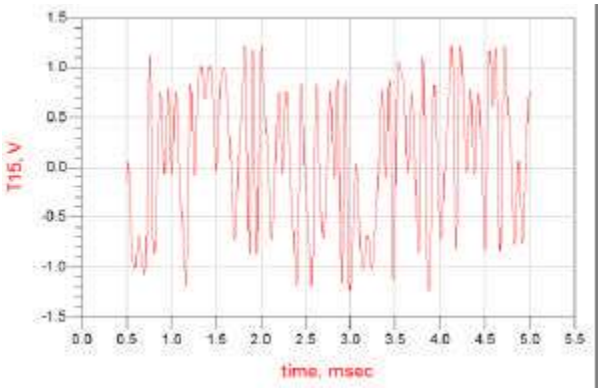
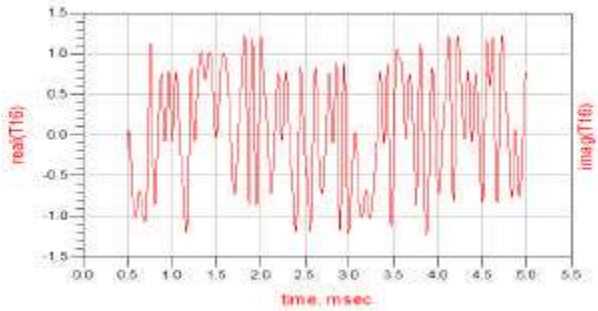


Fig. 10: LFP Q-Channel Output



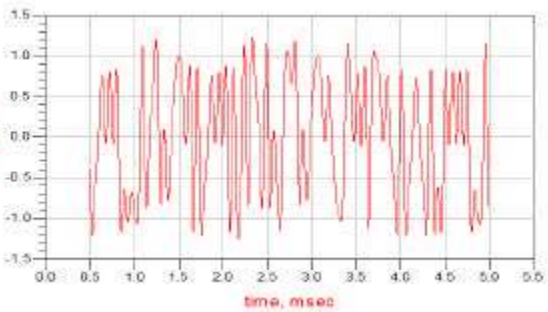


Fig. 11: QAM Modulator Output

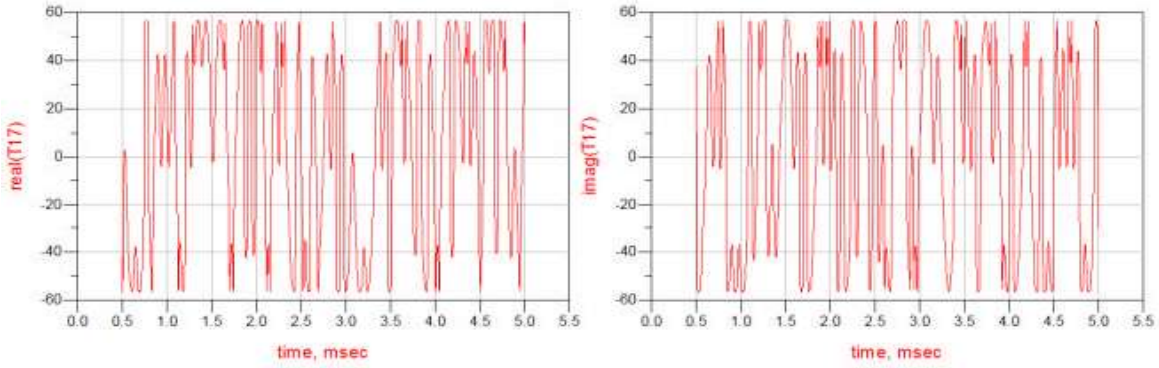


Fig. 12: IF-RF Output

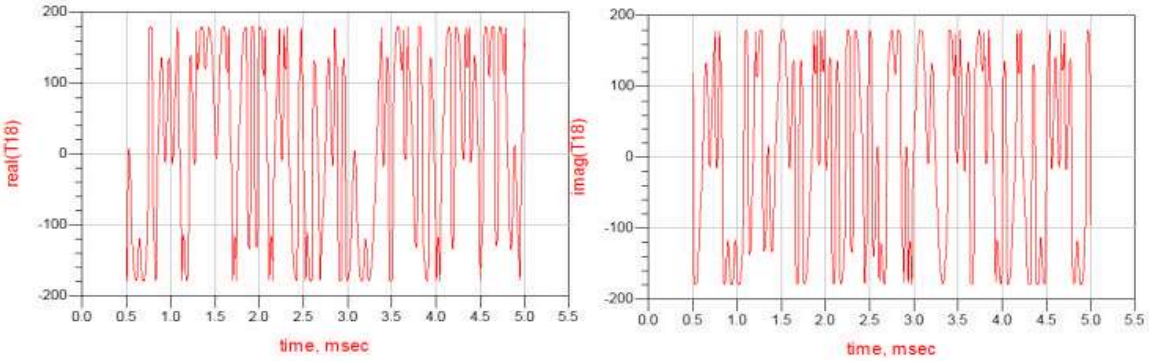


Fig. 13: Antenna Output

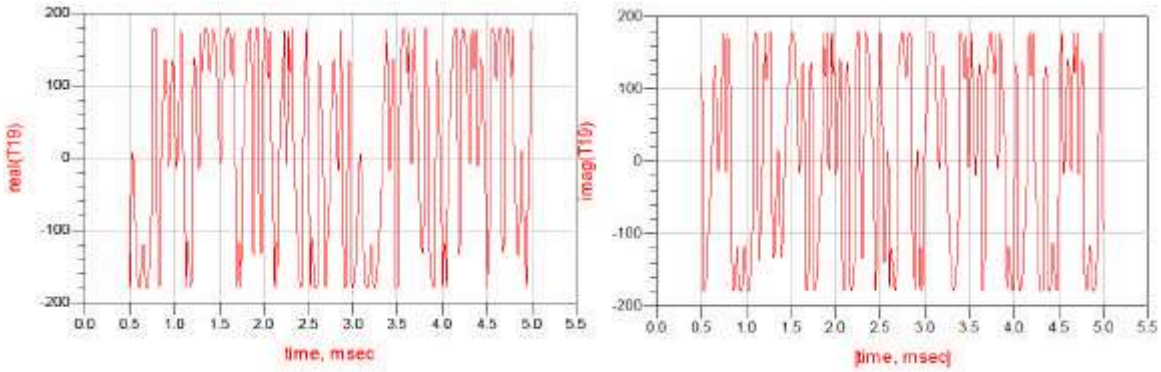


Fig. 14: ADD Density Output

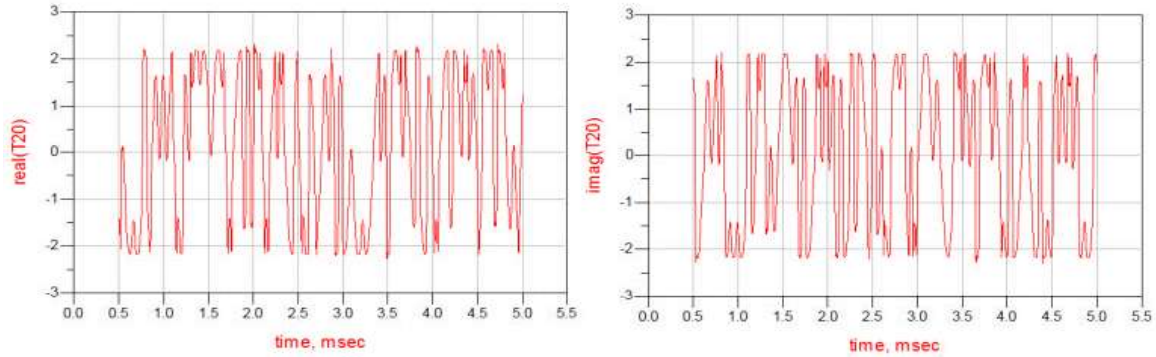


Fig. 15: RF-IF Output

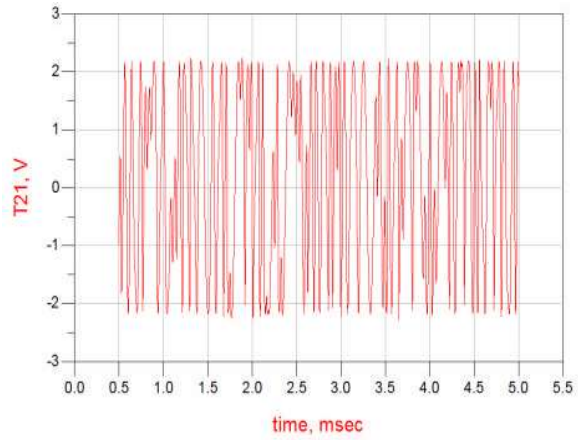


Fig. 16: QAM Demodulator I-Channel Output

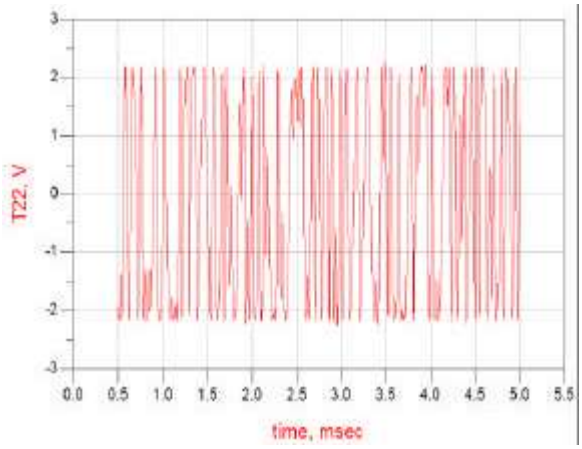


Fig. 17: QAM Demodulator Q-Channel Output

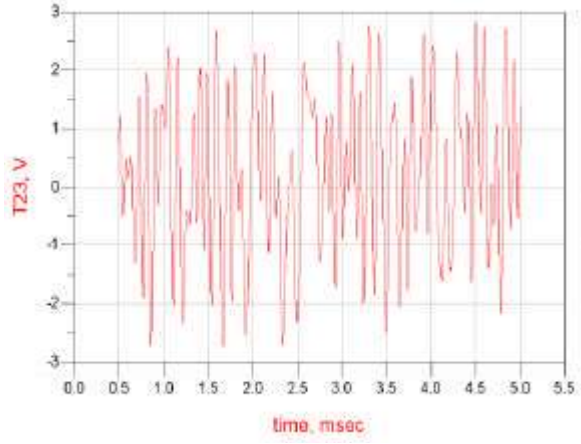


Fig. 18: LPF I-Channel Output

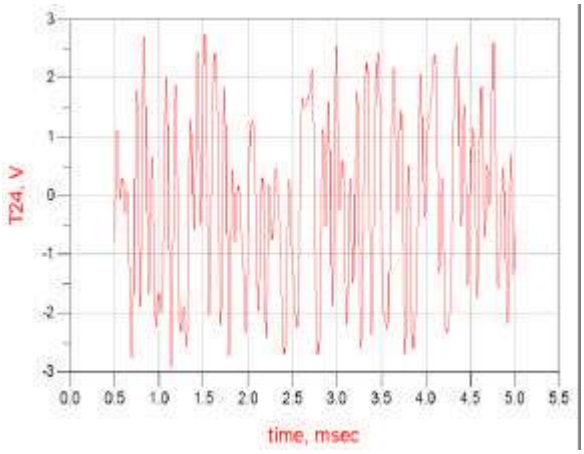


Fig. 19: LPF Q-Channel Output

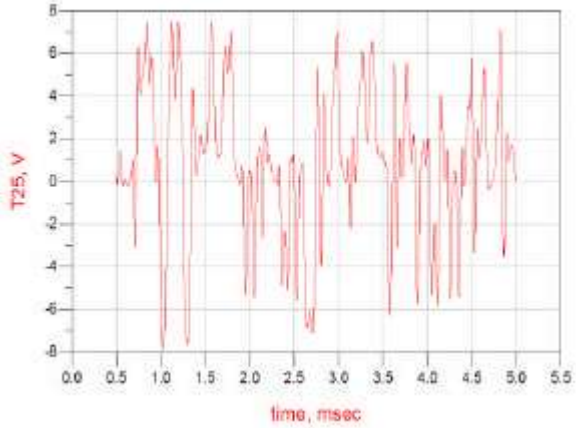


Fig. 20: DEC QPSK I-Channel Output

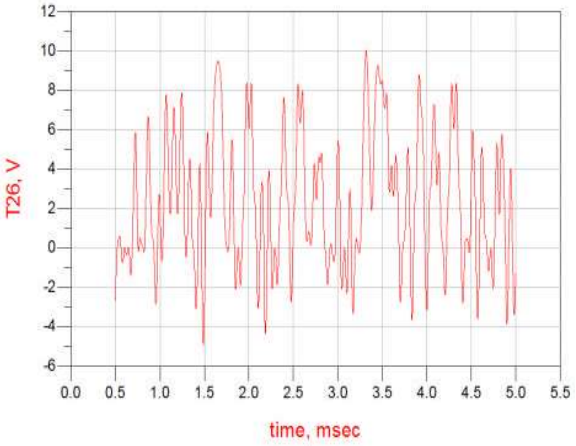


Fig. 21: DEC QPSK Q-Channel Output

Signal is going to propagated deep into the space and in order to avoid any loss of information or interruption from any external source, data has been encoded. Figure 7 and Figure 8 shows that both I and Q channel contain the information embedded in them, i.e. Phase of the data has been changed with the shape of the signal.

The filter with the property of pulse shaping has been chosen, which provides an ordered pattern of the encoded signal I and Q, given in Figure 9 and Figure 10.

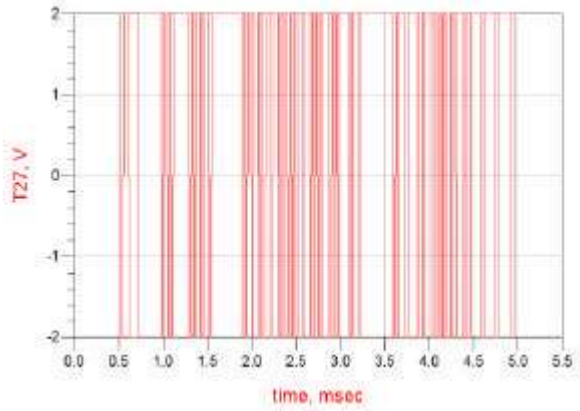


Fig. 22: Data Combiner Output

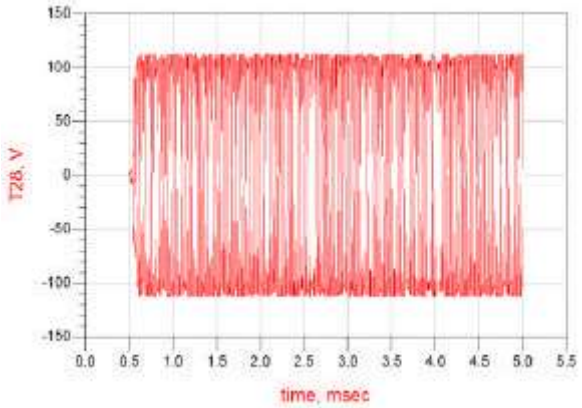


Fig. 23: Gain Output

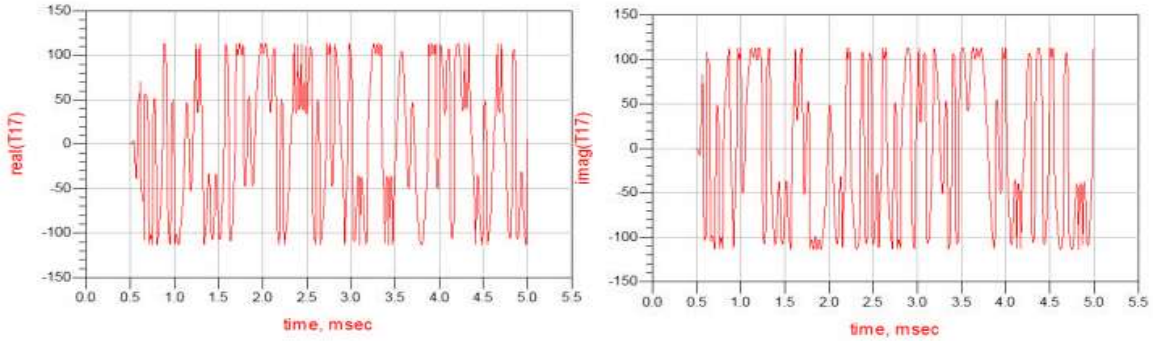


Fig. 24: Delay RF Output

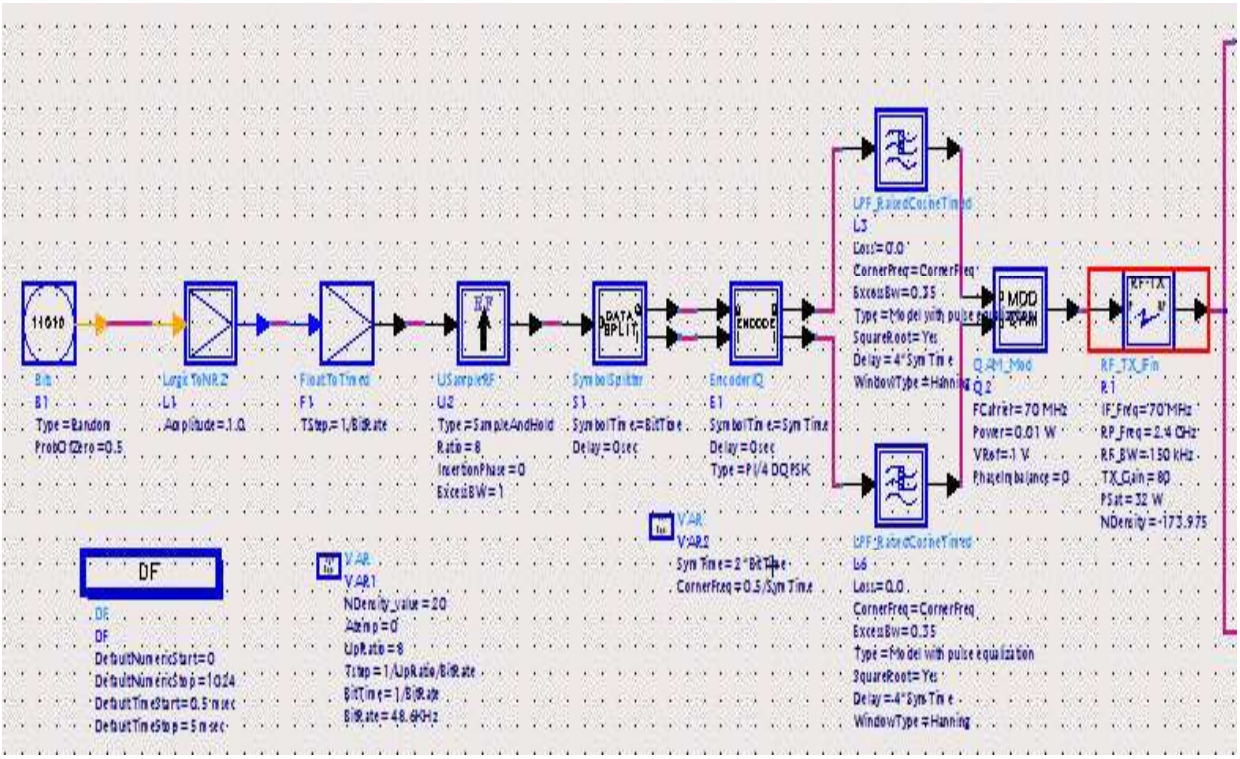


Fig. 25: Continued

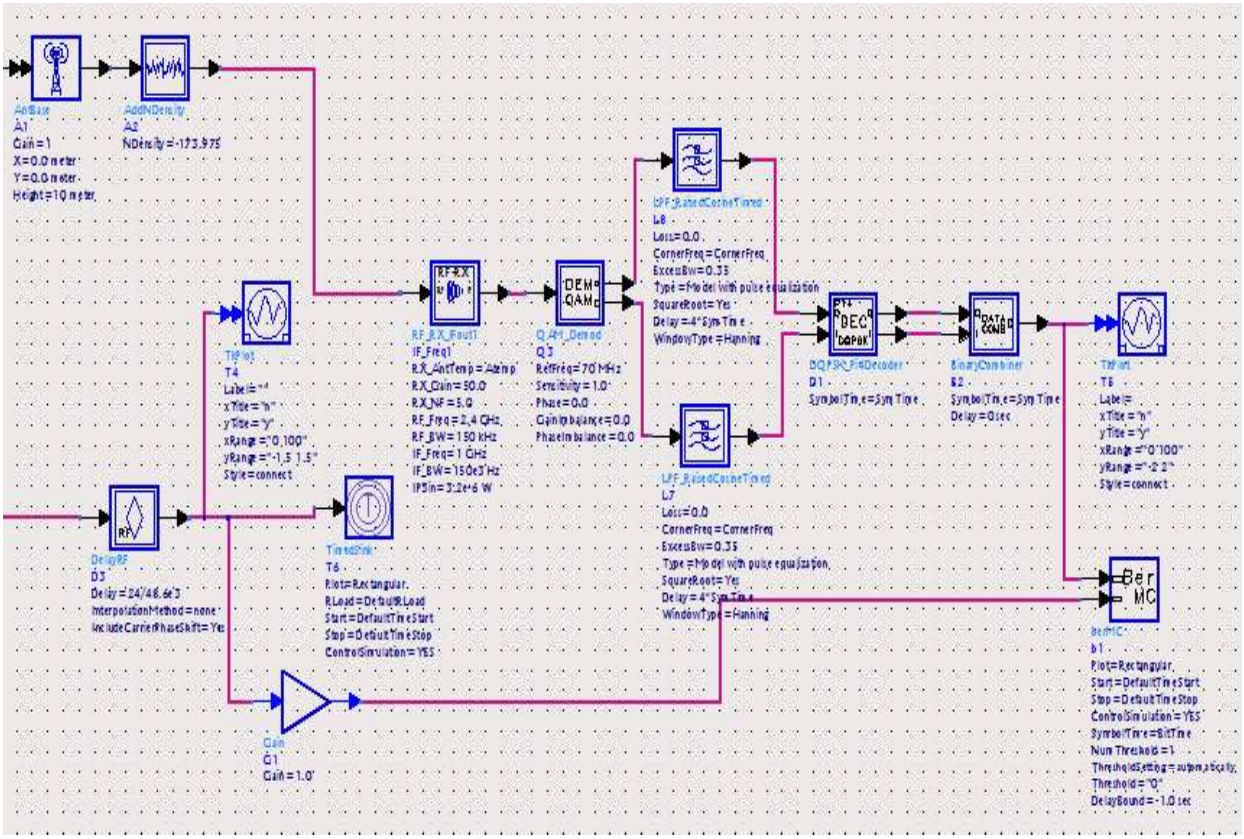


Fig. 25: System Model

Both the I and Q channel have been combined by the modulator which are going to be modulated to a higher frequency and it is very clear from the graph since the signal has become denser within the same allocated duration of time, as shown in Figure 11.

The data that was splitted into I and Q channel in the initial stages of the transmission has been combined into the same single signal showing pattern very similar to that of a binary signal as shown in Figure 21.

CONCLUSION

ADS software is inbuilt with all the modern components required to operate any communication operation. The product offers unique services in the results section as Constellations, Eye diagrams etc. The software is a product of Agilent Technologies and has undoubtedly earned significant reputation over the last few years. DQPSK has been derived from PSK in which the phase of the carrier wave is varied to convey information data on the other end. The problem with the PSK is that there comes an ambiguity In the phase of the signal once there is any change in the constellation. This can cause errors in the information. The reason to choose pi/4 DQPSK modulation scheme is that it can be detected using coherent detector, a differentiator or even discriminator followed by integrator. Coherent detection is more accurate but offers a higher level of complexity, on the other hand the other are more feasible to deal with practically. The proposed transceiver schematic uses raised cosine filter with an excess bandwidth of 0.35. Although differential encoding scheme protects any loss of data due to phase slips but it also results in a loss of a pair of symbols in case any error occurs.

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