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Design of Cntfet Based Ternary 2x2 Sram Memory Array for Low Power Application

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Abstract: In this paper, we have design of ternary 2x2 Sram memory Array using carbon Nano-tube field-effect transistors (CNTFETs).the CNTFET technology has new parameters and characteristics which determine the performances such as current driving capability, speed, power consumption and area of circuits have been proposed for ternary 2x2 Sram memory array is needed to optimize performance using CNTFET technology. The CNTFET used for design has different charity vector and threshold voltages of CNTFET transistor can be controlled by controlling the chirality vector. The channel length used here is 32nm wide. The power consumption is reduce compare to CMOS technology Second order effects are removed by using CNTFET. In a 3 Value Logic also Trivalent, Ternary, Trinary Logic, or Trilean sometimes abbreviated 3VL), it only takes *0, 1/2,1* bits to represent a binary number. In 3Value logic 6T 2x2 memory cell based CNTFET have been developed and extensive HSPICE simulations have been performed. The CNTFET based 3 value logic 6T ternary 2x2 SRAM array demonstrates that it provides low power dissipation and propagation delay which is better than CMOS 6T 2x2 SRAM array.

Key words: CNTFET · 3ValueLogic · HSPICE · Multi threshold value · FINFET · QDGFET · SNM · SWCNT · MWCNT · TEM

INTRODUCTION

Our goal is to design efficient ternary 2x2 Sram memory array with CNTFET using Ternary logic which can perform both read and write operation with low power consumption and high switching speed. This design also provides high noise margin and low area as CNTFET is used in the design. Large amount of data can be stored in smaller square area. a carbon Nano tube (CNT) is a hollow cylinder composed of one or more layers of carbon atoms arranged in a honeycomb lattice structure.A CNT with one layer of carbon atoms is called a single-wall CNT (SWCNT) and one with multiple layers is a multiwall CNT (MWCNT). An SWCNT can act as either a conductor (metal) or a semiconductor, depends on the angle of the atom arrangement along the tube. MWCNTs mostly show metallic behavior because of the increased probability of their having a metallic shell. Experimenters have used semiconducting SWCNTs to assemble electron devices similar to MOSFETs; these devices are known as CNFETs. CNFETs are promising Nano scale devices for implementing for low-power circuits. They've shown excellent electrical properties, including high trans conductance (ability to convert voltage into current) and high on/off current ratio (as a nearly optimal switch). From a CAD perspective, using numerical techniques to simulate a circuit in which multiple devices are present, such as CNTs with different diameters, is challenging because of the extensive processing usually required. For example, the numerical model of FET Toy uses a composite trapezoidal (Newton-Cotes formula) integration method for calculating charge densities. The carbon nano tube field-effect transistor (CNTFET) is a rising technology to a well-known bulk MOSFET for low-power and high-performance designs due to the realistic transport [4-6]. In a CNTFET, the threshold voltage is determined by chirality factor,

In this paper, 3 value logic ternary 6T 2x2 Sram memory cell are evaluated and compared with CMOS Sram memory cell in various simulation conditions and test benches by using novel efficient performance matrices. For 3 value logic ternary 6T 2x2 SRAM cell similar qualitative behavior has been observed as found. At a circuit level design of CNTFET, the analysis and

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simulation for selection of optimum diameters for optimized threshold voltages of the two types (i.e. N or P) of CNTFETs are also performed to achieve the best overall performance in terms of power consumption, propagation delay. Experimental results demonstrate that 3 value logic ternary 6T 2x2 SRAM cell outperforms better than 6T CMOS SRAM cell in terms of dynamic power dissipation and delay. The separate features of the proposed circuit for the write and read operations make this design very efficient.

The rest of this paper is organized as follows. Section II starts with brief review of the characteristics and physical features of carbon Nano tube transistors and threshold calculation Section III. The 3Value logic design and 6T standard ternary inverter Section VI. Circuit diagram for 6T Cntfet based Sram memory cell V. Design ternary 2x2 memory Array based three value logic Cntfet VI. Simulation results, simulation setup for a memory cell, measure such as power dissipation and delay are simulated by HSPICE in Section VII concludes and future work for this paper.

Carbon Nanotube Field-Effect Transistor: Carbon Nano-Tube Field Effect Transistor (CNTFET) is one of the emerging FET technologies in the VLSI industry.The exceptional electrical properties of carbon Nano-tubes arise from the unique electronic structure of graph here itself that can roll up and form a hollow cylinder. The CNT is connected between source and drain regions replacing the channel material instead of bulk silicon in the MOSFET structure. The circumference of such carbon Nano-tube can be expressed in terms of a chiral vector, which connects two crystal graphically equivalent sites of the two-dimensional graph here sheet. Here *n* and *m* are integers and $\hat{a}_1$ and $\hat{a}_2$ are the unit vectors of the hexagonal honeycomb lattice. Therefore, the structure of any carbon Nano tube can be described by an index with a pair of integers (*n*, *m*) that define its chirality vector. the chirality vector determines the diameter, the threshold voltage and whether the tube will behave as a metallic or semiconducting tube integers (*n*, *m*), the Nano tube diameter d_t

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm}$$

In the last decade two different CNTFET circuit design techniques have been used in the literature, One of them is directly replacing the MOSFET with CNTFET to approach better performance; The second is used CNTFET as a particular nanotechnology devices with its powerful CNT characteristics [1]. Fig.1 shows the schematic diagram of SWCNTFET. Transistors[16] which use SWCNT have many benefits rather than silicon MOSFET counterpart such as high density of on current and moderately high Ion/Ioff ratio that has many effects on frequency and changeable threshold voltage depending on carbon Nano tube diameter which is an important characteristic of CNTFETs.

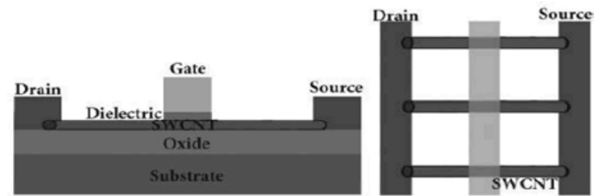

Fig. 1: Schematic Diagram of CNTFET

The threshold voltage is defined as the tube diameter and indirectly in terms of the chirality vectors; the threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half-band gap that is an inverse function of the diameter [9-11].

Threshold Voltage Calculation: The threshold voltage of the CNTFET used can be varied by altering the diameter of the CNT used between the source and drain of the FET. The diameter of the circuit is varied by altering the chirality vectors associated with that CNTFET. This is the main advantage of CNTFET over the MOSFET in which the threshold voltage is altered without increasing the no. of voltage sources which increases the cost and the chip area of the circuit.

Where {n, m} are the chirality vector of the CNT used in the CNTFET and a0 =0.142nm is the inter atomic distance. The formula to calculate threshold voltage from the obtained diameter is given below

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}}$$

Where a = 2.49 A° is The chiralities of the CNTs used in T1/T5, T2/T6 and T3/T4 are (19, 0), (10, 0) and (13, 0), respectively. Figure.6. circuit diagram for 6T CNTFET based Sram memory cell the diameters of T1/T5, T2/T6 and T3/T4 are 1.487, 0.783 and 1.018 nm, respectively. Threshold voltages of T3 and T9, T4 and T10, T5 and T11 are 0.289, 0.559 and 0.428 V, respectively.

The threshold voltages of the P-type CNTFETs T7 and T13, T8 and T14, T6 and T12 are -0.289, -0.559 and -0.428 V; respectively extensive research has been reported on manufacturing well-controlled CNTs [17]. In this paper, CNTFETs with different diameters are utilized and channel length of 32nm is selected for area efficient 3 value logic CNTFET based SRAM design.

Three Valued Logic: Multi-valued logic (MVL) has attracted considerable interest due to its potential advantages over binary logic for designing high performance digital systems. Theoretically, MVL has the potential of improving circuit performance Nowadays Ternary Logic is increasingly used in design of digital circuits, electronics and telecommunications [2]-[3]. Compared to a binary design, a ternary logic (or three-valued logic) implementation requires fewer operations, less gates and signal lines; hence, it is possible for ternary logic to achieve simplicity and energy efficiency in digital design, because this type of logic reduces the complexity of interconnects and chip area. In a ternary system, it only takes log3 (2n) bits to represent an *n*-bit binary number [7]. Ternary logic functions are defined as the functions having significance if a third value is introduced to the binary logic. In this paper, 0, 1/2 and 1 denote the ternary values to represent false, undefined and true, respectively. Any n-variable {X1,...,Xn} ternary function f(X) is defined as a logic function mapping {0,1/2,1}n to {0,1/2,1}, The Standard ternary inverter (STI) is the most widely used type of ternary inverter in digital circuits[2]. The STI has two different types with the no. of transistors used in it. They are 3T STI AND 6T STI where numerical value denotes the no. of transistors used in the circuit. Both the STI's are used in circuits based on constraints with the demand in the industry

6T Standard Ternary Inverter: The 6T STI consists of six CNTFETs, out of which there are three N-CNTFET T1, T2, T3 and three P-CNTFFET The chiralities of the CNTs used inT1, T2 and T3 are (19, 0), (10, 0) and (13, 0), respectively. The diameters of T1, T2 and T3 are 1.487, 0.783 and 1.018 nm, respectively. Therefore, the threshold voltages of T1, T2 and T3 are 0.289, 0.559 and 0.428 V, respectively. The threshold voltages of T5, T6 and T4 are -0.289, -0.559 and -0.428 V, respectively. When the input voltage changes from low to high at the power supply voltage of 0.9 V, initially, the input voltage is lower than 275 mV. This makes both T5 andT6 turn ON, both T1 and T2 turn OFF and the output voltage0.9V, i.e. logic 2. As the input voltage increases beyond 300mV, T6 is OFF and T5 is still ON. Mean while, T1 is ON and T2 is OFF. The diode connected CNTFETs T4 and T3 produce a voltage drop of 0.45 V from node n2 to the output and from the output to n1 due to the threshold voltages of T4 and T3. Therefore, the output voltage becomes 0.45 V, i.e., half of the power supply voltage. As shown in Table I, half Vdd represents logic 1.

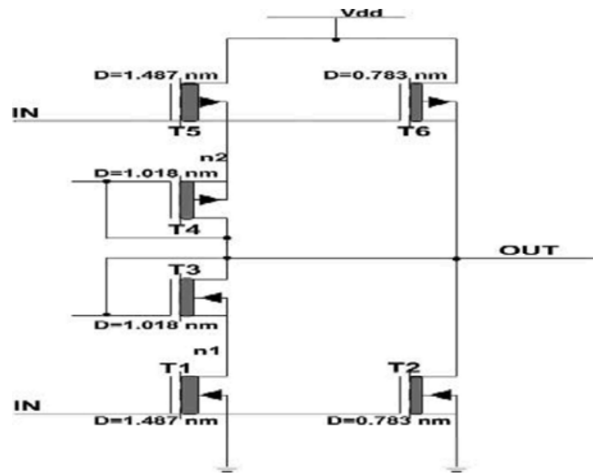

Fig. 2: Schematic of 6T STI

Table 1: Truth table of 6T-STI

IN	OUT
0	1
½	1
1	0

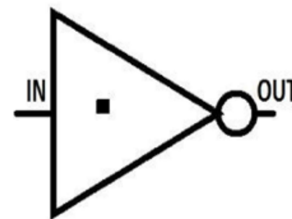

Fig. 3: Symbol of 6T STI

Once the input voltage exceeds 0.6 V, both T5 and T6 are OFF and T2is ON to pull the output voltage down to zero. The input voltage transition from high to low transition is similar to the low to high transition. This 6T-STI is used in most of the digital design based on the logic used[7].

Other logic gates like NOR, NAND gates can be designed using this ternary logic. The main requirement of ternary logic is multi-threshold voltage FET devices. In case of MOSFET, multi-threshold voltage can be

obtained using multiple power supplies which causes size and cost of a simple inverter is very much higher than of other type of FETs. But in the CNTFET multi-threshold voltage can be obtained by changing diameter of the carbon Nano-tube which is used in the corresponding FET, with single power supply can be used for all the CNTFETs used in the circuit.

Circuit Diagram 6t Ternary Memory: The 6T ternary memory cell design is shown in the schematic form in Fig. 4 and its transistor-level implementation is shown in Fig. 5. The write bit line wbl, is connected to the input of the write access gate which is a transmission gate. The transmission gate consists of two control inputs write word line bar, wwlb and write word line wwl. When wwl is high the transmission gate is ON and the wbl is connected to the input q of the cross coupled inverters. Whatever logic value present in the wbl is sent to the memory cell. The read bit line rbl, is connected to the input of the write access gate which is a transmission gate. The transmission gate consists of two control inputs write word line bar, rwlb and write word line rwl. When rwl is high the transmission gate is ON and the rbl is connected to the input q of the cross coupled inverters. Whatever logic value present in the memory cell is sent to the rbl with a delay due to the buffer.

As shown in Fig. 6, the memory cell consists of two transmission gates: one connected to wbl for the write operation and one connected to rbl for the read operation. The basic storage element of the proposed ternary memory cell consists of two back to back STIs, whose arrangement is very similar to a conventional binary cell, the basic storage element of this ternary memory cell consists of transistors T3–T14; they keep logic "0", "1/2" and "1" when the memory cell is holding data.

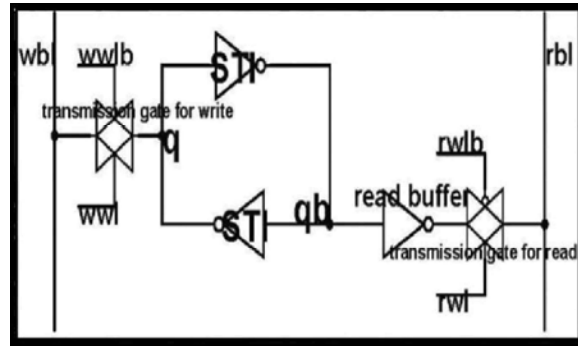

Fig. 4: Schematic of Memory Cell design

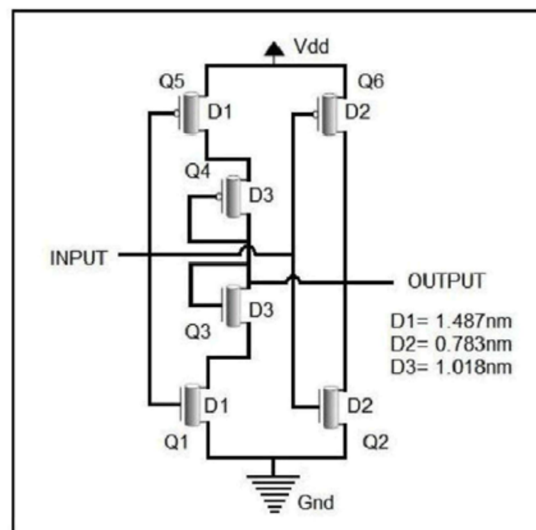

Fig. 5: 6T CNTFET BASED SRAM MEMORY CELL

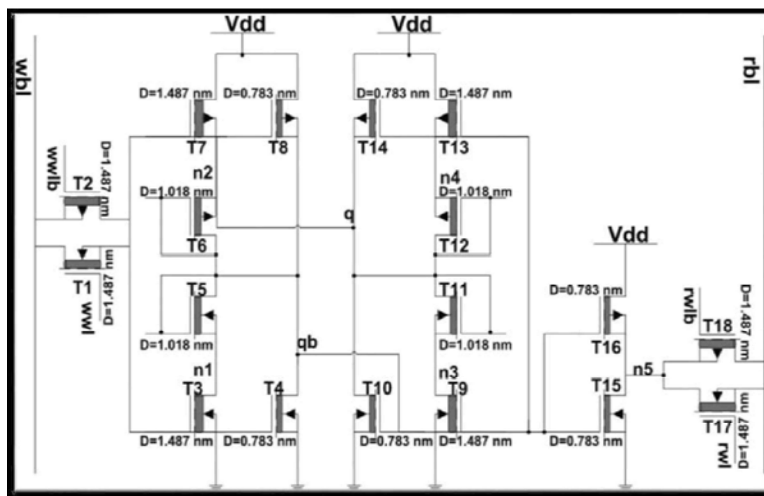

Fig. 6: Circuit Diagram for 6T CNTFET BASED SRAM MEMORY CELL

Ternary 2x2 Sram Memory Array:

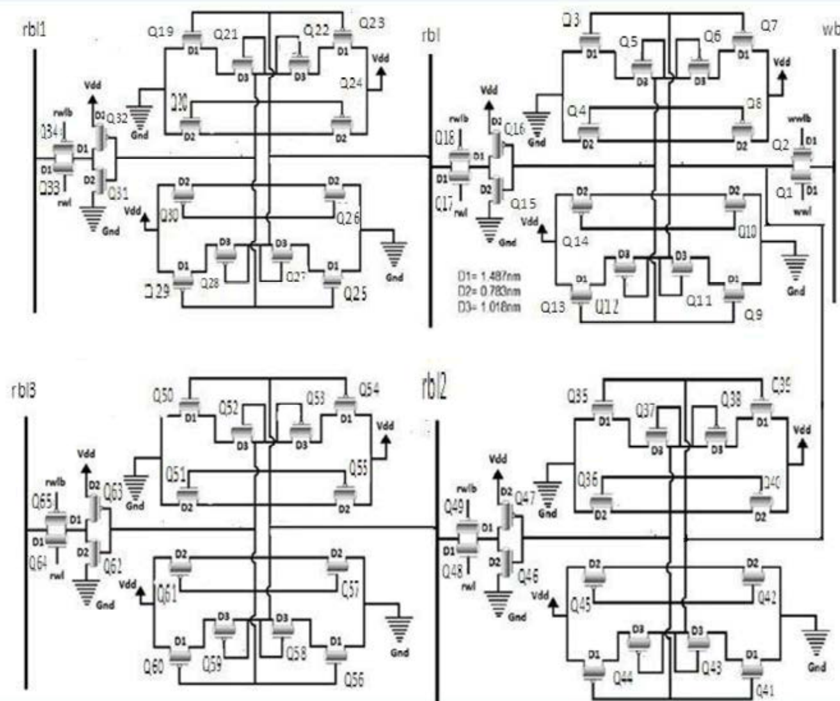

Fig. 7: TERNARY 2x2 memory Array

The proposed 2X2 ternary memory array design is shown in the schematic form in Fig. 7.

Write Operation: The write bit line wbl, is connected to the input of the write access gate which is a transmission gate. The transmission gate consists of two control inputs write word line bar, wwlb and write word line wwl. When wwl is high the transmission gate is ON and the wbl is connected to the input q of the cross coupled inverters. Whatever logic value present in the wbl is sent to the memory cell. The read bit line rbl, is connected to the input of the write access gate which is a transmission gate. When rwl is high the transmission gate is ON and the rbl is connected to the input q of the cross coupled inverters. Whatever logic value present in the memory cell is sent to the rbl with a delay due to the buffer. The operation of the proposed memory cell can be described as when the memory cell is holding logic“1/2”, transistors Q3, Q5, Q6, Q7, Q9, Q11, Q12, Q13 are ON to hold both nodes *q* and *qb* to the value of 1/2 Vdd; and when the memory cell is holding logic “0”,transistors Q6,Q7, Q8, Q9, Q10, Q11 are on to hold no de*q* to 0 and node *qb* to the value of Vdd; When the memory cell is holding logic “1”, transistors Q3,Q4, Q5,Q12, Q13, Q14 are ON to hold node *q* to Vdd and node *qb* to 0.The read operation is performed by the read buffer consisting of transistorsT15, T16, T17 and T18, with the threshold voltages of0.559, -0.559, 0.289 and -0.289 V, respectively. The read bit line rbl is precharged to 1/2 Vdd in the ternary memory. HSPICE simulation software is used write and read operation. The write transmission gate Q1 and Q2allows the correct data from data in to wbl to be written into the memory cell *q* and *qb*.

Read Operation: The read operation of the 2X2 ternary memory array is performed as follows: rbl is precharged to 1/2 Vdd prior to the read operation and the read transmission gates Q17 and Q18 are accessed to read the correct data from the memory cell. The read operation of the 2x2 ternary memory array has been simulated which operates as the ternary memory cell is storing a logic “1”; then, the read bit line rbl is charged to logic “1” when the read word lines rwl and rwlb are accessed. The ternary memory cell is storing logic “0”; the read bit line rbl is discharged to logic “0” when the read word lines rwl and rwlb are accessed. The ternary memory cell is storing logic “1/2”; rbl remains at logic “1/2”. A ternary STI is then connected to the read bit line rbl to sense the voltage at rbl. The power consumption is measured using HSPICE for the proposed 2X2 ternary memory array design.

The power consumption is reduced due to usage of ternary logic with CNTFET. Compared to the CMOS device, a CNTFET has a significantly smaller OFF current; so, the power consumed when the transistors OFF is greatly reduced in CNTFET designs. The CNTFET has a significantly higher ON–OFF current ratio compared to the MOSFET in the deep submicron range. The propagation delay is also reduced when compared to MOSFET circuits. For MOSFETCMOS circuits the minimum distance between pull up and pull down network must be 10 ë but with CNTFET circuit the same must be 3ë so the area can be reduced though Table 2 shows the power consumption and propagation delay of various Memory cells.

Simulation Results Analysis: The 6T ternary 2x2 SRAM Memory array based on CNTFET is designed at 32nm technology. This circuit is simulated in HSPICE model at 32nm feature size with supply voltage V_{DD} of 0.9V[9].

Simulation setup of 6T 2x2 Sram memory array using CNTFET Technology
Physical channel length (L_channel) =32.0nm
The length of doped CNT source/drain extension region (L_sd) = 32.0nm
Fermi level of the doped S/D tube (Efo) = 0.6 eV
The thickness of high-k top gate dielectric material (T_{ox}) 4.0nm
Chirality of tube (m, n) = (19,0)
CNT Pitch = 10nm

Flatband Voltage for n-CNTFET and p-CNTFET
(V_{fbn} and V_{fbp}) = 0.0eV and 0.0eV
The mean free path in intrinsic CNT (L_{ceff}) = 100.0nm The mean free path in p+/n+ doped CNT = 10.0nm
The work function of Source/Drain metal contact = 4.6eV

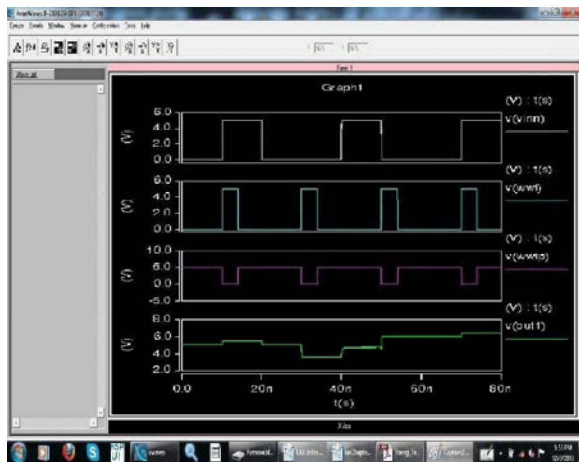

Fig. 8: Simulation Result of Ternary Memory cell write

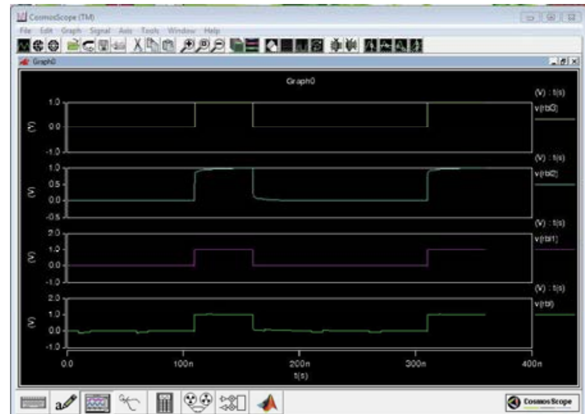

Fig. 9: Simulation Result of Ternary Memory cell read

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***** job concluded

******
**ternary memory cell.
****** transient analysis                tnom=  25.000 temp= 25.000

******
 propagation_delay= 9.9428E-09   targ= 3.0093E-08   trig= 2.0150E-08
 avgpower= 2.1457E-09  from= 1.0000E-09 to= 8.000E-08
 peakpower= 3.8326E-09      at= 5.0173E-08
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Fig. 10: Analysis Result of Ternary 2X2 Memory Array

Table 2: Result analysis of memory array Design

Parameter	Existing CMOS design	Proposed CNTFET based ternary design
Power consumption	1.33 x10-7 W	2.1457Nw
Propagation delay	12ns	9.9428ns

The power consumed by the ternary memory was reduced from 1.33 x10-7 W to 2.1457nW. This reduction in power is due to the usage of CNTFET. The propagation delay is also reduced from 12ns to 9.9ns which is caused due to ternary logic implementation

CONCLUSION

This paper has presented the first design of a ternary 2x2 Sram ternary memory array based on CNTFETs. As the threshold voltage of the CNTFET is the geometry of the CNTFET (i.e., the chirality and diameter), a novel multidiameter (multithreshold voltage) CNTFET-based ternary memory cell This memory cell does not require additional power supplies and the read/write operations are correctly executed by introducing in the design a transmission gate and a buffer to make these operations separate. Simulation results using HSPICE have showed that the proposed CNTFET-based ternary cell performs the correct function during the read and write operations. It has also been shown that the proposed ternary cells achieve a high SNM due to the separate read and write

operations, more than 90% lower standby power consumption for the "0" and "2"states and low area compared to a conventional binary CMOS, simulation results show that the proposed CNTFET-based ternary 2x2 memory array with substantial process variations still achieves the same SNM as its CMOS binary counterpart at 32 nm under ideal conditions.

Future Work: The future enhancement in this project is the improvement in the design of memory cell using CNTFET with 20nm technology i.e. the channel length is scaled down to 20nm in order to increase the performance of the circuit. With this improvement in the technology the various other storage cells are designed. Apart from designing memory cell with the standard ternary inverter one can design other storage components like flip flops, latches, shift registers.

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